Universität der Bundeswehr München
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18GHZ-36GHZ ROTARY TRAVELING WAVE VOLTAGE CONTROLLED OSCILLATOR IN A CMOS TECHNOLOGY

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Publications

The following articles resulted from this work

“ A 18GHz Rotary Traveling Wave VCO in CMOS with I/Q outputs”,
ESSCIRC 2003
”A 10Gb/s SONET Compliant CMOS Transceiver IC with Etremely Low Cross-Talk and Intrinsic Jitter”,
ISSCC 2004

Contents

List of Symbols

A_v	current gain	1
A	amplitude	V
C	capacitance	F
C_d	drain capacitance per meter	F/m
C_g	gate capacitance per meter	F/m
C_{ds}	Transistor drain-source capacitance	F
C_{gs}	Transistor gate-source capacitance	F
C_{ox}	oxide capacitance	F
C_{TAP}	tapping capacitance	F
C_f	fringe capacitance	F
C_{var}	variable capacitance	F
f_c	cutoff frequency	s^{-1}
FOM	figure of merit for oscillator	dB/Hz
g_m	small signal transconductance	S
G_m	large signal transconductance	S
G_{m-DVCO}	sum of transconductances for the DVCO	S
$G_{mNR-RTWVCO}$	sum of transconductances for the RTWVCO	S
I_{diff}	differential current	A

$I(z)$	current z coordinate dependent	A
i_n^2	squared noise current density	V^2/Hz
k	Boltzmann constant	$1.38.10^{-23} J.K^{-1}$
K_{VCO}	sensitivity of VCO frequency to tuning voltage variations	Hz/V
l	length	m
L	Length of transistor channel	m
L_{pl}	Inductance per length	$H.m^{-1}$
L_g	gate line Inductance	$H.m^{-1}$
L_d	drain line Inductance	$H.m^{-1}$
$L(\Delta\omega)$	Single side band phase noise	dBc/Hz
n	number of gain stages in the RTWO	1
N	number of couple gain-stage varactor in the RTWO	1
P_s	power spectral density of the signal	W
P_{diss}	power dissipated	W
Q	quality factor	1
Q_{loaded}	quality factor of the unloaded resonator	1
Q_l	quality factor of the transmission line	1
R	resistance	Ω
R_{gs}	gate resistance	Ω
R_{loop}	resistance of the resonator loop	Ω
R_{eq}	equivalent resistance	Ω
t	thickness	m
T	temperature	degree celcius
$u(t)$	unity function	
$V(z)$	z dependent voltage	V
V_{out}^l	output voltage at the left side of the line	V
v	celerity	$m.s^{-1}$
v_{phase}	phase celerity of the wave	$m.s^{-1}$
w	width of the line	m

W	width of the transistor channel	m
Z_0	impedance of the line	Ohm
Z_e	even impedance of a differential line	Ohm
Z_o	odd impedance of a differential line	Ohm
Z_0^d	drain line impedance	Ohm
Z_0^g	gate line impedance	Ohm
Z_0^i	termination impedance	Ohm
Z_{loaded}	loaded line impedance	Ohm
α	attenuation constant	Np/m
β	phase constant	rad/m
β_g	gate line phase constant coefficient	rad/m
β_d	drain line phase constant coefficient	rad/m
$\gamma = \alpha + j\beta$	propagation constant	
γ_g	gate line propagation constant	
γ_d	drain line propagation constant	
$\Gamma(\omega t)$	impulse sensitivity function	1
Γ_{rms}	rms value of the impulse sensitivity function	1
ϵ_0	permitivity in vacuum ($8.854.10^{-12}$)	F/m
λ	wavelength	m
μ_0	permeability ($4\pi.10^{-7}$)	H/m
$\delta(t)$	Dirac's impulse function	
ω_c	cutoff frequency of the transmission line	$rad.s^{-1}$
ω_r	resistive cutoff frequency of the line	$rad.s^{-1}$

Chapter 1

Introduction

This work describes the design and the fabrication of traveling wave voltage controlled oscillator in CMOS technology.

1.1 Objectives

As the bandwidth demand for data continues to grow, for Ethernet applications (IEEE 802.3ae) as well as for serial or optical backplane (SONET OC-192), low cost transmitter/receiver circuits stay increasingly challenging. With scaling, advances in complementary metal-oxide-semiconductor (CMOS) technologies made from it a serious competitor to the traditional SiGe, GaAs and bipolar technologies which becomes too power hungry and too expensive for a relatively low yield. The demand for lower cost, fast time-to-market and high level of integration makes the CMOS technology a good candidate. The 0.13 μm CMOS process has transistors with f_t of more

than 65GHz. However low power supply voltage (1.2V for the technology used in this work) makes design of the analog front-end very challenging. One of the critical blocks in receivers for optical communication is the clock and data recovery (CDR) which produces a timing clock signal from a stream of binary data (NRZ). One important component of the loop is the voltage controlled oscillator (VCO). Jitter requirements impose an upper bound on the VCO phase noise. The high frequency operation and the stringent jitter specifications make the design of the VCO a delicate task. The different architecture of VCOs are usually the ring oscillator, the relaxation oscillator, or the LC-tank VCO. Two phases at least are often needed in the transceiver architecture. The VCOs offer the possibility to generate multiple phases but at the cost of a high power consumption and/or instability risks of oscillations. CMOS technology offers now features which make it possible to implement strip-lines on chip. One reason for this is that the distance between the substrate and the top thick metal layer is sufficiently large. This yields a good enough property for high speed applications, despites a low resistivity substrate[23] [24]. The monolithic transmission lines on a CMOS chip offer new design opportunities, among them, new architecture of high speed oscillators.

1.2 Topic of the work

To obtain a VCO generating quadrature phase signals with low phase noise a new topology of oscillator is proposed based on a distributed resonator principle. The resonator composed of a strip-line pair integrated on the top metal layer is loaded with gain stages which are responsible for a sustained electrical wave to propagate in the resonator loop indefinitely. The topology

allows an easy access to different phases of the signal and generates outputs with low phase noise making it a good candidate for PLLs and CDR applications especially at frequencies close to the limit frequency of the active elements from the technology used. This is not the first study of this relatively new and promising structure, but it is surprising that only a few publications [25] have been written until now. The aim of this work was to implement the rotary traveling voltage controlled oscillator (RTW-VCO) on a CMOS process, and to measure its performances at different frequencies. A design procedure had to be found, to optimize between quality factor and minimum negative resistance. Design trade-offs for the resonator, the tuneability and the dimension of the gain stages have to be investigated. Layout considerations for practical implementation on the CMOS process are presented too. An analytical model of the phase noise based on the Hajimiri's theory is developed for the RTWO. The expression shows the influence of parameter variation on the phase noise which can greatly influence the design. The model is compatible with the Leeson's model and the newly developed model for distributed VCO of C. White.

1.3 Thesis organization

Chapter 2 introduces the basic concept of distributed amplification. First the ideal distributed amplifier (DA) is described. Then the non ideal effects occurring in an integrated circuit are discussed.
Chapter 3 deals with the distributed oscillator design and hence represents the focal point of the thesis. The design of two configuration – *single-ended distributed* (DVCO) and *rotary traveling wave oscillators* (RTWO)– is discussed in detail and illustrated with an implementation of two RTWOs on a CMOS 0.13 μm process. The physical properties of the strip-lines are

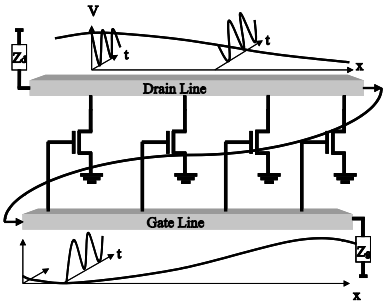


Figure 1.1: Distributed oscillator

discussed. A proposed design method is presented, the design trade-offs are discussed and the measurements are shown.

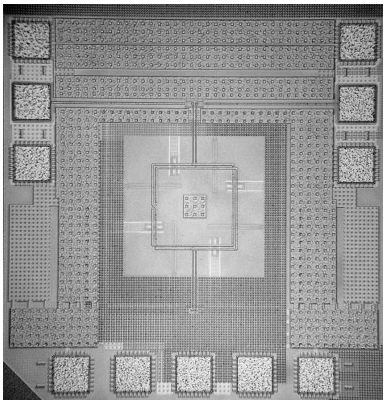


Figure 1.2: Chip Micrograph of the 18GHz RTW-VCO

Chapter 4 gives a brief introduction to the phase noise theory and the models – linear-time-invariant and time-variant – are given. A model for the RTWO oscillator is developed based on the Hajimiri's phase noise theory. An expression for the phase noise of the RTWO in term of power dissipation,

frequency and other parameters is obtained using an approximate analytical model. From the expression some design conclusion are drawn with respect to phase noise improvements.
Chapter 5 discusses the advantages and drawbacks of the RTW-VCO compared to commonly used topologies.
Chapter 6 conclude the thesis listing the achievements and outlooks.

Chapter 2

Distributed amplification

Rotatry traveling wave oscillators are *distributed* circuits, with strip-lines resonators. Hence, their analysis requires the knowledge of the distributed amplification theory. Furthermore, the loaded strip-lines which are the core of the RTWO-resonator and at the same time the device which makes the distributed amplification possible must be correctly described. For these reasons, this chapter gives a description of the distributed amplifier (DA) basic operation, and then discusses the model for the strip-lines. The parameters of the loaded transmission line are introduced.

2.1 Concept of distributed amplification

The distributed concept was invented by W. S. Percival of the United Kingdom in 1936, it has been developed later by Ginzton et al. who, in 1948 [16], for the first time name it "distributed amplification". Since

then, a variety of publications have been written [17]- [20] and it is now a standard amplifier for high bandwidth applications. A reference book was written by Thomas T. Y. Wong [21] from which the following study is based on. A short study of the distributed amplifier is important to understand the operation of the distributed VCOs (DVCO). Indeed, DVCOs draw their advantages over the traditional structures from the principle of distributed amplification.

Conventional amplifier stage have the product gain-bandwidth limited by the properties of active devices used (usually the transconductance and the output capacitance of the transistor). In such standard circuits, expanding the bandwidth is not possible without a degradation of the gain. Moreover, as the gain is made close to unity, cascading amplifier stages becomes inefficient. It also does not help combining amplifier stages in parallel, the gain-bandwidth product will not be improved. The improvement in the distributed amplification is that " the ordinary concept of maximum bandwidth-gain product does not apply". The structure allows a gain-delay trade-off without affecting the bandwidth.

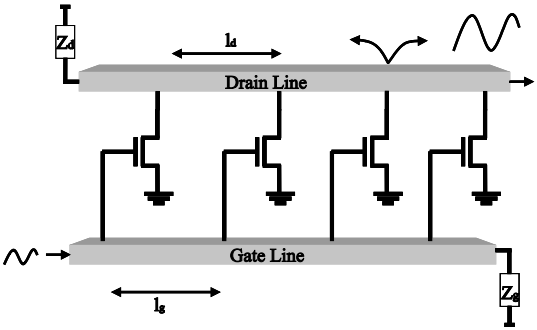


Figure 2.1: Basic Distributed Amplifier

As shown in the figure 2.1 the distributed amplifier is composed of two transmission lines tapped by amplifier stages, transistors in the simplest case, and terminated with their characteristic impedance (Z_g and Z_d). Transistors deliver gains and the gate and drain line play the role of delay line. A voltage step at the input propagates and appears at each gate of transistor with a delay. In order to achieve a constructive amplification along the drain line, the delay between two transistor gates has to be the same as the delay between two successive drains. Gains of each transistors are independent from each other, they contribute one after the other, additively and in phase, to the total gain. It means that ideally even if one transistor has a gain inferior to one, the total gain can be much greater than one depending on the number of transistors used only. The bandwidth of the amplifier is given by the network composed of the transmission line plus the transistor input or output capacitances (C_{gs} for the gate line or C_{ds} for the drain line). Capacitances tapping the line are absorbed in an equivalent transmission line whose bandwidth is determined by the inductance and capacitance of one period of the equivalent lumped transmission line.

2.2 Properties of tapped transmission lines

Before analyzing the actual operation of the distributed amplifier, it is useful to describe the distributed network composed of the transmission line tapped regularly with the gain stages.
An important attribute of the transmission line is its ability to absorb the input/output capacitance of the gain stages. According to the distributed approximation, the tapping capacitance is equivalent to a distributed capacitance along the line. This approximation stays valid as long as the inductive properties of the equivalent transmission line are dominant over the resistive

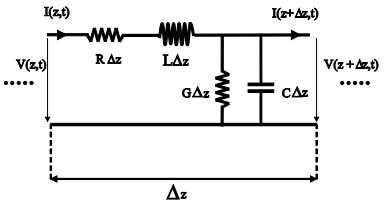


Figure 2.2: Equivalent circuit of a transmission line with length Δz

one ($LC >> RC$). Thus the tapped transmission line has a transmission and loss parameter which differ from the non-tapped case. These parameters are derived in the foregoing discussion.

2.2.1 Transmission Line equations

The transmission line properties are obtainable directly from the widely known solution of the telegrapher equations. In the frequency domain they can be written:

$$\frac{dV(z)}{dz} = -(R + L\omega)I(z) \tag{2.1}$$

$$\frac{dI(z)}{dz} = -(G + C\omega)V(z) \tag{2.2}$$

where R, L, G, and C are per-unit-length circuit parameters for the line. The two equations combined give wave equations for the current and voltage on the line.

$$\frac{d^2V(z)}{dz^2} = \gamma^2 V(z) \tag{2.3}$$

$$\frac{d^2I(z)}{dz^2} = \gamma^2 I(z) \tag{2.4}$$

where $\gamma = \alpha + j\beta = \sqrt{(R + jL\omega)(G + jC\omega)}$ is the propagation constant whose real and imaginary parts, α and β, are the attenuation constant (Np/m) and phase constant (rad/m) of the line. These equations admit traveling-wave solutions of the form

$$V(z) = V_o^+ e^{-\gamma z} + V_o^- e^{\gamma z} \tag{2.5}$$

$$I(z) = \frac{1}{Z_0}(V_o^+ e^{-\gamma z} + V_o^- e^{\gamma z}) \tag{2.6}$$

where

$$Z_0 = \sqrt{\frac{R + j\omega L}{G + j\omega C}} \tag{2.7}$$

is the characteristic impedance of the line and V_0^+ and V_0^- are amplitudes of the forward and backward traveling-waves at initial conditions.
Due to the relatively complicated expressions of the characteristic impedance and propagation constant two cases are often used in practical applications.

- *The Lossless Line* ($R = 0$ and $G = 0$)
  Propagation constant:
  $\alpha = 0$,
  $\beta = \omega\sqrt{LC}$
  Phase velocity
  $v_p = \frac{\omega}{\beta} = \frac{1}{\sqrt{LC}}$
  Characteristic impedance
  $Z_0 = \sqrt{\frac{L}{C}}$

- *The Low-loss Line* ($R << \omega L$ and $G << \omega C$)
  Propagation constant:

$\alpha = \frac{1}{2}(R\sqrt{\frac{C}{L}} + G\sqrt{\frac{L}{C}})$,
$\beta = \omega\sqrt{LC}$
Phase velocity
$v_p = \frac{\omega}{\beta} = \frac{1}{\sqrt{LC}}$
Characteristic impedance
$Z_0 = \sqrt{\frac{L}{C}}$

2.2.2 Tapped transmission line equations

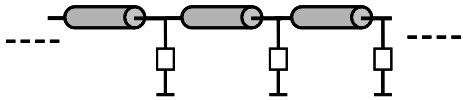


Figure 2.3: Strip-line periodically loaded

Assuming a capacitance C_{TAP} is tapping regularly the strip line with an interval $l[m]$. Making the distributed assumption, meaning the capacitance C_{TAP} is equivalent to a uniformly distributed capacitance distributed over the line, leads to the characteristic impedance:

$$Z_0 = \sqrt{\frac{L}{C + C_{TAP}/l}} \tag{2.8}$$

Assuming the lossless or the low-loss approximation, the propagation constant is redefined:

$$\beta_0 = \sqrt{L(C + C_{TAP}/l)} \tag{2.9}$$

The capacitive loading reduces the characteristic impedance and increases the propagation constant.

2.3 Distributed amplifier with transmission lines

This kind of amplifier is also called *traveling wave amplifier*.

2.3.1 Ideal distributed amplifier (DA)

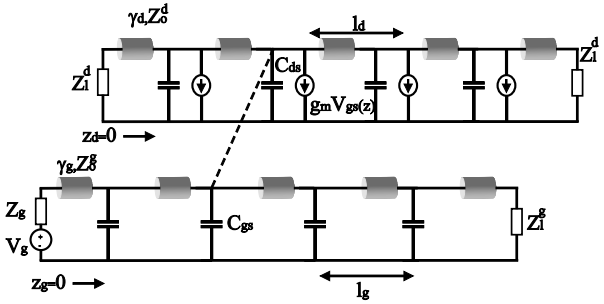


Figure 2.4: Distributed amplifier, the transmission lines periodically loaded with lossless unilateral active devices

In a first description the transistor is modeled simply with an input capacitance C_{gs}, an output capacitance C_{ds}, and a transconductance g_m. The transmission line is uniform, lossless and periodically loaded with lossless active devices. As phase synchronization is necessary to achieve a stable constructive amplification, two different coordinates z_d and z_g are introduced for drain and gate line respectively, see figure 2.4. Geometric distances between successive drains (l_d) and gates (l_g) are not necessary equal, important is just that the electrical length between two taps stays the same. It means for the wave coefficients that $\beta_g l_g = \beta_d l_d$. Assumed is that the coupling between the two lines is only due to the transconductance. The transmission

line is modeled as a distributed network, the propagation constants and the characteristic impedances of the loaded lines are:

$$\gamma_g = j\beta_g \approx j\omega\sqrt{L_g(C_g + \frac{C_{gs}}{l_g})} \tag{2.10}$$

$$\gamma_d = j\beta_d \approx j\omega\sqrt{L_d(C_d + \frac{C_{ds}}{l_d})} \tag{2.11}$$

and

$$Z_o^g \approx \sqrt{\frac{L_g}{C_g + \frac{C_{gs}}{l_g}}} \tag{2.12}$$

$$Z_o^d \approx \sqrt{\frac{L_d}{C_d + \frac{C_{ds}}{l_d}}} \tag{2.13}$$

where L_g, L_d, C_g, C_d are the series inductance and parallel capacitance of the gate and drain transmission line per unit length. Both lines of the DA are terminated by their characteristic impedances. The output voltage across the load on the right-hand side of the drain line is defined as the sum of all the current contributors and is evaluated as follow:

$$V_{out}^r = \frac{Z_o^d}{2}\int_0^{Nl_d} \bar{I}_0(z')e^{-j\beta_d(Nl_d - z')}dz' \tag{2.14}$$

with $\bar{I}_0(z')$ the current source assumed distributed along the line and N the number of transistors used. The phase of the currents are synchronized to the propagating wave along the gate line. The current is defined:

$$\begin{aligned}\bar{I}_0(z') &= -\frac{g_m}{l_d}v_g(z) \\ &= -\frac{g_m}{l_d}e^{-j\beta_g(\frac{l_g}{l_d}z')}\end{aligned} \tag{2.15}$$

where the gain pro length g_m/l_d is introduced. Accordingly the gain of the DA is then obtain after integration (see Appendix A for the development of the calculation):

$$A_v = -\frac{g_m Z_o^d}{2}\left[\frac{e^{-jN\beta_g l_g} - e^{-jN\beta_d l_d}}{j(\beta_d l_d - \beta_g l_g)}\right] \tag{2.16}$$

If the phase synchronization is respected ($\beta_g l_g = \beta_d l_d$), it can be reduced to:

$$A_v = -\frac{N g_m Z_o^d}{2} e^{-jN\beta_g l_g} \tag{2.17}$$

The factor $\frac{1}{2}$ comes from the fact that the energy is considered equally divided into the two possible directions in the drain line (forward or to the right and backward or to the left). According to the expression 2.17, the ideal DA has a gain which varies monotonically with the number of transistor N. Note that a backward wave is propagating whose amplitude is frequency dependent. The integration for the voltage at the left hand side of the drain line gives:

$$V_{out}^l = -\frac{V_{in}^l g_m Z_o^d}{2}\left[\frac{1 - e^{-jN(\beta_d l_d + \beta_g l_g)}}{j(\beta_d l_d + \beta_g l_g)}\right] \tag{2.18}$$

2.3.2 Distributed amplifier with losses

Two kind of losses can be taken into account, losses of the transmission lines and losses of active devices. The device losses are usually predominant and only them will be considered in this analysis. The equivalent schematic is shown in figure 2.5 where the two resistances R_{gs} and R_{ds} of the transistors are included.

This leads to new characteristic impedance and propagation constants which have to be evaluated. The transmission parameter γ is evaluated for the gate

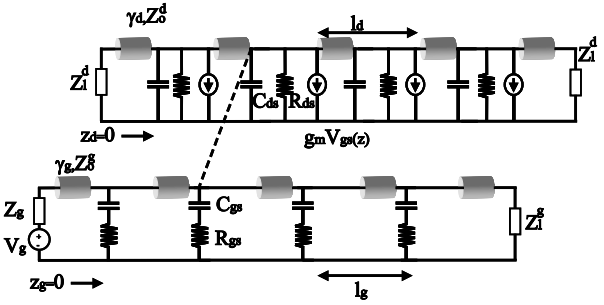


Figure 2.5: Distributed amplifier, the transmission lines periodically loaded with unilateral active devices

and drain line, always assuming the distributed approximation:

$$\begin{aligned}\gamma_g &\approx \sqrt{j\omega L_g\left(\frac{\frac{j\omega C_{gs}}{l_g}}{1+j\omega R_{gs}C_{gs}}+j\omega C_g\right)}\\ &\approx \frac{1}{2}\frac{\omega^2 R_{gs}C_{gs}^2}{l_g}\sqrt{\frac{L_g}{C_g+\frac{C_{gs}}{l_g}}}+j\omega\sqrt{L_g(C_g+\frac{C_{gs}}{l_g})}\\ &= \alpha_g + j\beta_g\end{aligned} \tag{2.19}$$

$$\begin{aligned}\gamma_d &\approx \sqrt{j\omega L_d\left(j\omega\left(C_d+\frac{C_{ds}}{l_d}\right)+\frac{1}{R_{ds}l_d}\right)}\\ &\approx \frac{1}{2}\sqrt{\frac{L_d}{C_d+\frac{C_{ds}}{l_d}}}\frac{1}{R_{ds}l_d}+j\omega\sqrt{L_d\left(C_d+\frac{C_{ds}}{l_d}\right)}\\ &= \alpha_d + j\beta_d\end{aligned} \tag{2.20}$$

In the case of CMOS transistors, the resistance R_{gs} is much smaller than R_{ds}. R_{ds} has little influence on the drain line contrary to R_{gs} which has a linear effect on losses in the drain line, as shown in the previous equation:

$\alpha_g = \frac{1}{2}\frac{\omega^2 R_{gs} C_{gs}^2}{l_g}\sqrt{\frac{L_g}{C_g+\frac{C_{gs}}{l_g}}}$. Moreover α_d has a quadratic frequency dependence, meaning that for high frequency performance the main losses to be considered are in the gate line.
The characteristic impedance is also affected by losses.

$$\begin{aligned} Z_o^g &\approx \sqrt{\frac{L_g}{C_g + \frac{\frac{C_{gs}}{l_g}}{1+j\omega R_{gs} C_{gs}}}} \\ &\approx \sqrt{\frac{L_g}{C_g + \frac{C_{gs}}{l_g}}}\left[1 + j\omega \frac{R_{gs} C_{gs}^2}{l_g\left(C_g + \frac{C_{gs}}{l_g}\right)}\right] \end{aligned} \tag{2.21}$$

The impedance has now an inductive component which makes the calculation of the gain quite complicated. However, in order to evaluate the equations, it is assumed the imaginary part is negligible within the frequency range where the transistor gain remains significant. Only the real characteristic impedance part is considered in the following.
The voltage gain with the lossy propagation constant is given by:

$$A_v \approx -\frac{g_m Z_o^d}{2}\left[\frac{e^{-N\gamma_g l_g} - e^{-N\gamma_d l_d}}{\gamma_d l_d - \gamma_g l_g}\right] \tag{2.22}$$

Even if the phase synchronization is respected, $\gamma_g l_g \neq \gamma_d l_d$ since the expressions of α differ for gate and drain line. With $\gamma = \alpha + j\beta$ the expression can still be simplified to:

$$A_v \approx -\frac{g_m Z_o^d e^{-jN\beta_g l_g}}{2}\left[\frac{e^{-N\alpha_g l_g} - e^{-N\alpha_d l_d}}{\alpha_d l_d - \alpha_g l_g}\right] \tag{2.23}$$

Since distributed amplifiers have their input and output impedance of the same order of magnitude, the power gain is a commonly used parameter for

their performances evaluation.

$$G \approx \frac{g_m^2 Z_o^d Z_o^g}{4} \left| \frac{e^{-N\alpha_g l_g} - e^{-N\alpha_d l_d}}{\alpha_d l_d - \alpha_g l_g} \right|^2 \tag{2.24}$$

Contrary to the previous gain expression it is noticeable that the power gain is, contrary to the lossless case, not any more a linear function of the number of transistors used in the amplification. So an infinite number of transistors would not increase the gain indefinitely. Whereas the low-frequency gain grows up with the number of transistor, the high frequency gain does not. In fact, as the number of transistors gets large, the gain approaches zero in the limit. An optimum can be found for a given frequency.
For practical design issue, Ayasli et al. [17] derived an approximation of the gain with a criteria for optimizing the number of active devices.

$$G \approx \frac{g_m^2 N^2 Z_o^d Z_o^g}{4} \left(1 - \frac{\alpha_g l_g N}{2} + \frac{\alpha_g^2 l_g^2 N^2}{6} \right)^2 \tag{2.25}$$

The factor $\alpha_g l_g N$ has to remain lower than one in order to have a gain with a quadratic dependence on N. Thus at the highest frequency

$$N \leq \frac{2}{R_{gs}\omega^2 C_{gs}^2 Z_o^d} \tag{2.26}$$

This expression gives also the maximum gate periphery that has to be employed in the DA.

2.3.3 Distributed amplifier as a coupled wave system

Physically a DA is composed of two transmission lines coupled by amplifiers. So far a unilateral coupling between the two lines is considered only. However

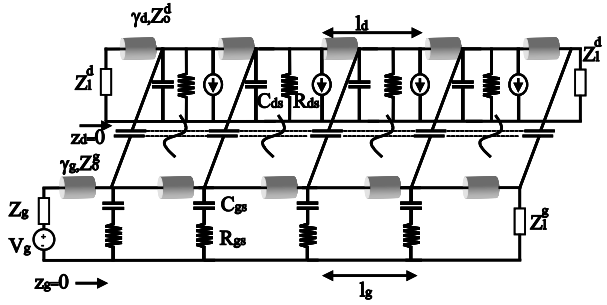


Figure 2.6: Model of a distributed amplifier, where the coupled transmission lines are periodically loaded with bilateral active devices

the electrical analysis of two metal lines with a defined spacing leads to the presence of two propagation modes in each direction. The coexistence of so called even and odd modes (see annexe 2) is the result of bilateral passive and active interactions between the two lines. The analysis of the mutual interactions require the use of numerical methods. The aim of this review is not to develop the heavy calculus but more to have an insight in the consequences this effect has on the circuit. A more detailed analysis will be done for the oscillator case. The figure 2.6 shows an equivalent schematic of a coupled DA. The transverse capacitance is a representation of both, the coupling between the two lines and the inevitable capacitance C_{gd} from the CMOS device.

These interactions have a direct influence on the propagation modes and lead to dispersion for the characteristic impedance and propagation constant. In both lines Z and γ for the two modes are frequency dependent, meaning that a matched load is quasi impossible. The consequences are that the gain will not be as constant as expected over the bandwidth considered.

Chapter 3

Distributed oscillator

This chapter deals with the analysis and design of the distributed CMOS voltage controlled oscillator DVCO. Beginning with a general study of the oscillator, the single-ended DVCO and the rotary traveling wave oscillator (RTWO) are introduced. A design method for the RTWO is presented and two implementations of it are shown. Last, Measurements and evaluation of the performances are detailed.

3.1 Oscillator Theory

An electrical oscillator is a circuit generating a periodically time varying signal with only dc supply. To describe oscillators two representations of the circuit are usually recommended: the two port model or the single port model. A description of these models will be presented.

3.2 Two ports model

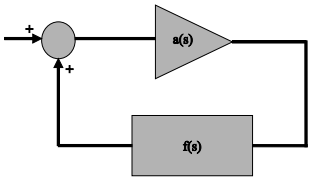


Figure 3.1: Ideal linear feedback model

An oscillator can be thought as an amplifier that provides its own input signal through positive feedback. Then it can be modeled as a linear single two port feedback circuit (see Fig 3.1) with the following overall transfer function:

$$H(s) = \frac{Y(s)}{X(s)} = \frac{a(s)}{1 - a(s)f(s)} \tag{3.1}$$

A self sustaining effect occurs at the frequency s_0 only if at this frequency the loop transfer function is exactly equal to one: $a(s_0)f(s_0) = 1$ so that the closed-loop gain approaches infinity. This is the well known Barkhausen's criteria. When the criteria is met, the loop transfer function has its imaginary part equal to zero meaning that the signal comes back *in phase* to the original signal at the input, and the loop gain is equal at least to one. Intuitively one can expect that if the gain were inferior to one the signal would be damped until zero level. On the other hand if the loop gain is superior to one, then the oscillation would be constantly amplified until the active device limit. In reality the assumption of a linear circuit is not valid. The loop gain magnitude is therefore usually chosen to be greater than one, relying on the non linearities which ensure having an effective amplification such that $|a(s)f(s)|$ becomes equal to one [6] [32].

3.3 One port model (negative resistance)

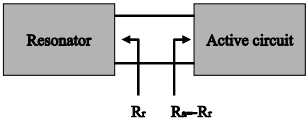


Figure 3.2: One port model of an oscillator

The one port model, Fig 3.2 considers the oscillator as two one port blocks connected together. The first, the resonator, is a simple tank with its own parasitic resistance R_r, the second is an active block generating a negative impedance $-R_r$ so that the equivalent resistance seen by the resonator is infinite. The resonator alone cannot oscillate since a part of the energy stored at every cycle is dissipated in R_r. But with the active device, the energy lost is replenished in every cycle so that stable oscillations occur. This model has the advantage to be simple, but it assumes that the parasitic resistance of the resonator can be converted into a parallel resistance. This approximation is valid in the vicinity of the resonance. In reality, as for the precedent model the negative resistance is often chosen to be much more negative to insure good start-up conditions.

3.4 Distributed amplifier with feedback

The simplest form of distributed resonator is a distributed amplifier for which the output is fed back to its input. It was first introduced as an oscillator by B. Kleveland and al. in 1999 [23] and with a more sophisticated circuitry as a VCO by H. Wu and al. [26].
This is a direct transcription of the two port model. If the amplifier (the open loop of the oscillator) respects Barkhausen's criteria, the closed loop will

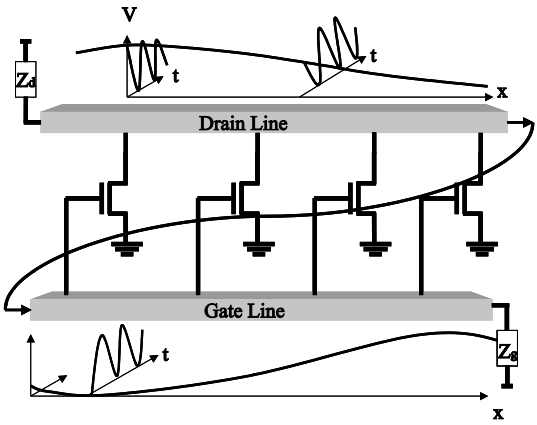


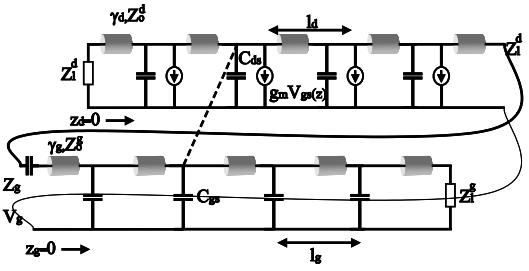
Figure 3.3: Distributed oscillator

oscillate. Another possible representation of it is to consider that the strip line including the transistor capacitors are the tank acting as a filter, allowing only a resonance frequency to pass, and the transistor gains compensate for the tank losses (negative resistance). The frequency is determined by the round trip time delay (from the drain of one transistor to the gate plus inverter time delay) which represents one half period of the clock cycle only since the inverting gain transistor shifts the phase by 180 degrees.

The open loop is a distributed amplifier for which the gain must be at least equal to one in order to allow oscillations. Taking the definition of the DA gain as defined in equation 2.23, one can then write:

$$A_v \approx -\frac{g_m Z_o^d e^{-jN\beta_g l_g}}{2}\left[\frac{e^{-N\alpha_g l_g} - e^{-N\alpha_d l_d}}{\alpha_d l_d - \alpha_g l_g}\right] = 1 \tag{3.2}$$

This equation is valid as long as the output is matched with the impedance of the drain line. If there is a mismatch, and this is the case of the DVCO since the drain line is ac-coupled to the gate line through a capacitor, some



[ht]

Figure 3.4: Schematic modeling the distributed oscillator

reflections occur at the output node. Considering the reflexion factor Γ one can write:

$$\Gamma = \frac{E_r}{E_i} = \frac{Z_i - Z_d}{Z_i + Z_d} \tag{3.3}$$

Where E_r is the reflected wave and E_i the incident wave and Z_i the input impedance seen from the drain line (Z_g with the coupling capacitance in series).

The voltage at the output is thus:

$$V_{out}^r = E_r + E_i = E_i . \frac{2.Z_i}{Z_i + Z_d} \tag{3.4}$$

With E_i expressed in term of V_{out}^r (2.14) the unity open loop gain A_v can be deduced:

$$E_i = -g_m \frac{Z_d}{2} \int_0^{Nl_d} \bar{I}_0(z') e^{-j\beta_d (Nl_d - z')} dz'$$

$$A_v \approx -g_m (Z_o^d // Z_i) e^{-jN\beta_g l_g} \left[\frac{e^{-N\alpha_g l_g} - e^{-N\alpha_d l_d}}{\alpha_d l_d - \alpha_g l_g} \right] = 1 \tag{3.5}$$

This complex equality gives information about amplitude and frequency of oscillations. In the case of similar propagation properties, that means for

drain and gate line : $\alpha_d l_d = \alpha_g l_g$, the equality can be simplified to

$$A_v \approx -N g_m (Z_o^d // Z_i) e^{-jN\beta l} e^{-N\alpha l} = 1 \tag{3.6}$$

Assuming the impedance Z_i is purely real, the imaginary part of the left side of the equation is zero, it means the phase of $e^{-jN\beta l}$ is a multiple of π. Since $\beta = \frac{2\pi.f}{v_{phase}}$ and $v_{phase} = \frac{1}{\sqrt{LC}}$ with L and C the inductance and capacitance per length of the loaded line, l the spacing between two transistors, the oscillation frequency can be expressed as:

$$f_{osc} \approx \frac{v_{phase}}{2Nl} = \frac{1}{2Nl\sqrt{LC}} \tag{3.7}$$

With the cutoff frequency of the loaded line $f_c = \frac{1}{\pi l\sqrt{LC}}$, the oscillation frequency yields:

$$f_{osc} \approx \frac{\pi f_c}{2N} \tag{3.8}$$

Up to the frequency f_c which is also called the bragg frequency, the impedance of the line is imaginary and no signal propagates. Note that for a given frequency of oscillation the cutoff frequency of the resonator can be increased. Indeed, for a given total width and length, increasing the number of stages distributed along the line, meaning decreasing the spacing l between them, increases f_c. For a practical application a limit is set by the smallest physical dimensions of the gain stages.

$$f_c \nearrow = \frac{1}{\pi l \searrow \sqrt{L(C + \frac{C_{gord}\searrow}{l\searrow})}} \tag{3.9}$$

The equation 3.6 gives also information on the amplitude of oscillation. At the oscillation frequency, assuming the voltage in the drain line is large

$(V_d >> (V_{gs} - V_T))$, the transconductance can be expressed as:

$$G_m = \frac{2I_D}{V_D} \tag{3.10}$$

The voltage amplitude of oscillation is thus:

$$V_A \approx \frac{2I_D}{G_m} = 2NI_D(Z_g||Z_i)e^{-\alpha Nl} \tag{3.11}$$

As shown in the expression the amplitude results from the additive contribution of transistors damped by losses in the line (α).

3.5 Rotary Traveling-Wave Oscillator

The rotary Traveling-wave oscillator (RTWO) was first presented by John Wood and al., who realized CMOS test chips for 950 MHz and 3,4 GHz clocks. The principle of the circuit is quite similar to two DVCO cross-coupled each other, it can also be seen as a differential ring oscillator in which the delay is given by the propagation time of the voltage wave in the line. It is also possible to describe it as a selective wave guide where the losses are compensated with active elements (one-port model). First, let's have an insight in the basic functionality of the oscillator.

3.5.1 Concept of the rotary clock oscillator

Oscillations are generated thanks to the Moebius effect, the figure 3.5 illustrates it: the differential line has two stable states, the one polarized positively, the other negatively. We consider the initial state not polarized (0 volt on the two lines).

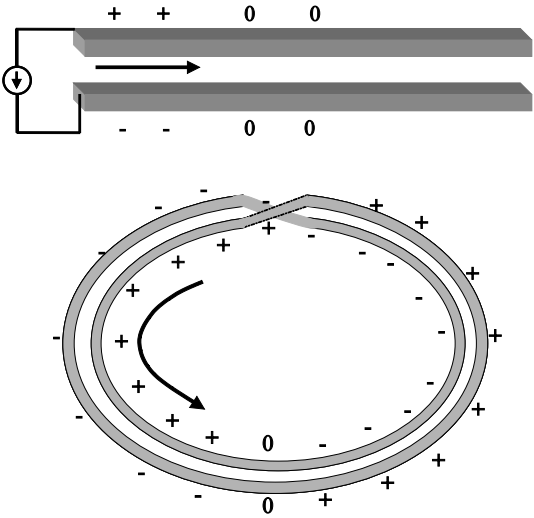


Figure 3.5: Moebus effect

- in the first case an open differential transmission line, with a given delay τ, is connected to a battery through an ideal switch. When the switch is closed, the voltage wave signal travels along the line.

- The second case shows the differential line with a cross-coupled feedback, so that the signal is inverted after one round (delay τ). If the feedback is strong enough to reverse the stable state of the line, then the state effectively switches. So, looking at a given place of the line, oscillation between the two polarized states occurs with a 2τ period.

From a theoretical point of view, there is no reason why the oscillation should prefer to occur in counterclockwise or in the other rotational direction as long as the system stays symmetric. In practical applications, nothing is perfectly symmetrical and it is the direction with the lowest energy losses which is dominant. For real applications the direction of rotation must be

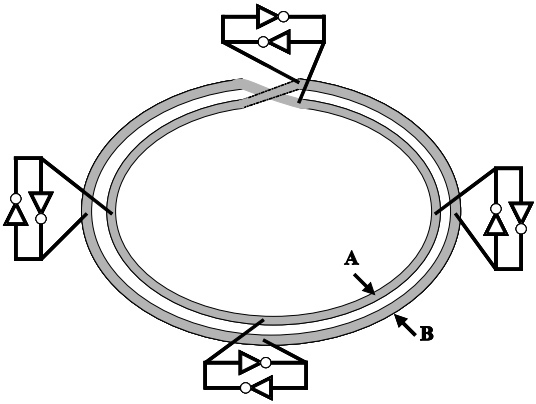


Figure 3.6: RTWO principle

fixed and known.

In electronic's applications, the differential line has two stable states thanks to cross coupled inverters distributed around the ring (fig. 3.6). The cross connected conductor insures the reverse feed-back. Similarly to the single-ended DVCO, the input and output capacitance of the inverters, as long as they are not too large, can be considered as distributed on the line. The oscillation frequency is given by the propagation speed of the voltage wave on the guide composed of the metal line tapped with inverters (distributed network). The time the voltage need to propagate from A to B on the figure 3.6 represents half the period of oscillation. It is interesting to precise that it is the nonlinearity of inverters which is allowing oscillations. Indeed, if inverters were perfectly linear, the feedback reverse signal would just be able to compensate exactly the following polarization, leading to a zero polarized state and annealing any oscillation.

There are several advantages in using such an oscillator compared to the single-ended DVCO or to a standard ring oscillator.

- The architecture is fully differential, the coupled strip lines have a better foreseeable inductance than a single strip line. Indeed the forward and backward path of current is well defined for the strip pair, whereas it is not always well defined for the single strip of a DVCO. Coupled strip lines have less dependency on substrate's capacitance and substrate losses.

- The resonator is fully closed, no problems of impedance termination over the bandwidth of interest occurs. In fact the feed-back imposes the strip-line to pass in another metal layer leading to a slight local mismatch of the impedance. This difference remains however minimal compared to the mismatch generated by the coupling capacitance of a DVCO over the bandwidth considered.

- Once the wave propagates on the medium, the losses from the oscillator are related to the resistive losses within the line only. Indeed, contrary to the ring oscillator, the energy which charges and discharges the MOS gate capacitance is part of the wave energy. This energy is not lost at each stage but recirculates from one stage to another into the closed path. The RTWO is adiabatic since the voltage drop required to charge the capacitances is developed mainly across the inductance, see [25].

For the designer, having a predictable oscillation frequency means that the properties of the differential strip line and of the elements tapping the line have to be precisely defined. The wave velocity propagating on the medium depends on the physical dimensions of the elements used. The properties of the different parts of the circuit will be reviewed.

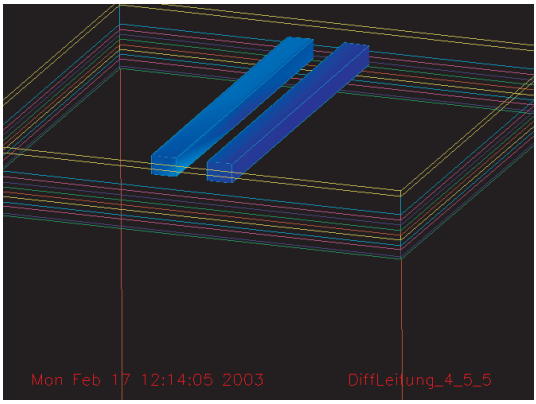


Figure 3.7: Differential line simulated with HFSS

3.5.2 Transmission Line

3.5.2.1 Model

The strip-line needed as wave resonator for the RTWO is a coupled-strip line. On this medium two modes of propagation are available [21] [22] [14], see appendix C. The first mode, the even mode also called the *fast wave mode*, is observed when the two lines are excited with the same signal. As a result the coupling capacitance between the two lines, see $C_f$in Fig 3.8, will have no effect on the propagation constant of this medium. The second mode, the odd mode also called the *slow wave mode*, is obtained as the line pair is excited differentially, so the coupling capacitance between the two lines has a doubled effect on the propagation constant of this mode. The odd mode is of interest for the RTWO, any even mode propagation is a lost of energy which does not contribute to the oscillation and should be excluded. The inverters are theoretically forcing the line to operate differentially but in reality mismatches and noises contributes to an even mode unwanted signal.

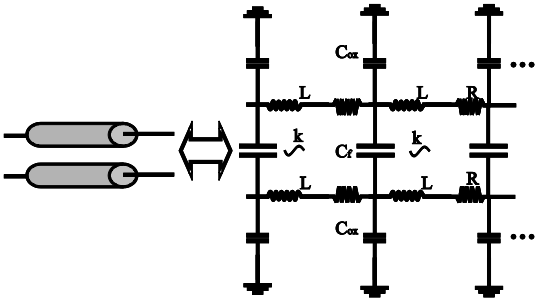


Figure 3.8: Coupled-strip-line model

The model from coupled strip line is presented in the figure 3.8 and contain the two modes, the corresponding propagating wave and impedance parameters are given in the table 3.1 where the losses are not taken into

Mode	Impedance	Propagation Constant
Even	$Z_e \approx \sqrt{\frac{L_e}{C_{ox}}}$	$\gamma_e \approx \pm j\omega\sqrt{L_e C_{ox}}$
Odd	$Z_o \approx \sqrt{\frac{L_o}{C_{ox}+2C_f}}$	$\gamma_o \approx \pm j\omega\sqrt{L_o(C_{ox}+2C_f)}$
	$L_e = L(1+k)$	$L_o = L(1-k)$

Table 3.1: Parameter correspondence for the coupled strip-line equivalent circuit

consideration. The resistive losses are however important at the high frequencies of interest and their effects will be described on the application example.

3.5.2.2 Design

The reversed closed differential line pair is the core of the resonator. The quality of this wave guide resonator influences directly the performances of

the oscillator. To enhance the properties of the RTW-VCO the differential impedance Z_{odd} of the strip line has to be maximized for the following reasons:

1. In order to conserve the adiabatic functionality of the circuit, the transmission line characteristics have to dominate over the RC characteristics. In practice, a criteria is given with :

$$R_{loop} < 2Z_{odd} \tag{3.12}$$

   For a given resistance in the line and in the inverters (parasitics; gate resistance), the dimension of the strip and the spacing between the two lines must be chosen to maximize Z_{odd}.

2. The power consumption which can be expressed:

$$P_{diss} = \frac{V_{odd}^2}{Z_{odd}^2} R_{loop} \tag{3.13}$$

   The impedance Z_{odd} increases with the inductance of the line. Maximizing the inductive storage energy within the line leads to reduce the power dissipation.

3. The third reason concerns the gain on the strip-line. The higher the impedance, the better the gain. As derived in the equation 3.11 the impedance is directly proportional to the gain.

4. The higher the impedance, the better the distributed approximation. A good accuracy of distribution approximation is allowing a better forecast of the oscillation's frequency.

To exploit fully the benefit of a transmission line resonator it results from the previous remarks that the inductance per length L_{pl} of the line must

be maximized. The dimensions of the differential pair should be chosen consequently. The equation for the inductance per length from [28] yields a good approximation, and is expressed:

$$L_{pl} = \frac{\mu_0}{\pi} log\left(\left(\frac{\pi s}{w+t}\right)+1\right) \tag{3.14}$$

where s is the conductor separation, w is the width of the strip, t is the thickness of the strip and μ_0 the permeability in vacuum. For imposed dimensions of the differential pair, the length limits the maximum value of the inductance. According to the equation 3.14, the way to increase the inductance per length of the resonator is to maximize the spacing s, and simultaneously to minimize the width w. The thickness t of the conductor is usually fixed by the process and is not a design variable. A practical limit is reached when the width of the strip becomes too small, resulting in an excessive attenuation due mainly to the skin effect (see Appendix E) which results in a resistance inversely proportional to the surface of the conductor. To avoid losses in the line at high frequencies, large dimensions of conductor are thus preferable. Another limiting factor is set by the electromigration: the current density in the conductor is limited by its physical dimensions and by the temperature. This requirement places another restriction to the dimension of the conductor since they must carry large value of ac current which circulates around the loop.

3.5.3 Gain stages properties

Due to symmetric concern, the inverters tapping the line have to load both lines with the same impedance, so that the properties of the resonator stay uniform along the pathway of the wave. The solution adopted in our case is the same as the one used by John Wood et al. [25]: the four transistor

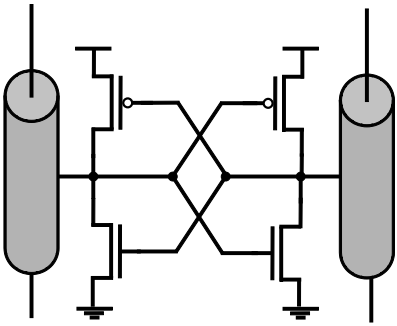


Figure 3.9: Inverter loading the line

switch. The simple complementary latch structure shown fig. 3.9 has the advantage to set the common mode on the differential line without any additive transistor for biasing. Each latch changes its state at the rotating wavefront and there is ideally only one region in the cross-conduction condition at one time. In fact, the transistor does not have enough time to develop completely the latching action. Even if the "clash" of state is not quick enough this implementation maximizes the voltage swing.

Another advantage of this configuration concerns the large loading capacitance for each stage it provides. Since the delay time between two consecutive stages is $l\sqrt{L(C + \frac{C_{in/out}}{l})}$, having a larger loading capacitance $C_{in/out}$ in our case allows reasonable dimension of the length l of the line for a given frequency of oscillation.

3.5.3.1 Sizing

To evaluate the dimensions of the transistors and thus of the negative resistance required to compensate for the losses in the resonator, two approaches are possible. The first uses the standard criteria, the same that is used for the LC standard oscillator (see appendix C) based on the quality factor. A way is described in the appendix B to derive a quality factor for a strip-line resonator loaded with taps. The resulting effective loaded quality factor Q_{loaded} with the loaded impedance Z_{loaded} yield a condition at which oscillations occur:

$$Gm \geq \frac{1}{R_{eq}} = \frac{1}{Q_{loaded} Z_{loaded}} \tag{3.15}$$

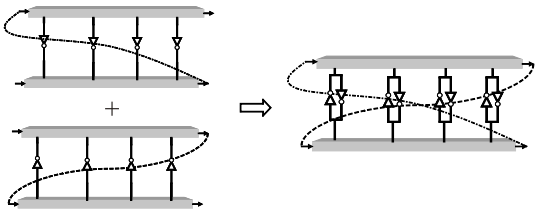


Figure 3.10: Decomposition of the RTWO as two DVCO

The second approach comes from the distributed analysis of the oscillator. The open loop RTWO can be seen as two distributed feedback amplifiers (DA) superposed as shown in figure 3.10. One criteria for a feedback DA to oscillate is a gain G_{m-DVCO} larger than one. With the gain defined as in 2.24 the condition is

$$G_{m-DVCO} \frac{Z_0}{2} \left(1 - \frac{\alpha l n}{2} + \frac{\alpha^2 l^2 n^2}{6}\right) > 1 \tag{3.16}$$

with α the attenuation constant, n the number of tapping elements, l the distance between two taps, and Z_0 the loaded characteristic. This criteria

can be rewritten:

$$G_{m-DVCO} > \frac{2}{Z_0} \frac{1}{1 - \alpha l n/2 + \alpha^2 l^2 n^2/6} \tag{3.17}$$

Assuming the RTWO is made of two DVCOs, the forward as the backward voltage wave contribute to the signal construction contrary to a single DVCO for which the backward wave is lost into the drain matching impedance. 100% of the power is used to establish the propagating wave in the RTWO contrary to 50% for the DVCO. The requirements for the negative resistance of the DVCOs composing the RTWO are then halved. Since the RTWO is composed of two DVCOs, one can conclude that the negative resistance G_m needed for the RTW-VCO is one fourth of the one of the DVCO. So the condition for the RTW-VCO to start is given by the relation:

$$G_{mNR-RTWVCO} > \frac{1}{2Z_0} \frac{1}{1 - \alpha l n/2 + \alpha^2 l^2 n^2/6} \tag{3.18}$$

We will see in the circuit implementation that the second equation 3.18 gives a result narrower to what is simulated. However the first evaluation overvalues only slightly the negative resistance and gives quickly a usable result.

3.5.4 Varactors

Frequency tuning is one of the most important feature of the VCO. The oscillator, when used in a phase-locked system, is controlled by a voltage which adjusts the phase of the clock. It is often preferable to have a larger tuning range as the one required by the system in order to compensate for the process, the unavoidable errors of modeling and the temperature variation. For DVCOs, two techniques are available to offset the frequency. The first

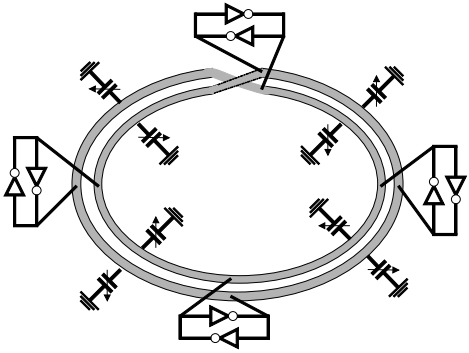


Figure 3.11: RTWO as VCO

is to shorten the line electrically so that the path way will be physically reduced, this solution has been successfully implemented by Hui Wu [26] for its 10 GHz DVCO with his so called *"Delay-balanced Current-Steering Tuning"*. Another solution could be to shorten directly parts of the line with programmable switches. It has however the drawbacks of lowering considerably the quality factor of the line since the switch becomes part of the resonator; the voltage wave has to pass through the switch. The second way to get an appreciable tuning range is to change the properties of the strip-line. The introduction of distributed varactors loading the line affects the phase velocity according to the relation:

$$v_{phase} = \frac{1}{\sqrt{L(C + \frac{C_{var}}{l_v})}} \tag{3.19}$$

where C_{var} is the variable varactor capacitance and l_v the distance between two varactors. The varactors available for the MOS technology are the so called MOS varactors or the pn-diode varactor.

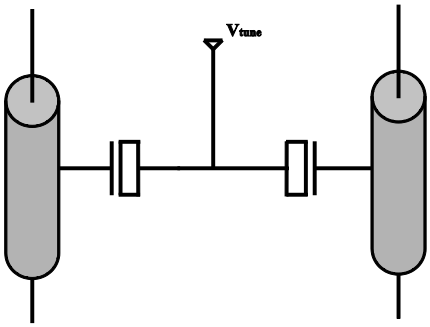


Figure 3.12: NMOS varactor implementation on the RTWO

The MOS varactors, relying on the MOS structure are intrinsically non-linear devices. The varactor is not a four-terminal device but a three-terminal device. The source and drain regions are shorted to apply the voltage V_{tune} which tunes the variable capacitance. The body is usually grounded and the signal, to be loaded with the capacitance, is on the gate. The figure 3.13 depicts the small-signal capacitance of a NMOS varactor with zero tuning voltage. This curve is divided in three regions: the accumulation, the depletion and the inversion. In accumulation, the slope is softer and has a more linear property than for the inversion region. But, the series resistance (substrate resistance) in accumulation is much larger than the resistance in inversion. This means, the quality factor of the MOS varactor is much better, especially for high frequency applications, in inversion than in accumulation. The drawbacks of this configuration can be seen in the figure 2: steep slope and nonlinearity of the curve. The steep slope implies a greater sensitivity to tuning voltage V_{tune} in a short range. This implies more sensitivity to

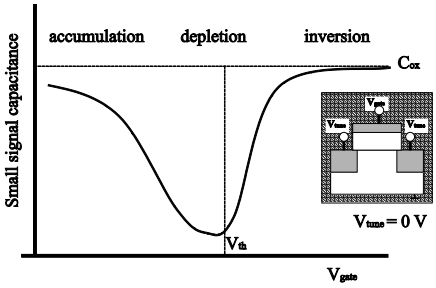


Figure 3.13: Typical measured signal capacitance characteristic of a NMOS varactor

noise on V_{tune} and V_{gate}. The next chapter will show that nonlinear capacitance has adverse effects on phase noise since the output waveform becomes non-symmetrical (up-conversion of low frequency noise). However, the distributed architecture of the RTWO tends to limit some of these drawbacks. The small signal capacitance resulting from the varactors, considered distributed over the whole line, have a softer slope and achieves an inferior maximum capacitance as depicted in the figure 3.14. The slope is inversely proportional to distance between the varactor as long as the distributed approximation is valid. A way to reduce the sensitivity of the VCO to the tuning voltage, K_{vco} [rad/V], would be to increase the distance between varactors, however large distance would be incompatible with the distributed approximation. So a compromise has to be found between the maximum K_{vco} value required and the number of varactors loading the line.

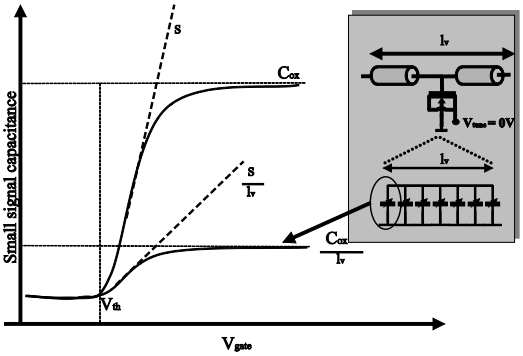


Figure 3.14: Small signal capacitance characteristic of a NMOS varactor and its distributed version

3.6 Realization of RTW-VCO in CMOS

The implementation of two RTW-VCOs are presented in this work. Circuits were realized over a 0.13μm CMOS technology from TSMC. The two circuits generate stable oscillations at 18GHz and 36GHz respectively. The target frequencies were originally 20GHz and 40GHz. The varactor model used did not predict the capacitance correctly, leading to an underestimation of its gate capacitor.

3.6.1 Design trade-offs

We have seen how advantageous it is to maximize the characteristic impedance of the unloaded resonator. Indeed this way the loaded resonator is optimized for power dissipation, and the tapping capacitive elements are better absorbed within the strip-line. To maximize $Z_{unloaded}$ the width of

the strip-line has to be minimized (increasing the inductance per length) and the distance between the two coupled lines must also be maximized (decreasing the fringe capacitance). Technology sets limits for width dimensions (2μm in our case) and in practice the width is not chosen minimal because it would result in a large dc resistance and a dominant skin effect degrading the quality factor of the resonator. Moreover the amount of current flowing in the resonator imposes a minimal width too, dictated by electro-migration rules. The pitch of the pair is determined by the layout and the area available.

The technology available had 8 Cu metal levels with a thick metal on the top. The top metal layer was used to implement the differential strip to minimize the substrate coupling effects and eddy current generation. 2.5D and 3D Simulations (ADS Momemtum and HFSS) gave the even and odd parameters needed for the simulation. After several simulations and layout considerations a coupled line with a pitch of 14μm and a width and thickness of 4μm was chosen for the 20GHz oscillator and a width of 5 μm and a pitch of 20μm for the 40 GHz. The simulator calculates the propagation and characteristic impedance of the even and odd modes. The following tables show the results:

Mode	Impedance	Propagation Constant
Even	$Z_e = 88.48 + j2.7864$	$\gamma_e = 61.308 + j837.288$
Odd	$Z_o = 48.98 - j1.472$	$\gamma_o = 35.37 + j784.45$

Table 3.2: Parameters for 20GHz: w=4μm;t=4μm;pitch=14μm

Mode	Impedance	Propagation Constant
Even	$Z_e = 91.13 + j3.4726$	$\gamma_e = 108.34 + j1666.6$
Odd	$Z_o = 62.942 - j0.18245$	$\gamma_o = 57.71 + j1581$

Table 3.3: Parameters for 40GHz: w=5μm;t=4μm;pitch=17μm

From these parameters the properties of the line per length are deduced and a model like the one shown in figure 3.8 is realized. For the parameter extraction the two equations are used:

$$\gamma Z_0 = R + j\omega L$$
$$\frac{\gamma}{Z_0} = G + j\omega C$$

The sum of gain stages must at least recover the losses in the resonator. The total gain is over dimensioned to ensure good start-up oscillation. To estimate the gain required by the oscillator the criteria 3.18 is used. The problem with this criteria is that the characteristic impedance of the line is dependent on the negative resistance G_{mNR} so that it is difficult to use this equation *a priori*. For the design, graphics were drawn to have a better insight into the influence of the parameter variations. Assuming the gain of a single inverter has been chosen with a corresponding loading capacitance for the line, the figure 3.15 represents the oscillation frequency variations as a function of the spacing between two stages. Once the spacing for the frequency is chosen, (for example a four stages 20GHz oscillator with a spacing of 150μm in the figure 3.15), simulations with spectre are performed to check if the global gain is sufficient to sustain the wave propagation. If it is not the case, five or six stages with the appropriate spacing is then necessary in order to increase the total negative resistance. In practice several optimization steps are necessary to conciliate layout possibilities with a proper operating oscillator. For our design four gain stages with four MOS varactors have been chosen. The figure 3.16 shows variations of frequency versus the capacitance of varactor for different spacing between two consecutive elements. The technology used for the design is a 0.13μm CMOS with deep n-well for NMOS. The process has eight copper metal levels with a standard substrate (resistance estimated $\approx 6\Omega.cm$). The distance to the substrate

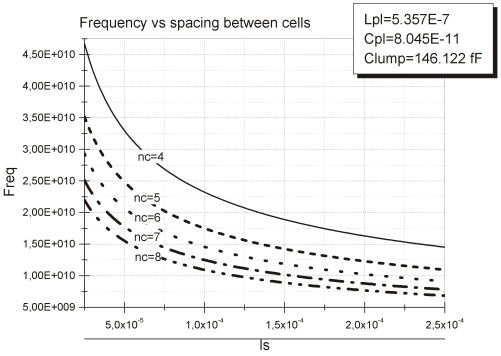


Figure 3.15: Variation of the oscillation frequency versus the spacing between two consecutive tapping gain stages l_s; n_c is the number of gain stages involved

is 6.6μm with a mean dielectric ϵ equal to 3.6. After optimization a total line length of 1.6mm with equally distributed elements was chosen. The odd parameters for the strip-line are:

$$L_{odd} = 305.4nH/m$$
$$C_{odd} = 127.5pF/m$$
$$R_{odd} = 2.88k\Omega/m$$

The gain stage is laid out with multi-finger gates contacted on both sides to reduce source/drain junction capacitance and the intrinsic gate resistance. The dimension of the NMOS are $W = 28\mu m$ with $L = 130nm$. and for the PMOS $W = 72\mu m$ with $L = 130nm$. The resulting loading capacitance from the stage on the line is simulated and its value: $C_{gs} = 391.8fF$. Varactors are also multi-fingered gate transistors with $W = 144\mu m$ and $L = 130nm$ in a deep n-well. With zero volt tuning voltage the small signal capacitance of the varactor is equal to $C_{var} = 285.7fF$. The two outputs are terminated

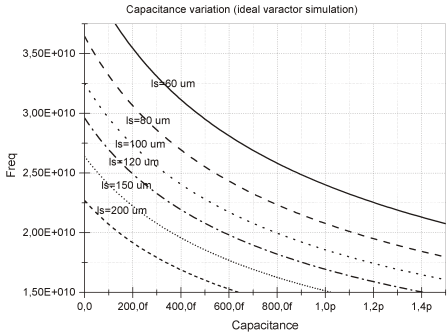


Figure 3.16: Variation of the oscillation frequency in the case of four gain stages versus the value of the tapping varactor for different spacing

with buffers which are complementary inverters with the same dimension as the gain stage. Their loading capacitances influence the resonator, their value are $C_{buf} = 158.9fF$. The loaded impedance Z_0 of the strip line has its value given by:

$$Z_0 = \sqrt{\frac{lL_{line}}{lC_{line} + C_{var} + C_{gs}}} \tag{3.20}$$

where l is the distance between two stages in [m], L_{line} and C_{line} are the inductance per length and the capacitance per length of the unloaded line, C_{var} and C_{gs} are the loading capacitances of the varactor and the gain stage respectively. For the design of the VCO in our case it results in:

$$Z_0 = \sqrt{\frac{2E^{-4} * 305.38E^{-9}}{2E^{-4} * 127.48E^{-12} + 285.7E^{-15} + 391.8E^{-15}}} = 9.32\Omega \tag{3.21}$$

The quality factor of the loaded resonator will be calculated with the definition given by the equation B.28. The expression B.30 has not been taken since the product $f_r = \frac{1}{RC} = 277GHz$ in this example. The equation 3.8

allows us to rewrite it:

$$Q = Q_l \left(1 - \left(\frac{\pi}{2n}\right)^2\right) \tag{3.22}$$

where Q_l is the quality factor of line as defined in B.26, and n is the number of gain stages loading the strip line. So for our example $n = 4$, $Q_l = \frac{\beta}{2\alpha} = 11.08$, it results a loaded quality factor of $Q = 9.3778$. The condition for the negative resistance can be checked and it gives with the condition 3.18:

$$G_{mNR} > 83.35mS \tag{3.23}$$

where $\alpha = 0.2915$(dB/stage) has been evaluated with the expression B.15. The expression 3.15 would have given in this case a minimum value of 115mS which is according to the simulation overvalued. The dimension of the gain stage offers a total negative resistance of 120mS. The criteria is thus respected.

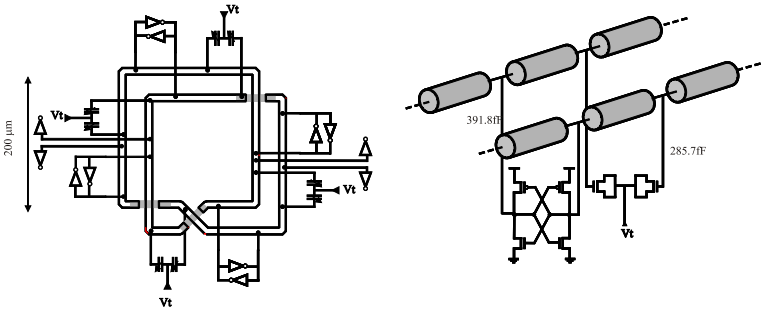


Figure 3.17: Overview of the dimensions for the 18GHz oscillator

The operating frequency is calculated for a zero tuning voltage $V_T = 0V$:

$$f_{osc} = \frac{1}{\sqrt{L_{odd} \times 1.6.10^{-3} \left(C_{odd} \times 1.610^{-3} + C_{gs} \times 8 + C_{var} \times 8 + C_{buf} \times 4\right)}}$$

which results in:

$$f_{osc} = 18.08GHz$$

3.6.2 Layout

The figure 3.18 is the photo of the chip as it has been implemented. Few remarks concerning the layout can be done. Since mistakes can result quickly in an underperforming circuit at these operating frequencies, proper layout is an extremely important design concern. The disposition of elements should minimize the noise, and interconnect parasitic effects. In order to minimize the magnetic coupling between the HF-path and the DC-line, 90 degrees layout techniques is extensively used. It means that DC-lines are orthogonal to the HF-lines as much as possible. The number of stages is even for symmetry concern. However the resonator is not perfectly symmetrical since the cross-coupling imposes to pass at the level metal 7. On-chip decoupling capacitances have been also added as close as possible to the gain stages and the varactors.

3.6.3 Measurements

Measurements were performed on wafer with DC and HF-probes. The measured power spectrum is presented figure 3.19. The measurement equipment from probes to spectrum analyzer generates a 12 dB insertion loss. The oscillator was functional down to 0.8V supply voltage, although 1.1V was required to generate start-up. The total current consumption is 20mA and 14.4mA without buffers contribution. The figure 3.20 presents the tuning range and the gain K_{vco} or sensitivity (f/V) of the RTW-VCO. A tuning

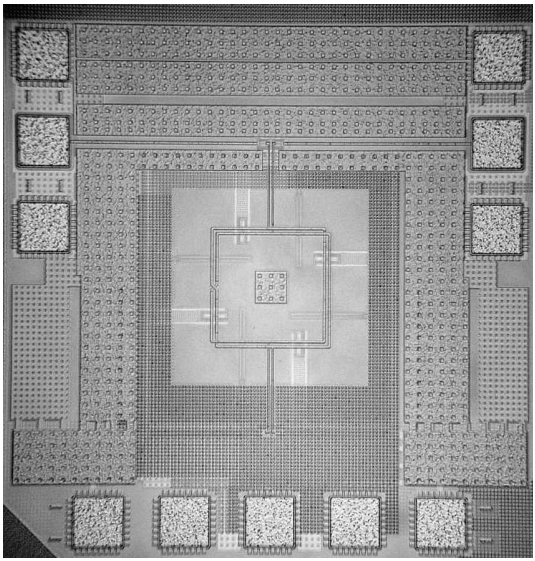


Figure 3.18: Chip Micrograph of the 18GHz RTW-VCO

range of 1 GHz is approximately achieved, this is a 5.6% variation of the voltage frequency. Although it seems to be a poor tuneability, the gain of the VCO achieves 2 GHz/V with a non-linear characteristic. This is a common property for oscillators in the GHz range with low power supply level. It raises two issues, first the achieved tuneability is still too weak compared to the 20% wanted to compensate for process variations, second the sensitivity is too high, consequently the noise at the tuning voltage of the oscillator will result in a worser frequency modulation of the carrier and thus in phase noise. To alleviate these problems, a discrete tuning concept comparable with the LC VCO tuned with switched capacitances schould be considered.

The phase noise of the oscillator was measured from a spectrum analyzer.

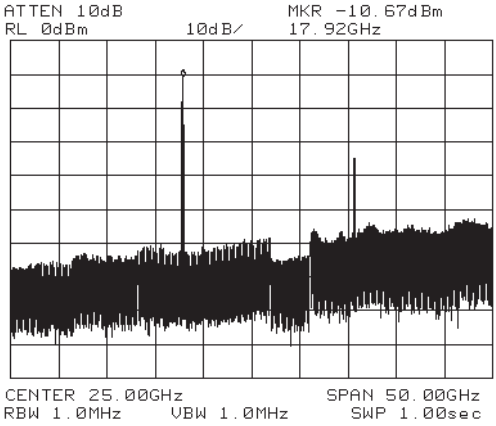


Figure 3.19: Output power Spectrum

Results are visible on the figure 3.21, for 1MHz offset from the carrier at 17.99GHz the phase noise measured is equal to L{1MHz}=-117dB/Hz. More details about the phase noise characteristic of the oscillator will be presented in the next chapter. To be able to compare the performance of the VCO with others, a figure of merit (FOM) is commonly used [7] and defined as:

$$FOM = 10log\left(\left(\frac{f_o}{\Delta f}\right)^2 \frac{1}{L\{\Delta f\}P}\right) \tag{3.24}$$

With P the power consumption expressed in [mW]. The figure of merit is thus: **FOM**=-189dB/Hz. In table 3.4 the performance of comparable VCOs is listed. The 17GHz is a standard LC-tank and the 10GHz is a single-ended DVCO. Variations in voltage supply result in variation of the frequency. Pushing or supply loading quantifies the sensitivity of the output frequency to changes in the power supply and is expressed in [Hz/V]. The figure 3.22 presents the variation of the oscillations for different tuning voltages versus

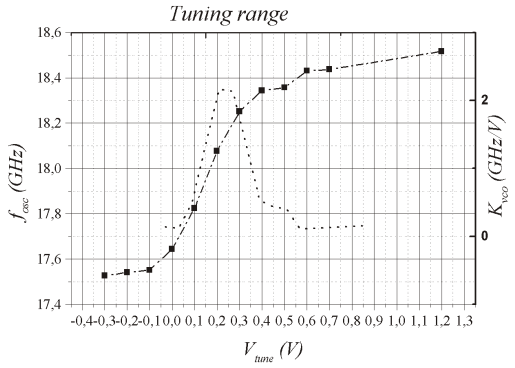


Figure 3.20: Tuning Range and K_{vco} curve

VCO	Frequency GHz	Power mW	Phase Noise dBc/Hz	FOM dBc/Hz
[30]	10	10.5	-108	-182
[26]	17	9	-84	-159
RTWO	18	14.4	-117	-189

Table 3.4: Comparison of FOM and phase noise at 1 MHz offset from the carrier of recently published CMOS integrated VCO

V_{dd}, the worse case for $V_{Tune} = 0.2V$ has a pushing of $\approx 1.5GHz/V$. Figures 3.23and 3.24 show the temperature variation of the oscillation frequency and of the amplitude respectively. Inductance variation is assumed to be negligible compared to the capacitance variation and is consequently not considered. The decrease in threshold voltage with increased temperature results in an earlier inversion for varactors, which means the mean capacitance of varactors rises. This results in a decreasing frequency as shown fig 3.23. As the temperature rises, the resistance of the resonator rises and the gain of stages slightly decrease. The negative resistance required to sustain stable oscillations rises whereas the one gain stages can deliver decreases

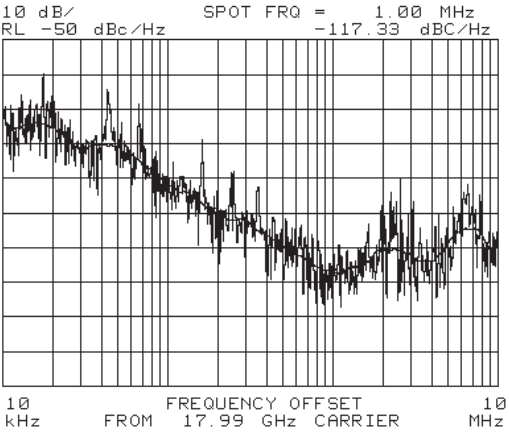


Figure 3.21: Phase Noise from a 17.99 GHz carrier (worst case $V_{tune} = 0,3$)

with temperature. This leads as in figure 3.24 to an amplitude loss.

3.6.4 36GHz RTW-VCO

A 36GHz RTWO-VCO has been designed the same way as the 18GHz. The resonator could not have the same properties per length as for the 18GHz oscillator otherwise the layout would not have been practically realizable (wavelength too short). The pitch of the coupled line changed to be 20μm and the width 5μm. The odd parameters for the strip-line pair are:

$$L_{odd} = 395.9nH/m$$
$$C_{odd} = 99.95pF/m$$
$$R_{odd} = 3.92k\Omega/m$$

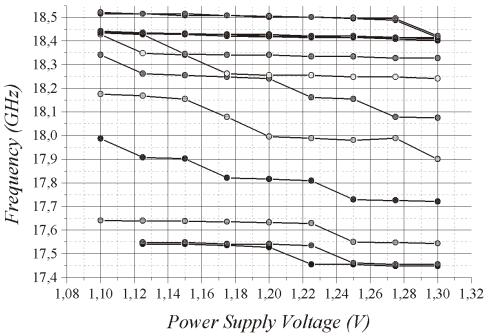


Figure 3.22: Pushing

Dimensions of gain stages differ: for the NMOS W=16μm with L=130nm, for the PMOS W=36μm with L=130nm, and for the varactor (NMOS) W=36μm with L=130nm. The capacitances loading the line are from output buffer $C_{buff} = 142.8fF$, from varactor $C_{var} = 71.43fF$, and from gain stage $C_{gs} = 191.7fF$. The total length of the resonator is $L = 768\mu m$. The frequency of oscillation is thus estimated to be $f_{osc} = 36.5GHz$ which is conform with measurements

The layout has half the dimension of the 18GHz VCO. It was laid out the same way as for the 18GHz and same remarks are valid. The Die size of $755\mu m$ by $710\mu m$ is dominated by the pads. Measurements were performed with the spectrum analyzer HP8562E. No microwave amplifier were used to compensate for the losses of probes and cables which are evaluated to be more than 6 dB at 36 GHz. . The measured spectrum from one end of the differential output is shown Fig. 3.26. The current consumption of the core at 1.2 V is 7 mA. The tuning range (Fig. 3.27) is about 1 GHz with a 1.2

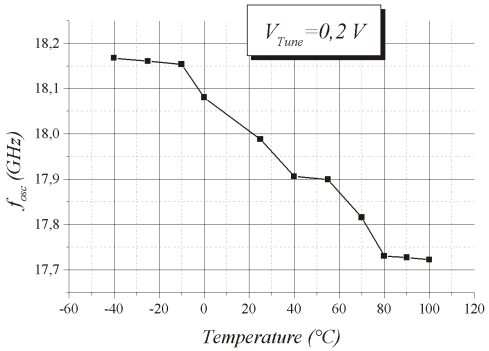


Figure 3.23: Frequency variation with temperature

V variation in tuning voltage, the output power, due to the structure, stay constant over the tuning range. The single side band phase noise presented in Fig. 3.28 is 87 dBc/Hz at 600 kHz offset from the carrier.

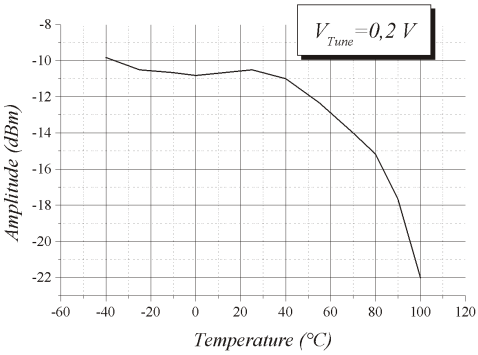


Figure 3.24: Output power variation with temperature

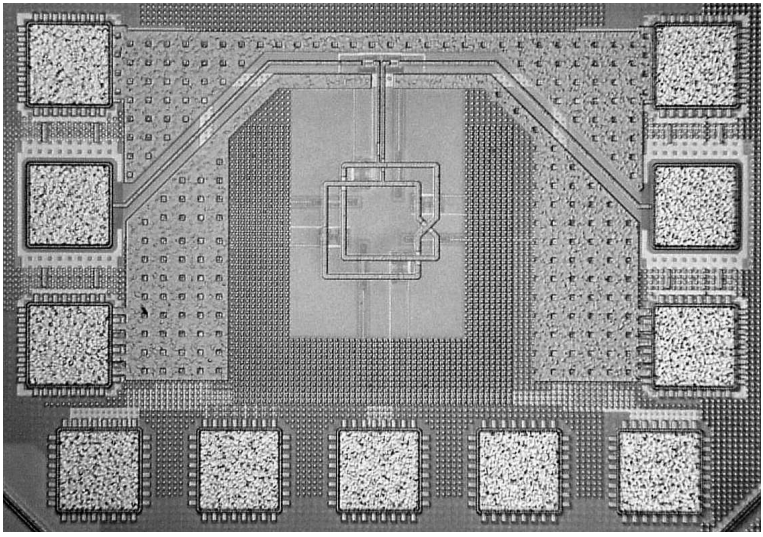


Figure 3.25: Chip Micrograph of the 36GHz RTW-VCO

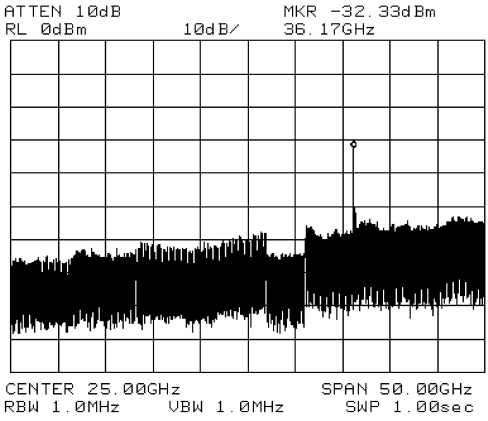


Figure 3.26: Output power Spectrum

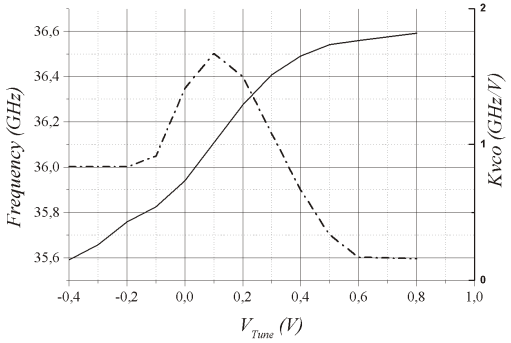


Figure 3.27: Tuning Range and K_{vco} curve

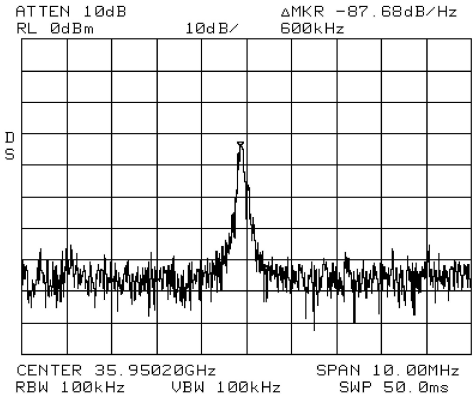


Figure 3.28: Phase Noise from a 36 GHz carrier (worst case $V_{tune} = 0, 3$)

Chapter 4

Phase Noise in Distributed VCOs

4.1 Introduction

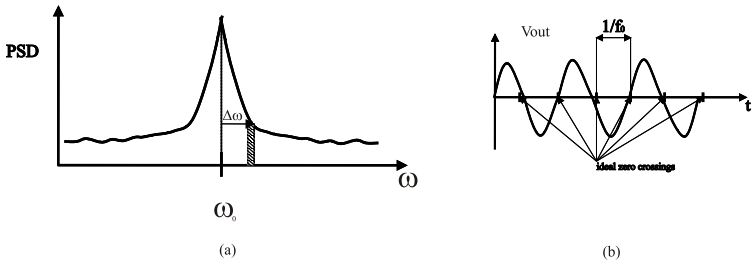


Figure 4.1: (a)Spectrum of a real oscillator with noise side bands and wide band noise floor;(b) Signal zero crossing are not equally space due to phase noise

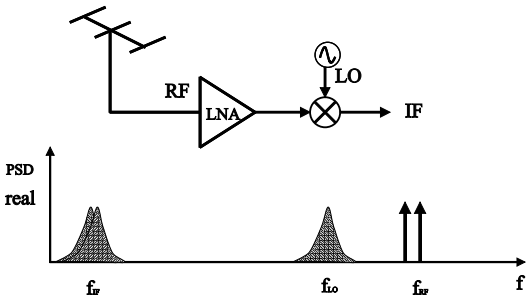


Figure 4.2: Effect of phase noise for two adjacent channels

Oscillators are autonomous systems producing relatively high level of noise at the frequencies closed to the frequency of oscillation. The spectral purity is a key performance measure of a VCO together with the power consumption. Noise sources (thermal, 1/f, supply or substrate interference) cause instabilities in the amplitude and frequency of oscillation. The output spectrum of the oscillator is not a pure tone but has noise sidebands (Fig 4.1:(a)) which means for the time domain that there is an amplitude variation and that the zero crossings of the output signal are not equally spaced in time(Fig 4.1:(c)). Zero crossings exhibit a random variation around a reference fixed value, this variation is referred as jitter. Because the noise is close to the oscillation frequency, it can not be removed by filtering.

An example is given to understand the negative effect of phase noise. Consider the simplified radio receiver figure 4.2. The aim of the circuit is convert the RF signal detected by the antenna and amplified by the LNA into an IF (intermediate frequency) signal. The mixer does the conversion. As shown in the figure if a signal in an adjacent channel with the same power is present, the phase noise of the LO will modulate both signals at the IF frequency so that interferences between them will occur. The signal-to-noise ratio (SNR) is then deteriorated. This phenomenon often referred to as *reciprocal mixing*

determines how close two channel can be. A better phase noise allows the use of more closed channels and then bandwidth frequency reduction.

4.2 Phase noise description

4.2.1 Phase Noise definition

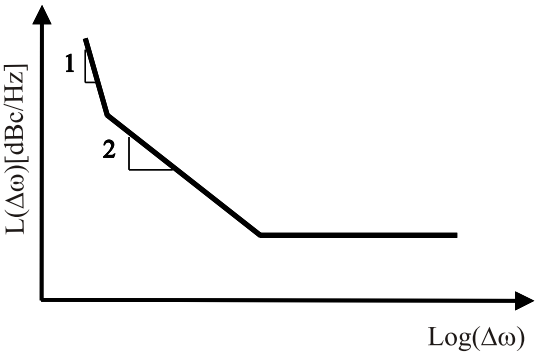


Figure 4.3: Typical plot of phase noise side band as a function of frequency offset from the carrier

Since for an oscillator we are usually interested in the noise around the first harmonic, phase noise is characterized by the single sideband noise spectral density (in dB/Hz) defined as:

$$\mathbf{L}(\Delta\omega) = 10.log\left\{\frac{P_{sideband}(\omega_0 + \Delta\omega, 1Hz)}{P_s}\right\} \tag{4.1}$$

where $P_{sideband}(\omega_0 + \Delta\omega, 1Hz)$ represents the signal sideband power at a frequency offset of $\Delta\omega$ from the carrier with a measurement bandwidth of 1 Hz, and P_s represents the total signal power. $P_{sideband}(\omega_0 + \Delta\omega, 1Hz)$ is also the PSD around the first harmonic for the frequency $f = f_0 + f_m$.

In fact in this form $\mathbf{L}(\Delta\omega)$ depends on the effect of phase and amplitude variations. For oscillators amplitude variations are eliminated by passing the output signal in a buffer which play the role of a limiting stage so that the measured single sideband noise is mainly due to phase variations. Thus, since the effect of phase variations are the main contributor to the measured single sideband noise (SSB), the SSB is referred as phase noise. The figure 4.3 gives a typical example of phase noise curve versus the frequency offset from the carrier. Three regions are visible: the flat region representing the noise floor, the region with the slope 2 where white noise sources gives rise to a $\Delta\omega^2$ dependence of the phase noise power on frequency offset, and the region 3 where the effect of the 1/f noise adds to white noise to give rise to a $\Delta\omega^3$ dependence.

4.2.2 LTI approach: Leeson's model

These models are based on the Linear Time Invariant (LTI) system assumption. The most known model for phase noise description is the one Leeson proposed in 1966 [3] which was further expanded [4]. The model predicts a behavior given by:

$$L\{\Delta\omega\} = 10.log\left(\frac{2FkT}{P_s}\left[1+\left(\frac{\omega_0}{2Q_L\Delta\omega}\right)^2\right]\left(1+\frac{\omega_{1/f^3}}{|\Delta\omega|}\right)\right) \tag{4.2}$$

where F is an empirical parameter often called device excess noise factor, k is the Boltzmann's constant, T is the absolute temperature, P_s is the signal power, ω_0 is the oscillation frequency, Q_L is the quality factor of the loaded tank, $\Delta\omega$ is the offset from the carrier, and ω_{1/f^3} is the frequency corner which locates the transition between the $1/f^2$ and the $1/f^3$ region.
With this model of phase noise, it is quite clear that the $1/f^2$ region depends

on the quality factor of the resonator on one hand and on the amplitude on the other hand. The figure 4.4 presents the influence of parameter variations on the output spectrum (power spectral density) with the present LTI approach. The oscillator is presented as a RLC filter amplifying the white noise composed of the thermal noise sources from active devices and resistance of the tank. The factor kT represents the effective resistance of the tank and the factor F is a multiplicative factor accounting for the shot noise of active devices. With increasing Q the pass band is narrower and the noise around the frequency f_0 is more effectively damped. This results in a better signal to noise ratio, thus in an improved phase noise. Another way to improve the signal to noise ratio is to decrease the white noise floor (2FkT) or to increase the signal power (P).

Except the factor F which can often only be determined *a posteriori*, the equation for the $1/f^2$ region is quite conform to the intuition we could have. It is however more difficult to give a LTI explanation for the up-conversion of $1/f$ noise into the spectrum of oscillation since it results from a nonlinear process. The 1/f noise is based on surface effects inside the transistor, it is an increasing worry for the MOS transistors since new processes tends to have transistors with 1/f corner well above 1 MHz [33] [34].

Resulting from a linear analysis this expression provides a partial understanding of the physical processes generating the phase noise. Nevertheless the Leeson's formula is a good empirical formula. It gives some informations for the optimization of the phase noise performances. Accordingly, an increase of the quality factor results in a reduction of the phase noise. A way to optimize the VCO is thus to increase the quality factor. Unfortunately it is almost a fixed property of the technology used. Another way is to increase the signal power by maximizing the output swing. Indeed, according to the formula the phase noise in dB is inversely proportional to the output amplitude. The Leeson's formula is however unable to give estimations *a priori*

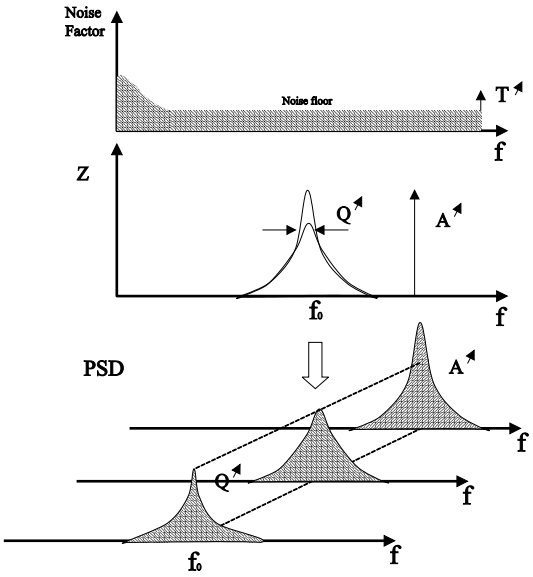


Figure 4.4: LTI view of the white noise amplification of an oscillator: the signal to noise ratio is improved either from a quality factor increase (Q) or from an higher amplitude signal (A)

since the parameters F and ω_{1/f^3} can only be given after having taken measurements. The designer, ideally, would need a model which can account for the changes of phase noise according to the parameters of the circuit.

4.2.3 LTV approach: Hajimiri's approach

The Hajimiri theory takes the time-varying nature of the oscillator into account. The model is constructed above the observation that oscillators exhibit periodic cycles of sensitivity to noise. Consider the example of the LC oscillator figure 4.5. The same perturbation $\delta(t-\tau)$ at two different times

of the same period has not the same effect on the phase. For a perturbation when the voltage in the resonator is maximum the amplitude of the signal changes but not the phase, whereas, in contrast, if the perturbation occurs at the zero crossing voltage the phase change is maximum. The sensitivity

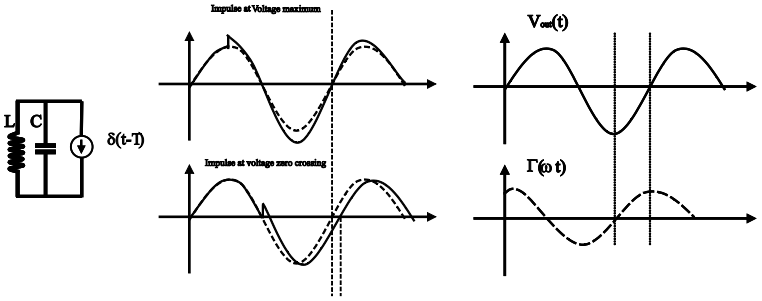


Figure 4.5: Oscillator impulse sensitivity

of the oscillator over the time is periodic and called ISF (impulse sensitivity function) and noted $\Gamma(\omega_0 t)$, where ω_0 is the oscillation frequency of the oscillator. The ISF is dimensionless, frequency- and amplitude-independent 2π-periodic. It can be proved, as intuitively guessed, that the ISF of a pure sinusoidal signal will be also sinusoidal with 90 degrees phase lag. The periodic phase sensitivity in terms of linear time-varying phase impulse response is thus expressed as Hajimiri described it in [31]:

$$h_\phi(t,\tau) = \frac{\Gamma(\omega_0 t)}{q_{max}} u(t-\tau) \tag{4.3}$$

where q_{max} is the maximum charge stored in the resonator and $u(t)$ is the unit step. It has been shown [31] that the phase noise of an oscillator is proportional to the rms value of the ISF function. More precisely:

$$L\{\Delta\omega\} = 10log\left(\frac{\Gamma_{rms}^2}{q_{max}^2}\frac{\bar{i_n^2}/\Delta f}{2\Delta\omega^2}\right) \tag{4.4}$$

The great advantage of this result is the absence of fitting parameter. A measure of the ISF function coupled with the exact knowledge of all the noise sources (intrinsic devices noise and external noise sources) allow us theoretically to have a perfect prediction of the phase noise. Although it seems to be a great advantage over the Leeson's formula, the model has actually transfered the difficulty to another level: the determination of the ISF. To give an analytical form of the ISF is not an easy task and several approximations have to be done in order to calculate it. Hajimiri has proposed in his book [31] a way to predict the value of the ISF for a ring oscillator and argued that for an LC-tank oscillator the $\Gamma_{rms} = 1/2$ which is valid under some simplifications only.
Nevertheless the ISF can always be measured, this is a very convenient function. Comparing two ISF of two different circuits gives a good scale to determine which of it is the lowest sensitive oscillator *a posteriori*. However it gives us little informations about how to improve the ISF at the circuit level. The only way to gain visibility on parameter influence over the phase noise would be to get an analytical expression of the ISF. This is what is proposed in this work: to calculate the ISF of the RTW-VCO in order to find ways of phase noise improvement.

4.2.3.1 Simulations

Before starting to calculate the ISF, it is instructive to see the simulation of the ISF for an RTW-VCO structure. In this case, for the simulation, the oscillator is composed of the strip-line resonator loaded with the same total amount of G_m but more or less distributed along the resonator. It means for the NMOS transistor with a width W_n that $W_T = n.W_n$ with W_T the total width and n the number of NMOS involved. Results in figure

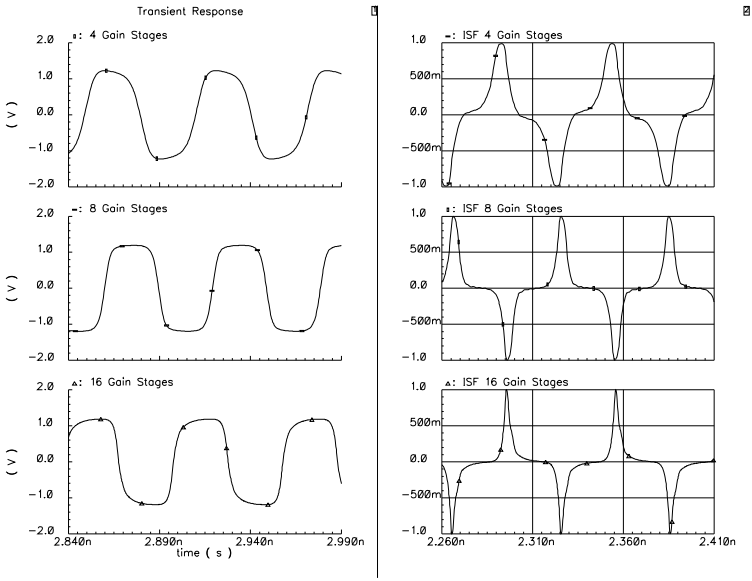


Figure 4.6: Oscillator impulse sensitivity

4.6 show the tendency for the ISF. The simulation makes it clear that for the most distributed network (16 gain stages for the example) the best ISF function; the one with the lowest rms value, is achieved. This is explained owing to the fact that having a more distributed loaded resonator results in a higher cutoff frequency of the distributed network and thus a steeper slope for the edges of the oscillating signal. The zero-crossing range being the most sensitive to noise for phase perturbation, the faster the transition between the two states (the steeper the slope), the most insensitive

Number of Gain Stages	Γ_{rms}
4	$482, 69.10^{-3}$
8	$391, 10.10^{-3}$
16	$287, 5.10^{-3}$

Table 4.1: Comparison of the Γ_{rms} for different gain stage distributions.

to noise is the resonator. The rms values of the ISF are presented in table 4.1.

The corresponding phase noise simulations with cadence spectre are shown figure 4.7. Doubling the number of states meaning approximately doubling the cutoff frequency of the loaded resonator results in a simulated improvement of 3dB/Hz in the thermal noise area ($1/f^2$). Simulations enable us to conclude that the most distributed the circuit is, the better the phase noise. The goal of our study is now to express an analytical function of the phase noise. This expression, to be useful for the designer, must contain the parameters of the circuit. It must also be in agreement with simulations carried out. To start with, a simplified expression of the ISF will be defined.

4.3 Analytical form of the ISF

To determine the ISF, it is necessary to know the shape of the signal in the resonator very precisely. Indeed in the general theory of phase noise in electrical oscillator [37], A. Hajimiri and T. Lee give us a way to find a closed-form formula for the ISF derivate from the waveform f of the signal. Assuming the oscillator is a second order system, the ISF is defined as:

$$\Gamma(x) = \frac{f^{'}}{f^{'2} + f^{''2}} \tag{4.5}$$

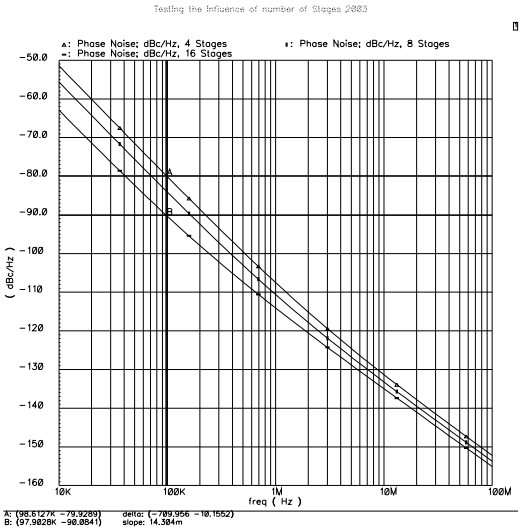


Figure 4.7: Phase noise simulation with Spectre for the three increasingly distributed resonators

For the specific example of the ring oscillator with N identical stages the expression can be approximated with:

$$\Gamma_i(x) = \frac{f_i^{'}(x)}{f_{max}^{'2}} \tag{4.6}$$

Ideally a RTW-VCO without any losses and with ideal inverter gain stages would generate square wave output. A 2π-periodic square wave can be expressed as a Fourier function.

$$f(x) = \frac{2}{\pi} \sum_{p=1}^{p=n} \frac{1}{(2p+1)} sin((2p+1)x) \tag{4.7}$$

where $n \rightarrow \infty$ for an ideal square wave. However the gain stages as well as the resonator are not ideal and the cut-off frequency of the resonator has a finite value. This leads to a finite value of n. Figures 4.8 shows in a 3D representation the evolution of a square wave signal as the number of harmonics increases. The respective ISF is also shown in 3D. Two 2D schematics of the ISF for n=1 and n=20 are presented for improved visibility too. Assuming the output signal of the oscillator only contains odd harmonics, the ISF and its rms value can be expressed analytically. To neglect the even harmonics signifies that the effect of 1/f noise up-conversion are simply ignored. Initially only the stationary noise sources will be considered, what means that only sources of noise whose statistical properties do not depend on time or operating point (thermal noise) are taken into account.

From the graphic one can remark that, like in the simulation, the rms value of $\Gamma(x)$ decreases with an increasing value of n. Let's calculate the rms value

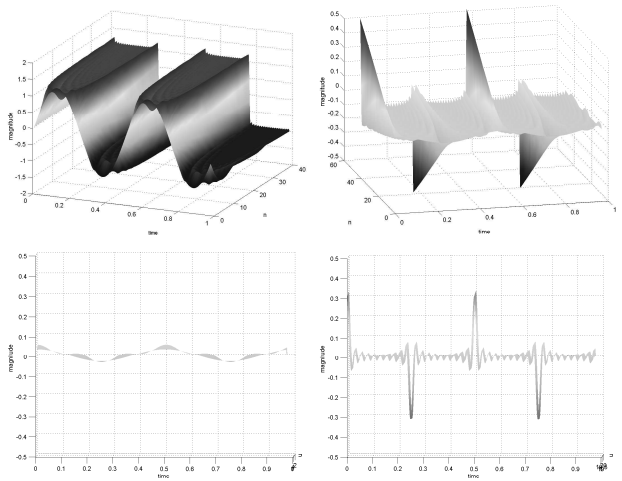


Figure 4.8: Fourier decomposition of a square wave signal and its respective ISF

of the ISF with n as variable. The rms is defined as:

$$\Gamma_{rms}^2 = \frac{1}{2\pi}\int_0^{2\pi} \Gamma^2(x)dx \tag{4.8}$$

For the simplified expression of the ideal symmetrical case $\Gamma(x)$ can be expressed:

$$\Gamma(x) = \frac{\frac{2}{\pi}\sum_{p=0}^{p=n} cos((2p+1)x)}{(\frac{2}{\pi}\sum_{p=0}^{p=n})^2} \tag{4.9}$$

Which gives for the rms value since:

$$\frac{1}{2\pi}\int_0^{2\pi}\left(\sum_{p=0}^{p=n} cos((2p+1)x)\right)^2 dx = \frac{n+1}{2}$$

$$\Gamma_{rms}^2 = \frac{\pi^2}{8}\frac{1}{(n+1)^3} \tag{4.10}$$

Γ_{rms} is proportional to $1/(n+1)^{3/2}$. n is the number of harmonics present in the signal. For the case of the RTW-VCO the resonator has a cut-off frequency f_c which gives the highest harmonic possible in the resonator. Therefore f_c and n are correlated. Indeed, the number of harmonics is directly related to f_c since the following equation must be respected:

$$(2n+1)f_{osc} < f_c$$

For the distributed oscillator structure we saw that $2Nf_{osc} = \pi f_c$ with N the number of stages loading the line. It results the following condition for the number n:

$$n < \frac{2N/\pi - 1}{2}$$

$$n = E\left(\frac{N}{\pi} - \frac{1}{2}\right) \tag{4.11}$$

with E the integer part function. The equation 4.11 makes clear that increasing the number of distributed stages increases the number of harmonics and consequently diminishes the rms value of the ISF.

4.3.1 Analytical Expression of Phase Noise for the RTW-VCO

The expression is derived assuming the sources of white noise are dominant. 1/f noise is neglected in this part. Once the ISF function is defined, a contribution of all noise sources should be described. Figure 4.9 depicts the noise sources in one gain stage. The total differential noise power due to the

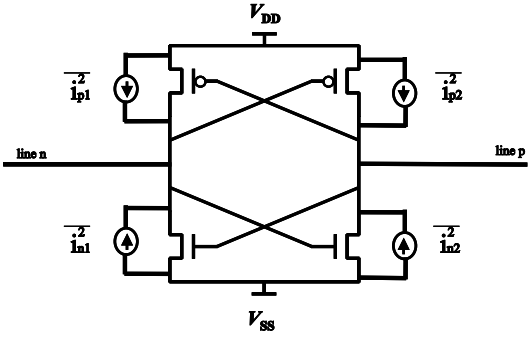


Figure 4.9: Noise sources in the complementary gain stage

four cross coupled transistors is [31]:

$$\bar{i_t^2} = \frac{1}{4}(\bar{i_{n1}^2} + \bar{i_{n2}^2} + \bar{i_{p1}^2} + \bar{i_{p2}^2}) = \frac{1}{2}(\bar{i_n^2} + \bar{i_p^2}) \tag{4.12}$$

where $\bar{i_n^2} = \bar{i_{n1}^2} = \bar{i_{n2}^2}$ and $\bar{i_p^2} = \bar{i_{p1}^2} = \bar{i_{p2}^2}$. The noise densities are given by:

$$\frac{\bar{i_n^2}}{\Delta f} = 4kT\gamma\mu C_{ox}\frac{W}{L}(V_{GS} - V_{Th}) \tag{4.13}$$

where μ is the mobility of the carrier in the channel, C_{ox} the oxide capacitance per unit area, W and L the width and length of the MOS transistor, $(V_{GS} - V_{Th})$ is the overdrive voltage. γ is a factor which can have a value between 2 and 3 for short channel devices [38].

Assuming the thermal noise sources of the different gain stages are uncorrelated and making the assumption the ISF function is the same at each nodes of the resonator except a phase shift lead or lag, the total phase noise is the sum of phase noise contribution of each gain stage. Each of the N gain stages is noisy and generates thermal noise. The maximum charge swing in the case of the RTW-VCO is the product of the equivalent capacitance

between two stages time the voltage swing. Calling the total capacitance C_T the expression of q_{max} is given by:

$$q_{max} = \frac{C_T}{2N} A = \frac{A}{Z_0 v} \tag{4.14}$$

where N is the number of stages, A the amplitude of the signal, Z_0 the loaded impedance of the resonator, and v the velocity of the electrical wave in the loaded resonator. The contribution of all noises results in an expression for the phase noise given by:

$$L\{\Delta\omega\} = 10.log\left(\frac{\Gamma_{rms}^2}{q_{max}^2}\frac{N(\bar{i_t^2}/\Delta f)}{2\Delta\omega^2}\right) \tag{4.15}$$

$$L\{\Delta\omega\} = 10.log\left(\frac{N^2\pi^2}{2C_T^2A^2(n+1)^3}\frac{(\bar{i_T^2}/\Delta f)}{2\Delta\omega^2}\right) \tag{4.16}$$

where $\bar{i_T^2} = N\bar{i_t^2}$. With the simplification:

$$E\left(\frac{N}{\pi} - \frac{1}{2}\right) \approx \frac{N}{4}$$

which is valid for value of N under 40, one can rewrite the expression of phase noise:

$$L\{\Delta\omega\} = 10.log\left(\frac{64\pi^2}{2C_T^2A^2N}\frac{(\bar{i_T^2}/\Delta f)}{2\Delta\omega^2}\right) \tag{4.17}$$

$$\text{or } L\{\Delta\omega\} = 10.log\left(\frac{4Z_0^2}{A^2N}\frac{(\bar{i_T^2}/\Delta f)\omega_0^2}{\Delta\omega^2}\right) \tag{4.18}$$

The amplitude A is dependent on the current in the gain stages and the quality factor of the differential line. Since $R_{eq} = Q_L Z_0$ the amplitude of

the differential signal can be expressed:

$$A = R_{eq} I_{diff} = Q_L Z_0 I_{diff} \tag{4.19}$$

where I_{diff} is the differential current of the gain stage. Finally we have an expression for phase noise:

$$L\{\Delta\omega\} = 10.log\left(\frac{4Z_0(\bar{i_T^2}/\Delta f)}{NP_{diss}Q_L^2}\frac{\omega_0^2}{\Delta\omega^2}\right) \tag{4.20}$$

This equation is an analytical description of the phase noise spectrum of an RTW-VCO in the $1/f^2$ region of the phase noise spectrum. It is interesting to note that contrary to the Leeson's formula no fitting parameter is used. The equation merits some remarks. First it is compatible with the widely known Leeson's model. The phase noise in dB is inversely proportional to the quality factor squared and to the power dissipation. But like in the results of the simulated circuits 4.7 there is a dependency on the number of stages loading the line. This is a remarkable characteristic of the RTW-VCO. The ring oscillator for example has also a Γ_{rms} dependent on the number of stages but the total phase noise is not dependent on it in the single stage case and degrades with it for the differential case [31]. With the RTW-VCO, for the same total negative resistance, the more distributed it is, the better the phase noise. The equation predicts that doubling the number of stages results in an improvement of 3 dB for the $1/f^2$ phase noise region. This is indeed what is simulated figure 4.7.

Now the value of the phase noise at 1MHz offset for the 18GHz RTW-VCO will be calculated with this formula. For the circuit designed it was found previously that the loaded impedance is $Z_{loaded} = 9.32\Omega$ and the quality factor is $Q_L = 9.3778$. There are four stages: n=4. The total thermal noise

injected is simulated: $\frac{\bar{i_t^2}}{\Delta f} = 1.309344.10^{-21} A^2/Hz$. Finally, the value found with the expression 4.20 is:

$$L\{1MHz\} = -117.89\ dBc/Hz \tag{4.21}$$

which is to be compared with the $-119\ dBc/Hz$ simulated and the $-117\ dBc/Hz$ measured experimentally. The predicted phase noise with the analytical equation is in excellent agreement with the simulated and the experimental measurements. For the second circuit implementation (36GHz) the evaluation of the phase noise is with $n = 4$, $Z_0 = 11.58\Omega$, $Q_L = 3.34$, $P_{loss} = 9.6mW$, and $\frac{\bar{i_t^2}}{\Delta f} = 9.0344.10^{-22} A^2/Hz$:

$$L\{600kHz\} = -86\ dBc/Hz \tag{4.22}$$

which is to be compared with the the $-87dBc/Hz$ measured and the $-89dBc/Hz$ simulated with Cadence Spectre.
The two circuits measured are in agreement with the formula 4.20. It is also compatible with the equation of C.J.White [39] who recently developed an expression for phase noise in distributed oscillators. He made the evaluation for a single ended distributed oscillator, the circuit as described in the chapter 5.1. White's expression is:

$$L\{\Delta\omega\} = 10.log\left(\frac{Z_0^2 \sum \Gamma_{eff.rms}^2 . i_n^2/\Delta f}{V^2} \frac{f_0^2}{2\Delta\omega^2}\right) \tag{4.23}$$

The term $\sum \Gamma_{eff.rms}^2$ makes the expression valid for every offset frequencies, whereas the expression 4.20 is not valid for the 1/f up-conversion region. Meanwhile the term $\sum \Gamma_{eff.rms}^2$ can only be simulated and it is hard to see how variation of parameters influences the phase noise. Advantage of the

expression 4.20 is that parameters of the circuit are present. The expression 4.23 is unable to predict at the first sight that increasing the number of gain stages goes with an improvement in phase noise performances. The expression developed here, despites some simplifications, instantaneously delivers the possible ways to improve performances. In the case of the single ended DVCO, noise is dominated by the noise generated by the terminations. An improvement of the quality factor of the resonator (without termination: line plus loading gain stages) has only little influence on the total quality factor, strongly attenuated by the losses in the terminations. Consequently C. J. White and A. Hajimiri wrote that: *"the phase noise is largely independent of the loss in the transmission line"* In the case of the RTW-VCO, the termination problems do not take place since the resonator is closed on itself. The losses in the loaded line then play a major role which cannot be ignored since they are the main source of noise.

According to the expression 4.20, the simplest way to minimize the noise is to use as many as possible distributed stages. That remains valid until a certain limit. While supposing that, in practice, the layout remains realizable, a drastic reduction in dimensions of the transistors does not go without an non-linear increase in the gate resistance , and thus finally decreases the quality factor of the resonator. A compromise must be found between the quality factor and the number of stages loading the line.

Another interesting approach for the phase noise description is to consider the RTW-VCO as a coupled oscillator system. A gain stage with the loaded resonator stands for one oscillator. So with N stages one can consider the VCO as a N coupled oscillators system. The theory for phase noise in coupled oscillators has been extensively studied [40] [41] [42]. The theory developed in [40] proves that, neglecting the AM to PM conversion, the near-carrier phase noise is reduced by $1/N$ that of a single oscillator, provided the coupling network is reciprocal. In the case of the RTW-VCO the coupling

results from the line resonator, there is a strong reciprocal coupling between the virtual single oscillators. The term virtual is used here because there is in fact no separation possible between each oscillator since they share the same resonator. The loaded line in this interpretation plays a doubled role, one for the coupling, the other for the resonator of each oscillator. The phase noise for a single oscillator can be estimated the same way as the complete RTWO and is given by:

$$L_{singleosc}\{\Delta\omega\} = 10.log\left(\frac{4Z_0(\bar{i_t^2}/\Delta f)}{(P_{diss}/N)Q_L^2}\frac{\omega_0^2}{\Delta\omega^2}\right) \tag{4.24}$$

where P_{diss} is the total power dissipation with all the stages accounted for. With $L\{\Delta\omega\} = \frac{1}{N}L_{singleosc}\{\Delta\omega\}$ and $\bar{i_T^2} = N\bar{i_t^2}$, the expression of the noise in the $1/f^2$ is identical to the equation 4.20.

4.3.2 Flicker noise

The simulations of the resonator for different number of gain stages show also a variation of the point ω_{1/f^3}. The improvement for the 1/f noise up-conversion is presented in fig 4.10. On this figure it is clear that the offset frequency ω_{1/f^3} decreases with an increasing number of gain stages. It should be noted that for these simulations no varactor was used. However part of the flicker noise up-conversion still comes from voltage dependent capacitance [35] which converts AM noise into FM noise. Indeed the loading capacitances of gain-stages are voltage dependent, see figure 4.11 where the contribution of the NMOS and PMOS is visible. The figure 4.11 shows two different small signal capacitance variations, one with the dimension of transistors doubled compared to the other. The capacitance for the small dimension stage is evidently smaller by a half. To understand why the 1/f

noise differs from one case to the other, one needs to express the current noise for each case. For the first one we have from [1]:

$$\bar{i}_{n1}^2 = \frac{KG_m^2}{C_{ox}WL}\frac{1}{f} \tag{4.25}$$

where K is a process dependent constant and G_m the transconductance of one gain stage. The notation assumes a bandwidth of 1 Hz.
For the second case the width of transistors are divided by two, the current noise is:

$$\bar{i}_{n2}^2 = \frac{K(G_m/2)^2}{C_{ox}(W/2)L}\frac{1}{f} = \frac{\bar{i}_{n1}^2}{2} \tag{4.26}$$

Due to the distributed nature of the system, in both cases the impedance of the loaded resonator stays the same. Thus the AM noise in the second case is two time lower than for the first one, indeed:

$$\bar{v}_{n1}^2 = Z_0 * \bar{i}_{n1}^2 \tag{4.27}$$

$$\bar{v}_{n2}^2 = Z_0 * \bar{i}_{n2}^2 = Z_0 * \frac{\bar{i}_{n1}^2}{2} \tag{4.28}$$

The noise voltage source resulting from the 1/f noise of transistors is thus inversely proportional to the number of stages loading the capacitance at the condition that the loaded impedance stay the same in the resonator and that the model of 1/f noise stays valid for the dimensions of transistors used. Noise sources in both cases are not correlated to each other so that the total AM noise is the sum of all noise sources.

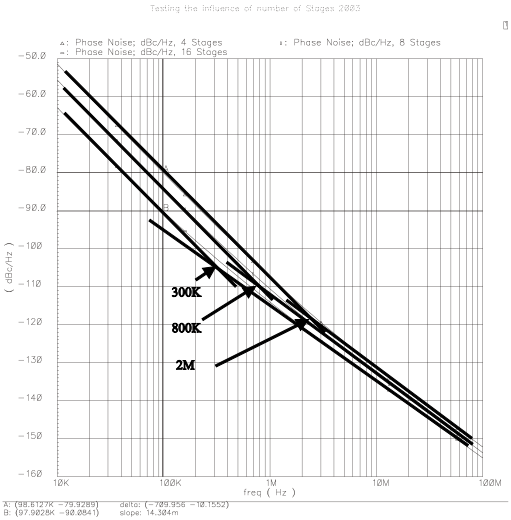


Figure 4.10: Phase noise simulation with Spectre for the three increasingly distributed resonators

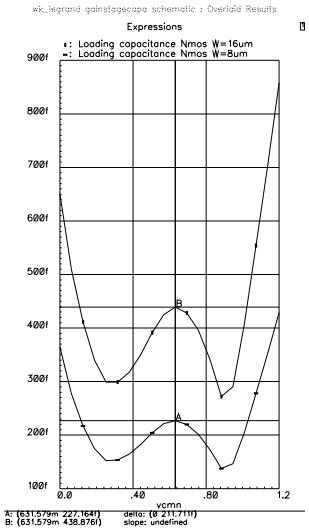


Figure 4.11: Small signal capacitance of two loading gain stages with different dimensions

Chapter 5

Comparison of VCO implementations

After having studied in detail the RTW-VCO, it is now time to compare this structure with its potential competitors. The ring and relaxation oscillators are not really serious competitors since they achieve at high frequencies modest noise properties for a large current consumption [31]. That is mainly due to the lack of resonator. Moreover the topologies of these oscillators have a sensitivity to noise maximum when the oscillation is in the area of zero voltage crossing, unfortunately at the same time the current flowing through the transistors is maximum. The maximum sensitivity to perturbations occurs in a period when the noise is in its worse case, making it very difficult to obtain good phase noise performances. An advantage of the ring oscillator still stays the easiness of multiple phases generation it may provide. Another advantage is the small area the layout of both oscillators are requiring.

More interesting is the comparison with the LC-tank oscillator which is the standard established for most integrated oscillators combining low power consumption with good phase noise properties. A precise comparison is needed to understand the advantages of the RTW-VCO.

5.0.2.1 Scaling effects

First the resonator design is compared for a fixed oscillation frequency f_{osc}. In the case of the LC-tank, as seen in the appendix C the frequency f_{osc} is defined as:

$$f_{osc} = \frac{1}{2\pi\sqrt{L_{LC}C_{LC}}} \tag{5.1}$$

where L_{LC} and C_{LC} are the resonator inductance and capacitance required to obtain f_{osc}. For the RTW-VCO we also saw in the chapter 3 that the frequency of oscillation was given by:

$$f_{osc} = \frac{1}{\sqrt{L_d C_d}} \tag{5.2}$$

where L_d and C_d are the total inductance and capacitance of the loaded resonator. It is directly observable that for the same target frequency the inductance or capacitance of the distributed oscillator is multiplied by a factor $4\pi^2$ compared to the LC-tank. For the same f_{osc} we have:

$$L_d = 4\pi^2 L_{LC}$$
$$\text{or } Cd = 4\pi^2 C_{LC}$$

It has to be counted as a great advantage for the RTW-VCO. Indeed, as the frequency of operation increases the LC product must decrease. However the parasitic capacitances of transistors, the loading from output buffers and the

tuneability required result on restrictions on the minimum capacitance C usable. This leads thus to smaller values of inductance L and consequently to larger power dissipation. The distributed structure topology tends to delay the process: either the minimum capacitance value margin is relaxed (more parasitics or loading capacitance are allowed), or the inductance value is larger (power optimization). For example, designing a LC-tank oscillator at 18GHz with the same amount of capacitive loading as in the RTW-VCO presented in this work would have required an inductance of $12.4pH$ which is practically not realizable. With a capacitive loading divided by $4\pi^2$ the inductance should be $480pH$. It would be possible to realize it but it still would generate only one phase contrary to the RTW-VCO which gives access to two quadrature outputs. For the scalability the RTW-VCO topology is advantageous. It can drive larger capacitance than its LC-tank counterpart for the same inductor value.

From a practical point of view, measurements for the couple strip-line pair are easier than for the single inductor (spiral or horse shoes see Annexe A for one example). The characterization of the strip-line pair can be done for large length and then be scaled linearly whereas for the single inductance, one device after the other has to be measured, which is an even more difficult task as the values of inductors go down. For inductances in the pH area, the deembeding structure have values comparable or even higher than the device under test making the measurements very difficult. Finally, for the simulation, the model for the coupled strip-line pair is simple: the variation of inductance, capacitance and resistance are varying linearly with the length for a given frequency, whereas the model of inductor at high frequency are even more complicated, hardly scalable and less physically related since they result often from a fitting of parameters with the measurements.

5.0.2.2 Power Consumption, several signal phases generation

The power consumption is a major concern, a strength of the LC-tank topology is its low consumption. The RTWO has an adiabatic operation which makes it very attractive too. To compare the two topologies the minimum negative resistance G_{mNR} required should be defined in each case for the same operating frequency. However it is very difficult to compare fairly both topologies. The consumption in both cases is very dependent on the quality factor and loaded impedance of their respective resonator. The loaded impedance of the strip-line pair will be improved with decreasing dielectric in the next generation of processes, however it will still stay far lower than what can be achieved with the LC oscillator. In comparison, an inductor-based LC-resonator with an impedance of 50 ohms at the resonance is common whereas in our examples a value of 10 ohms is hardly achieved. This leads to more consumption for the oscillator core in the distributed case. On the other hand the output power of the distributed oscillator is higher than for the LC-tank. The output can be delivered directly to a low impedance. Moreover the number of outputs do not increase drastically the consumption of the RTW-VCO, whereas if several phases are needed with the LC tank, in the case of coupled oscillator the consumption is at least multiplied by a factor 1.5. For the consumption, if more than one signal phase is needed, the RTW-VCO is an attractive alternative to the LC tank based oscillator.

5.0.2.3 Phase Noise

Since the RTW-VCO as well as the LC-VCO are based on integrated resonator they have both good phase noise performances. Both are dependent on their respective quality factor. Both topologies have comparable performances. The structure of reciprocal coupled gain stages of the RTW-VCO

allows the variation of a new parameter to improve the phase noise: the distribution rate. As seen in the previous chapter the larger the number of gain stages for a given total gain, the better the phase noise.

Chapter 6

Conclusion

6.1 Achievements

In this work a study of the circuit topology for rotary traveling wave voltage controlled oscillator was done. It has been shown that the RTW-VCO combines the advantages of the LC oscillator and the ring oscillator without their respective drawbacks. The topology allows the generation of more than one signal phase. It is based on a resonator architecture making low power consumption combined with good spectral purity possible. To describe the operation of the new oscillator a review of the distributed amplifier has been done from which the structure is derived. The quality factor of the strip-line resonator has been defined as well as its cutoff frequency. These parameters influence the power consumption as well as the phase noise. An analytical phase noise equation has been developed which predicts the influence of parameter variation like the number of gain stages or the loaded quality

factor. It has been shown that the most distributed the structure was, the best optimization for phase noise and power consumption.
Two circuits were designed, fabricated and tested in $0.13\mu m$ gate-length CMOS technology. They are capable of providing oscillation frequencies of respectively 18GHz and 36GHz while providing 5% of tuneability. These were the first RTW-VCO circuits at such high frequencies. The feasability on standard process of fabrication has been proved. The phase noise of these oscillators is very competitive with the LC-tank oscillator. Phase noise of $-118dBc/Hz$ at 1 MHz offset for the 18GHz and $-87dBc/Hz$ at 600 kHz offset for the 36GHz have been measured. These values are in agreement with the formula for phase noise derived from the Hajimiri description of phase noise. This formula is compatible with the widely known Leeson's formula and with the recently published formula from White specific to the single-ended distributed oscillator.

Appendix A

Development of calculations

to obtain the equation 2.17 page 12

$$V_{out} = \frac{Z_0}{2} \int_0^{Nl_d} I_0(z') e^{-j\beta_d (Nl_d - z')} dz' \tag{A.1}$$

with $I_0(z') = V_{in}\frac{-g_m}{l_d}v_g(z) = \frac{-g_m}{l_d}e^{-j\beta_g(\frac{l_g}{l_d z'})}$ $(V_{in}=1)$

$$= -\frac{Z_0}{2}\frac{g_m}{l_d}e^{-jN\beta_d l_d}\int_0^{Nl_d} e^{-j\beta_g(\frac{l_g}{l_d z'})}e^{j\beta_d z'}dz' \tag{A.2}$$

$$= -\frac{Z_0}{2}\frac{g_m}{l_d}e^{-jN\beta_d l_d}\left[\frac{e^{j(\beta_d-\beta_g\frac{l_g}{l_d})z'}}{j(\beta_d-\beta_g\frac{l_g}{l_d})}\right]_0^{Nl_d} \tag{A.3}$$

$$= -\frac{Z_0}{2}\frac{g_m}{l_d}e^{-jN\beta_d l_d}\left(\frac{e^{j(\beta_d Nl_d-\beta_g Nl_g)}-1}{j(\beta_d-\beta_g\frac{l_g}{l_d})}\right) \tag{A.4}$$

$$= -\frac{Z_0}{2}g_m e^{-jN\beta_d l_d}\left(\frac{e^{j\beta_d Nl_d}\left(e^{-j\beta_g Nl_g}-e^{-j\beta_d Nl_d}\right)}{j(\beta_d l_d-\beta_g l_g)}\right) \tag{A.5}$$

$$= -\frac{Z_0}{2}g_m\left(\frac{e^{-j\beta_g Nl_g}-e^{-j\beta_d Nl_d}}{j(\beta_d l_d-\beta_g l_g)}\right) \tag{A.6}$$

$$= -\frac{NZ_0}{2}g_m\left(\frac{e^{-j\beta_g Nl_g}-e^{-j\beta_d Nl_d}}{jN(\beta_d l_d-\beta_g l_g)}\right) \tag{A.7}$$

$$\tag{A.8}$$

$$V_{out} = -\frac{NZ_0}{2}g_m e^{-jN\beta_g l_g}\frac{1-e^{-j(\beta_d l_d N-\beta_g l_g N)}}{jN(\beta_d l_d-\beta_g l_g)} \tag{A.9}$$

for $\beta_d l_d \to \beta_g l_g$ one can expand $e^x = 1+x+O(x^2)$

$$= -\frac{NZ_0}{2}g_m e^{-jN\beta_g l_g}\frac{1-1+j\left(\beta_d l_d N-\beta_g l_g N\right)-O((j\left(\beta_d l_d N-\beta_g l_g N\right)^2)}{jN(\beta_d l_d-\beta_g l_g)} \tag{A.10}$$

$$A_v \underbrace{=}_{\beta_d l_d\to\beta_g l_g} -\frac{NZ_0}{2}g_m e^{-jN\beta_g l_g}. \tag{A.11}$$

Appendix B

Distributed Networks

Distributed networks differ from ordinary electric networks in one key feature: the electrical size. In an ordinary network the physical wavelength of signals is much larger than the circuit size. Circuits are thus described by lumped elements over which no spacial variation of current or voltage is possible. On the other hand a distributed network has usually the size of an appreciable fraction or even of multiple wavelengths of the signal. In this case a distributed parameter network is necessary. Voltage and current can vary in magnitude and phase over the length of a circuit element. A review of the tapped transmission line equations as distributed network and their mathematical description will be presented. Transmission line are the core of the resonator for the distributed oscillators considered in this work. Periodic structures, as defined in [14] are referred as transmission line periodically loaded with reactive elements with or without resistive elements in series. Their study is a key to understand the influence of tapped elements

loading the VCO resonator. Some examples will be considered which can directly be used for the study of the resonator of distributed VCOs. A quality factor of these structures will be given.

B.1 Periodic Structures

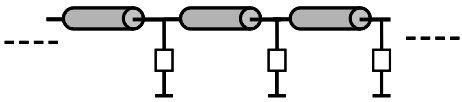


Figure B.1: Strip-line periodically loaded

Periodic structures are defined as transmission lines periodically loaded with reactive and resistive elements. They act similar to filters with pass and stop-band characteristics. A "slow wave" can propagate with a velocity inferior to the phase velocity of the unloaded line. A cut-off frequency may be then defined, above which no wave can propagate. Transmission properties of loaded strip lines are described with the help of the reciprocal two-port network theory and the image parameter method [14]. The periodic structure is a cascade of identical two ports networks. A two ports network is fully defined with the ABCD parameters. The image impedances Z_{i1} and Z_{i2} are defined as matching impedance to each port 1 and 2 (figure B.2) . For a reciprocal two-port network, the equation of the ABCD parameters is given by:

$$\begin{pmatrix} V_1 \\ I_1 \end{pmatrix} = \begin{pmatrix} A & B \\ C & D \end{pmatrix} \begin{pmatrix} V_2 \\ I_2 \end{pmatrix} \tag{B.1}$$

with $AD - BC = 1$ (reciprocal network). If the network is symmetrical $A = D$.

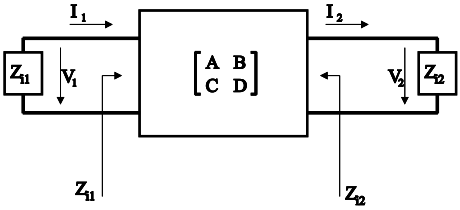


Figure B.2: Two-port network terminated with its image impedance

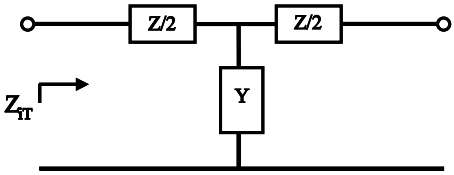


Figure B.3: Elementary T-section

The image impedance is derived for a reciprocal network.

$$Z_{i1} = \sqrt{\frac{AB}{CD}} \tag{B.2}$$

$$Z_{i2} = \sqrt{\frac{DB}{CA}} \tag{B.3}$$

The image propagation factor is defined as:

$$e^{-\gamma} = \sqrt{AD} - \sqrt{BC} \tag{B.4}$$

with $\gamma = \alpha + j\beta$. Since $AD - BC = 1$, γ is more conveniently expressed as:

$$\gamma = cosh^{-1}(\sqrt{AD}) \tag{B.5}$$

Applying these results to the elementary section shown in figure B.3 , we

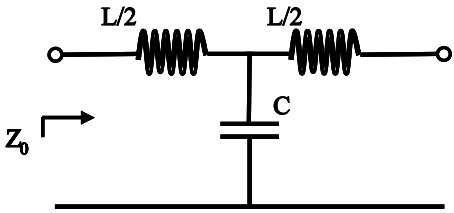


Figure B.4: Elementary LC-section

get:

$$Z_{iT} = \sqrt{\frac{z}{y}(1 + \frac{zy}{4})} \tag{B.6}$$

and

$$\gamma = cosh^{-1}(1 + \frac{zy}{2}) \tag{B.7}$$

B.1.1 Lossless Lumped Transmission Line

For a lossless cascade of elementary LC-sections such as in the figure B.4, the image impedance and propagation factor are:

$$Z_0 = \sqrt{\frac{L}{C}(1 - \frac{\omega^2}{\omega_c^2})} \tag{B.8}$$

and

$$cosh\gamma = 1 - \frac{2\omega^2}{\omega_c^2} \tag{B.9}$$

with $\omega_c = 2/\sqrt{LC}$ the cutoff frequency up to which the image impedance goes from real to imaginary values. Beyond ω_c, the propagation factor has a real component attenuating the transmission. More precisely, expanding

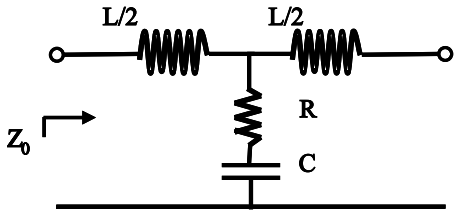


Figure B.5: Elementary L-CR section

$cosh(\alpha + j\beta) = cosh(\alpha)cos(\beta) + jsinh(\alpha)sin(\beta)$ we obtain:

- for $0 \leq \omega < \omega_c$, $\alpha = 0$ and $\beta = 2sin^{-1}\frac{\omega}{\omega_c}$
- for $\omega_c \leq \omega < \infty$, $\alpha = cosh^{-1}\frac{\omega}{\omega_c}$ and $\beta = \frac{\pi}{2}$

B.1.2 Lumped Transmission Line tapped with a capacitance and a resistance in series

An analysis of the structure depicted in the figure B.5 is important since it models simply, as we will see later, a transistor tapping a transmission line with its gate. The image impedance of the periodic structure is:

$$Z_0 = \sqrt{\frac{L}{C}(1 + j\frac{\omega}{\omega_r} - \frac{\omega^2}{\omega_c^2})} \tag{B.10}$$

where $\omega_c = 2/\sqrt{LC}$ and $\omega_r = 1/RC$. The impedance has an imaginary part resulting from the resistive losses within the line. The propagation factor is derived from the equation:

$$cosh\gamma = 1 - \frac{\omega^2}{2\omega_c^2}\frac{1}{1 + j\frac{\omega}{\omega_r}} \tag{B.11}$$

Splitting the equation into real and imaginary parts, we obtain:

$$cosh(\alpha)cos(\beta) + jsinh(\alpha)sin(\beta) = 1 - \frac{2\omega^2/\omega_c^2}{1+(\omega/\omega_r)^2} + j\frac{2(\omega/\omega_c)^2\omega/\omega_r}{1+(\omega/\omega_r)^2} \tag{B.12}$$

For $\omega << \omega_c$ $cosh\alpha \approx 1$ and $sinh\alpha \approx \alpha$ expressions of α and β may be extracted from:

$$cos\beta \approx 1 - \frac{2\omega^2/\omega_c^2}{1+(\omega/\omega_r)^2} \tag{B.13}$$

using $cos^2 + sin^2 = 1$ we obtain:

$$\beta \approx 2\sqrt{\left(1 - \frac{\omega^2/\omega_c^2}{1+(\omega/\omega_r)^2}\right)\frac{\omega^2/\omega_c^2}{1+(\omega/\omega_r)^2}} \tag{B.14}$$

and

$$\alpha \approx \frac{(\omega/\omega_c)^2\omega/\omega_r}{\sqrt{(1+(\omega/\omega_r)^2 - \omega^2/\omega_c^2)\,\omega^2/\omega_c^2}} \tag{B.15}$$

B.1.3 Lumped Transmission Line with losses

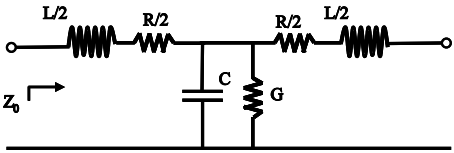


Figure B.6: Elementary lossy lumped transmission line

In this example influence of intrinsic losses from lossy inductance and lossy capacitance will be examined. In a first approximation, for low-loss line the image impedance is:

$$Z_0 = \sqrt{\frac{L}{C}(1 - \frac{\omega^2}{\omega_c^2})} \tag{B.16}$$

with $\omega_c = 2/\sqrt{LC}$.
The propagation and attenuation factor have to be extracted from the equality:

$$cosh(\alpha+j\beta) = 1+\frac{(R+jl\omega)(G+jC\omega)}{2} = 1-\frac{2\omega^2}{\omega_c^2}+j\frac{2\omega}{\omega_c^2}\left(\frac{G}{C}+\frac{R}{L}\right) \quad \text{(B.17)}$$

With the approximations $\omega << \omega_c$, $cosh\alpha \approx 1$, and $sinh\alpha \approx \alpha$ expressions of α and β are:

$$\alpha \approx \frac{\frac{2\omega}{\omega_c^2}\left(\frac{R}{L}+\frac{G}{C}\right)}{\sqrt{1-\left(1-\frac{2\omega^2}{\omega_c^2}\right)^2}} \quad \text{(B.18)}$$

and

$$\beta \approx \sqrt{1-\left(1-\frac{2\omega^2}{\omega_c^2}\right)^2} \quad \text{(B.19)}$$

The accuracy of these expressions decreases as ω approachs ω_c.

B.1.4 Lumped Transmission Line with losses and resistance in series with the capacitance

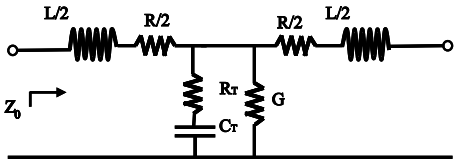


Figure B.7: Elementary lossy lumped transmission line with resistive tap

In this example the effect of both intrinsic losses within the artificial transmission line and the resistive losses due to non-ideal capacitance tapping the line are considered. This example combines the both previous one and

will be helpful in determining the quality factor of the distributed VCO resonator. We determine the attenuation factor and the propagation factor in this case with the same assumptions as in the previous examples plus the approximation that the intrinsic capacitance of the line is small compared to the capacitance tapping it. We have:

$$cosh\gamma = 1 + \frac{(R + jL\omega)(G + jC\omega)}{2(1 + j\omega RC)} \tag{B.20}$$

What gives after extraction:

$$\beta \approx \sqrt{\frac{\frac{4\omega^2}{\omega_c^2} - \frac{4\omega^2}{\omega_c^2\omega_r}(\frac{R}{L} + \frac{G}{C})}{1 + \frac{\omega^2}{\omega_r^2}} \left[2 + \frac{\frac{4\omega^2}{\omega_c^2\omega_r}(\frac{R}{L} + \frac{G}{C}) - \frac{4\omega^2}{\omega_c^2}}{1 + \frac{\omega^2}{\omega_r^2}}\right]} \tag{B.21}$$

and

$$\alpha \approx \frac{\frac{4\omega^3}{\omega_c\omega_r} + \frac{4\omega}{\omega_r}(\frac{R}{L} + \frac{G}{C})}{\beta(1 + \frac{\omega^2}{\omega_r^2})} \tag{B.22}$$

B.1.5 Quality factor Q of transmission line resonator

The power losses associated with the transmission line we consider are: the conductor losses and the power dissipation in the dielectric of the substrate. Considering a transmission line resonator, the quality factor Q is defined by the following expression:

$$Q = \frac{\omega_0 U}{W} \tag{B.23}$$

where U is the energy stored and W is the average power lost per cycle. With V_m and I_m, the maximum voltage and current at some place along the line, Q may be written in the form:

$$Q = \omega_0 \frac{(LI_m^2/2 + CV_m^2/2)/2}{(RI_m^2 + GV_m^2)/2} \tag{B.24}$$

Assuming the low-loss line conditions are satisfied ($R << \omega L$,$G << \omega C$), $Z_0 = \sqrt{\frac{L}{C}}$ and with $I_m = \frac{V_m}{Z_0}$ we get

$$Q = \frac{\omega_0 \sqrt{LC}}{(R/Z_0 + GZ_0)} \tag{B.25}$$

With α and β as defined for the low-losses line, the Q of a resonant transmission line is yields:

$$Q = \frac{\beta}{2\alpha} \tag{B.26}$$

For a well substrate-isolated line, $\frac{GL}{C} << R$, Q reduces to the familiar expression of a parallel resonant circuit:

$$Q = \frac{\omega L}{R} \tag{B.27}$$

As we define the quality factor for the low-loss transmission line resonator, it is instructive to define the Q of the periodic structures considered previously. Since $Q = \frac{\beta}{2\alpha}$ we can directly write after simplifications:

- Case 1: low-loss lumped transmission line

$$Q = Q_l \left(1 - \frac{\omega^2}{\omega_c^2}\right) \tag{B.28}$$

  with $Q_l = 1/(\frac{R}{\omega L} + \frac{G}{\omega C})$ which is the quality factor of the non-lumped equivalent transmission line. ω_c is the cutoff frequency of the line. The higher the cutoff frequency (or also called bragg frequency), the closer the Q is from its continuous equivalent counterpart Q_l.

- Case 2: Lossless lumped transmission line with resistance in series to the capacitance

$$Q = \frac{\omega_r}{\omega} \left(1 - \frac{\omega^2/\omega_c^2}{1 + \omega^2/\omega_r^2}\right) \tag{B.29}$$

with $\omega_r = 1/RC$. In most cases the product RC is dependent on the technology and materials used. The only way to improve the Q is to increase ω_c.

- Case 3: Low-loss lumped transmission line with resistive taps
  This case is the combination of the both previous one. As $Q_l \to \infty$ the quality factor should be the one of the second case and as $R_T \to 0$ the quality factor should be the one of the case 1.

$$Q = \frac{1 - \frac{\omega}{\omega_r}\frac{1}{Q_l}}{\frac{\omega}{\omega_r} + \frac{1}{Q_l}} \left(1 - \frac{\frac{\omega^2}{\omega_c^2}\left(1 - \frac{\omega}{\omega_r}\frac{1}{Q_l}\right)}{1 + \frac{\omega^2}{\omega_r^2}} \right) \tag{B.30}$$

  where $\omega_r = 1/R_T C_T$, $Q_l = 1/(\frac{R}{\omega L} + \frac{G}{\omega C})$ and $\omega_c = 2/\sqrt{LC}$.
  As for the second case ω_r is dependent on the technology used, then the only direct way to improve the Q is to increase the ω_c. It means that to obtain a better Q the number of lumped elements in the line has to be maximized (L and C decrease).
  This example will be helpful to determine the selectivity of the distributed resonator. The selectivity of the resonator is directly correlated to the noise sensitivity.

Appendix C

Coupled transmission line

The properties of a pair of transmission line uniformly coupled is presented. An equivalent circuit from the coupled transmission line pair is shown figure C.1 Applying the Kirchhoff's laws to the incremental circuit results in

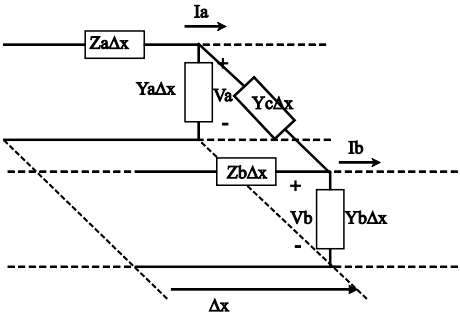


Figure C.1: Incremental equivalent circuit for a coupled transmission line pair.

the following equation:

$$-\frac{\delta V_a}{\delta x} = Z_a I_a \tag{C.1}$$

$$-\frac{\delta I_a}{\delta x} = Y_a V_a + Y_c(V_a - V_b) \tag{C.2}$$

$$-\frac{\delta V_b}{\delta x} = Z_b I_b \tag{C.3}$$

$$-\frac{\delta I_b}{\delta x} = Y_b V_b + Y_c(V_b - V_a) \tag{C.4}$$

$$\tag{C.5}$$

which gives combined:

$$\frac{\delta^2 V_a}{\delta x^2} = Z_a(Y_a + Y_c)V_a - Z_a Y_c V_b \tag{C.6}$$

$$\frac{\delta^2 V_b}{\delta x^2} = Z_b(Y_b + Y_c)V_b - Z_b Y_c V_a \tag{C.7}$$

Assuming the solutions are of the form: $V = V_0 e^{\gamma x}$, the dispersion equation is given by:

$$\begin{vmatrix} \gamma^2 - Z_a(Y_a + Y_c) & Z_a Y_c \\ Z_b Y_c & \gamma^2 - Z_b(Y_b + Y_c) \end{vmatrix} = 0 \tag{C.8}$$

It results:

$$\gamma = \pm \left(\frac{Z_a(Y_a + Y_c) + Z_b(Y_b + Y_c) \pm \sqrt{\left[Z_a(Y_a + Y_c) - Z_b(Y_b + Y_c)\right]^2 + 4Z_a Z_b Y_c^2}}{2} \right) \tag{C.9}$$

$$= \begin{cases} \pm\gamma_1 \\ \pm\gamma_2 \end{cases} \tag{C.10}$$

As Y_c tends to zero, the coupling vanishes, reducing γ_1 to $\sqrt{Z_a Y_a}$ and γ_2 to $\sqrt{Z_b Y_b}$. In the presence of coupling, the voltages in the line can be written as:

$$V_a = A_a e^{-\gamma_1 x} + B_a e^{\gamma_1 x} + C_a e^{-\gamma_2 x} + D_a e^{\gamma_2 x} \tag{C.11}$$

$$V_b = A_b e^{-\gamma_1 x} + B_b e^{\gamma_1 x} + C_b e^{-\gamma_2 x} + D_b e^{\gamma_2 x} \tag{C.12}$$

which is saying that, in general, two waves with different velocities are traveling in each direction. Their amplitudes are dependent on the termination. To visualize the nature of coupled-wave interactions two identical semi-finite lossless transmission lines coupled to each other with a distributed capacitance equal to one half of the intrinsic capacitance of each line. The parameter of propagating waves are thus:

$$\gamma_1 = \pm\sqrt{LC} = \pm j\beta_1 \text{ and, } Z_1 = \sqrt{L/C} \tag{C.13}$$

$$\gamma_2 = \pm\sqrt{2LC} = \pm j\beta_2 \text{ and, } Z_2 = \sqrt{L/2C} \tag{C.14}$$

Amplitudes of the wave are related by:

$$\frac{A_a}{A_b} = \frac{B_a}{B_b} = 1 \tag{C.15}$$

$$\frac{C_a}{C_b} = \frac{D_a}{D_b} = -1 \tag{C.16}$$

The wave with the wave number β_1 is referred to as the fast wave and the wave with the wave number β_2 the slow wave. From the equation C.15 C.16 we conclude that the fast wave are in the two line in phase whereas the slow waves are of opposite phase. The fast and slow wave are also called even and odd mode since they have even and odd symmetry with respect to the ground.

Considering the case of the semi infinite line with equal magnitude for the slow and fast wave the tension are defined as:

$$V_a = A(e^{-j\beta_1 x} + e^{-j\beta_2 x}) \tag{C.17}$$

$$V_a = A(e^{-j\beta_1 x} - e^{-j\beta_2 x}) \tag{C.18}$$

They are only two terms in each equation because of the absence of reflected waves in semi-infinite lines. With two waves coexisting in the medium interferences occurs. The envelope of the interference pattern is :

$$|V_a| = \left| cos\frac{(\beta_2 - \beta 1)}{2}x \right| \tag{C.19}$$

$$|V_a| = \left| sin\frac{(\beta_2 - \beta 1)}{2}x \right| \tag{C.20}$$

If $\beta_2 >> \beta_1$, the even mode or the fast wave is largely attenuated whereas on the contrary if $\beta_1 >> \beta_2$ the period of the envelope approaches infinity and the slow wave is almost inexistent. For the RTW-VCO application it is important to maximize β_2 and to minimize β_1 because the fast wave is a parasitic signal resulting in up-conversion of noise in the resonator.

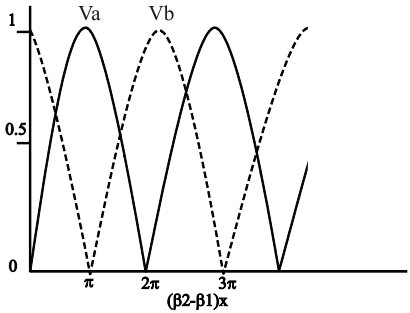


Figure C.2: modulated voltages on the coupled line

Appendix D

Classes of VCOs

There are commonly three different topologies for controlled oscillators on silicon ICs: Ring oscillators, relaxation oscillators and tuned oscillators [1].

- Ring oscillators consist of a number of singled or differential inverters in a loop with feed-back connections. The realization of it is easy to integrate on monolithic IC and very compact. The frequency is usually tuned by varying the current charging or discharging the output capacitance of the inverters. Tuning can be performed over several order of magnitudes.

- Relaxation oscillators alternatively charge and discharge a capacitor with a constant current. Like for the ring oscillator this version can be tuned by varying the current value. The easiness of integration and its compactness make it attractive candidate for integration.

- Tuned oscillators contain a passive resonator which can be an LC tank,

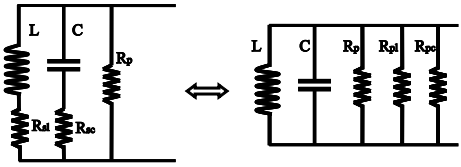


Figure D.1: At frequency resonance the resistive parts in series are equivalent to resistances in parallel

a strip line resonator or a crystal. The resonator sets the frequency of oscillation and the active circuit is there to compensate for the resistive losses. It is more difficult to integrate this type of oscillator because of the lack of good quality passive devices in a standard IC technology. A further disadvantage is the large chip size they require. The Great advantages are the frequency stability, the pure spectrum, and the low power dissipation.

D.1 LC tank oscillator

The description of this type of oscillator give a reference to the described distributed oscillator. LC tank oscillator is one of the most frequently used in high radio frequencies since it can be integrated with good phase noise performances and low power dissipation. It is the ideal candidate for wireless, battery powered communications systems. The simplest way to describe it is to use the one-port model shown in the figure D.1. The passive resonant circuit (tank) is composed of a lossy inductor in parallel with a lossy capacitor and resistive losses. To determine the necessary negative conductance the equivalent parallel resistance of the tank has to be computed. Admittance

of the tank is:

$$Y(\omega) = \frac{1}{R_p} + \frac{1}{j\omega L(1+1/Q_L^2)} + \frac{j\omega C}{1+1/Q_C^2} + \frac{1}{Q_L \omega L(1+1/Q_L^2)} + \frac{\omega C}{Q_C(1+1/Q_C^2)} \tag{D.1}$$

where $Q_L = \omega L/R_{sl}$ and $Q_C = 1/\omega C R_{sc}$ are the quality factors of the inductance and the capacitance respectively. For sufficiently large Q_L and Q_C, second order terms can be neglected. Thus the equivalent circuit of the figure D.1 is applicable where $R_{pl} \approx Q_L \omega L$ and $R_{pc} \approx Q_C/\omega$. The equivalent LC tank is a standard RLC circuit at the resonant frequency $\omega_{res} = \frac{1}{\sqrt{LC}}$ where the characteristic impedance, and the quality factor are:

$$Z_0 = \frac{1}{\omega_{res} L} = \omega_{res} C = \sqrt{\frac{L}{C}} \tag{D.2}$$

$$R_{eq} = R_p // R_{pl} // R_{pc} \tag{D.3}$$

$$Q_T = \frac{R_{eq}}{Z_0} \tag{D.4}$$

$$\frac{1}{Q_T} = \frac{Z_0}{R_p} + \frac{1}{Q_L} + \frac{1}{Q_c} \tag{D.5}$$

The last equation makes it clear that the total quality factor Q_T of the tank is determined by the lowest quality factor component.
To force oscillation at the resonance frequency $\omega_{res} = \frac{1}{\sqrt{LC}}$ a negative conductance g_m is connected in parallel whose minimal absolute value is given by:

$$g_m = \frac{1}{R_{eq}} = \frac{1}{Q_T Z_0} \tag{D.6}$$

In practice, the negative conductance is 2 to 3 time the minimal value to insure good start-up conditions.

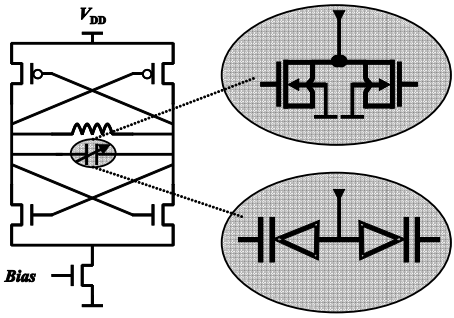


Figure D.2: Implementation of the LC oscillator, varactor implementation with pn-diodes or MOS varactors

D.1.1 Tuning the LC oscillator

The VCO needs to be tuneable for two reasons. The first resulting directly from the application: the system needs to control the operating frequency with a tuning range of a few percent only (the application bandwidth is always much smaller than the center frequency). The second reason why a tuning range of typically +/- 10% is needed comes from the process variations. To vary the frequency of oscillations either inductance has to be changed electronically or the capacitance. Tuneable inductance are not available but voltage dependent capacitances named varactors are standard in CMOS technology. Two kinds of varactors are usually available: the pn junction diode and the MOS varactor [2]. To allow a tune between f_{max} and f_{min} the variable capacitance must at least have a value ΔC which respects the equation:

$$\Delta C > C\frac{f_{max} - f_{min}}{f_0} \tag{D.7}$$

Varactors in CMOS process suffer from several drawbacks. For high frequency VCOs they have a lower quality factor than fixed capacitances or

inductances, so that the tank quality factor reduces if a large tuneability is required. The varactor in both implementations (pn junction or MOS) suffers from parasitic capacitances that limit the tuning range for a given fixed tank capacitance. From the point of view of power consumption, it is always better to maximize the inductance [7] for a given target frequency. Consequently, for a given LC product in the tank, a trade-off must be found between the power consumption and the tuneability required.
Another problem concerns the pn-junction varactors only since they have to remain reverse biased under all conditions, careful design is mandatory. A conduction would degrade the quality factor of the tank severely.
The decrease of power supply in CMOS process degrades the tuneability of the pn-diode and the MOS varactor [5]. As the speed of oscillator increases and the power supply scales down, the tuning voltage faces a dilemma: the tuning range imposed by the process variations must be large enough with a tuning voltage remaining in the window imposed by the voltage supply, and the sensitivity (or gain) of the varactor must remain low. Inevitably, if a large tuning range is required, the sensitivity goes up and with it the sensitivity to noise at the voltage node setting the control voltage. To understand the importance of the sensitivity of the varactor consider a noisy resistance R placed at the tuning voltage node, the phase noise resulting from it is [6]:

$$L\{\Delta\omega\} = 2kTR\left(\frac{K_{VCO}}{\Delta\omega}\right)^2 \tag{D.8}$$

where K_{VCO} is the tuning gain in $[rad/V]$. The expression makes it clear that when the sensitivity goes up the noise at the control voltage affects quadratically the phase noise in dB of the oscillator. Moreover, in a PLL design a high value of K_{VCO} is not an advantage since it can either result in stability problems or it imposes a low impedance driving source which slows down the loop and requires high values of capacitor (area consuming). A

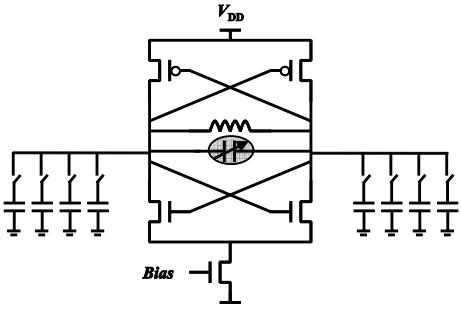


Figure D.3: Discrete Tuning Concept implementation which comes additionally to the continuous tuning from the varactor

solution to overcome this problem is to use a discrete tuning concept with switched fixed capacitances [15]. This way, additionally to the continuous tuning from the varactor, an array of fixed capacitors is used to have a discrete tuning, see Fig D.3. With this concept a wide tuning range with a weak gain K_{VCO} is realizable. The discrete tuning is used for the wide tuning whereas the tuning from the varactor is only the few percent required for the application. The varactor part of the capacitance of the tank decreases, so the K_{VCO} gain may be reduced. As a consequence the sensitivity to variations in tuning voltage and effects of these variations are also reduced. For the array of capacitances Metal-Insulator-Metal capacitance may be used. However the MIMcaps are not available in low-cost processes. Therefore MOS capacitances may also be used as switched-capacitances. However the MOScap have a voltage dependent capacitance and the switching circuitry around it may be noisy so that noise injection in the tank may happen if no care is taken for the design array.

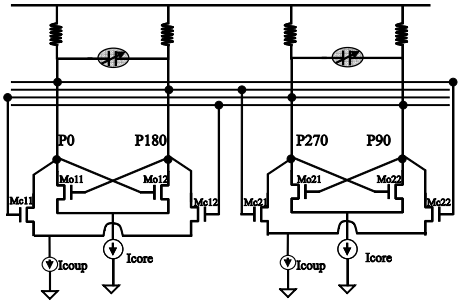


Figure D.4: Current-coupled quadrature VCO

D.1.2 Coupled LC oscillator

The generation of a quadrature phase signal is required in many communication systems, in wireline communications as well as in the RF front-ends of wireless tranceivers [10]- [13]. Three design options are commonly used for quadrature generation [7]:

1. Combination of oscillator with polyphase-filter (or RC-CR filter), and output buffers [8]

2. VCO at the double frequency followed by a master-slave flip-flop (divider).

3. Two cross-coupled VCOs: Quadrature LC-VCO (QVCO)

Despite the cost for the increased silicon area, the low-phase-noise, and the low power performances of the Quadrature LC-VCO (QVCO) make it a good candidate for most applications [7]. The QVCO is made from two current-coupled VCOs as shown figure D.4. Each oscillator consists of a cross coupled pair of transistors (Mo11, Mo12, and Mo21, Mo22) with their respective LC tank. The additional transistors (Mc11, Mc12, Mc21, Mc22) are used for the

coupling between the two oscillators. As reported in [11] such a configuration leads to the generation of two quadrature phase shifted signals. However such a circuit raises the issue of the so called phase ambiguity. The first output can either lead or lag the second output by 90°. Two different modes of oscillation may thus occur leading to an uncertainty in the frequency of operation. The way the mode is selected seems to be unpredictable since it was shown for two symmetrical VCOs that is was independent on the initial conditions [11]. This phenomenon is called bimode oscillation and is a main drawbacks of the structure for generation of quadrature I/Q signals. However, recently, S. Li et al. give a way to eliminate the bimodal effect. He remarks that the change of mode was correlated with the amount of phase shift the coupling network (here transistors Mcxx) introduces. For a certain amount of phase shift in the coupling path the coupled oscillator does not experience bimodal oscillations and this for any coupling current (I_{coup} in Fig. D.4). For a standard configuration as shown in figure D.4 the phase offset of the coupling network has a critical value close to 0° which represents the limit phase offset for which the transition between two modes occurs. For that offset a parasitic backward coupling signal or other small perturbations may easily change the offset so that oscillations at the setting time "struggle" between the two modes. The resulting mode is then settled randomly. One solution proposed in [11] is to use a cascode circuit instead of single transistor for the coupling. It has the advantage of having a non-critical phase shift (not at a transition between two modes) and it attenuates the backward coupling responsible for the main instabilities. Nevertheless the QVCO is a very attractive structure for its noise performances but not without risk for the designer because of the bimodal effect.

Appendix E

Phase Noise Measurement

A typical phase noise measurement setup is show in Figure 1. The output from the oscillator under test (RF) is mixed with the output of a low phase noise reference oscillator set to a frequency so the signal is down converted at 24MHz, this is the first loop. The translated carrier frequency is then mixed with a low phase noise reference set to the same frequency with a relative phase of 90°. The phase shift is adjusted to exact phase quadrature indicated by a minimum DC level at the output of the mixer. The mixer is now operating as a phase detector and produces a voltage proportional to the phase difference of the two sources. Since the reference oscillator has a very low phase noise, the mixer output is principally a function of the phase noise of the oscillator under test. This assumes that neither oscillator has any significant amplitude modulation. The output of the mixer is low-pass filtered to remove the higher-frequency sum terms and mixer leakage spectral components. The output spectrum is read using a wave analyzer or FFT spectrum analyzer. The phase noise is usually displayed as a power

spectral density using units of decibels relative to the carrier power per unit Hz bandwidth (dBc/ Hz).

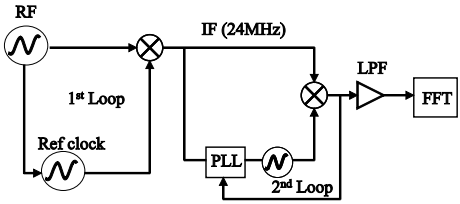


Figure E.1: Test Setup for measuring Phase Noise

Appendix F

Inductance

Monolithic Inductances in CMOS processes suffer from the following sources of performance degradation:

- Eddy current-induced losses, due to magnetic field penetration into the substrate and adjacent traces.
- Trace resistance, due to its finite conductivity and little dimensions. This includes the high frequency degradation effect (skin and proximity effect).
- Substrate capacitance and ohmic losses.

All these losses are depending on the quality of the substrate except the second which is only depending on the quality of the metal used and the geometry. For high frequency applications such as oscillators, one needs to have a good quality factor with a relatively high inductance for the frequency of interest.

F.1 Skin and proximity effect

The inductance formulas are usually given considering a uniformly distributed current over the trace section of the wire (figure F.1(a) and figure F.1(a)). At high frequency the current density is not uniform, there is a tendency for the current to forsake the interior of the cross section and to crowd into portions nearer the surface of the wire (figure F.1(b) and figure F.1(b)). This is the so called "skin effect", the electromagnetic energy penetrates the surface of the conductor and is more and more attenuated and delayed in phase as it approaches the inner center. At very high frequency, the skin depth, a measure of the distance of current's penetration into the wire, becomes very small. The calculation of inductance with geometric mean distance is not valid since most of current is concentrated on the surface, it implies often a slight diminution of the inductance value. The critical parameter in which skin effect plays an important role is the resistance of the conductor. Since the volume in which the current is flowing decreases with frequency, the resistance increases with it. The simplified representation of current density distribution in a trench of wire is described on the figure F.1. One can see the non-uniformity of current density (b) in comparison to the low frequency current distribution (a).

The third schematic (c) in the figure F.1 shows another effect called proximity effect. At high frequency the inductance of the traces becomes vastly more important than their dc-resistance, and current flows in the least inductance pathway. The general principle of least-inductive current flow means for the current to minimize the total stored magnetic field energy. So, at high frequency, the current distributes itself to neutralize all internal magnetic forces. The current in the inductance of figure F.1 (c) is not distributed

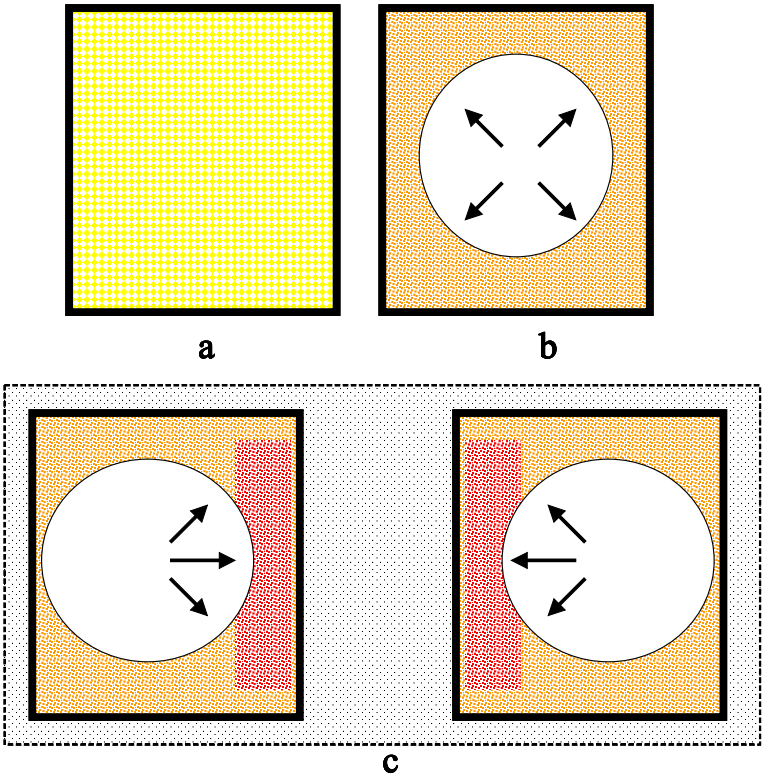


Figure F.1: skin and proximity effect: a) uniform distributed current density; b) the interior of the wire is forsaken contrary to the surfaces where the density is high, this is the "skin effect"; c) the proximity effect results in a asymmetrical distribution of current density, the lowest inductance pathway is favored

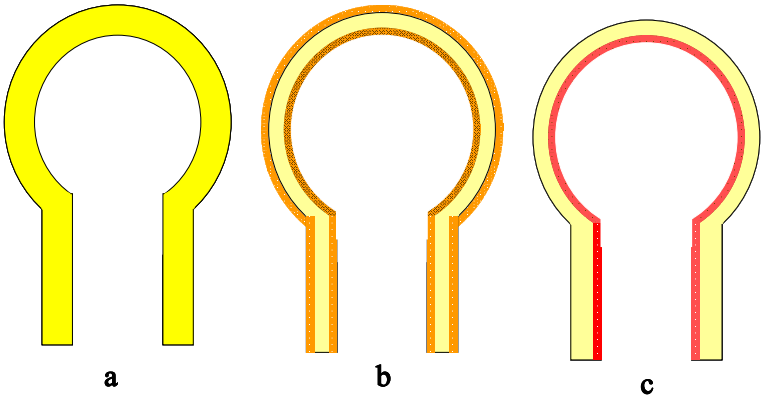


Figure F.2: skin and proximity effect on an inductance: the same remarks as before are valid but from an aerial view.

uniformly around the conductor. Indeed, the magnetic field of the one side of the wire affects the other side, resulting in a nonuniform distribution. The pathway where the inductance is minimized corresponds to the one with the minimum radius. So at the external part of the circle the density is poor whereas it is high at the internal part of the circle. The proximity effect increases the apparent resistance of the conductor since the effective current medium decreases.

F.2 Skin depth

The skin depth is noted δ, it corresponds to the depth through which the amplitude of a traveling plane wave decreases by a factor of e^{-1}, it is also called the depth of penetration. For example, the copper has a skin depth of $0,038mm$ at 3 MHz, and only $0,66\mu m$ at 10 GHz.

F.3 Series resistance

Considering only the skin effect, as far as the dimension of the trace stay very inferior to the skin depth δ, the ac resistance will not be changed. For example for a rectangular trace with W as width, T as thickness:

$$R_{ac} = R_{dc} = \rho \frac{l}{WT} \tag{F.1}$$

with $W, T << \delta$.

F.4 Inductance enhancement

The quality factor of integrated inductances is a critical parameter, it influences directly the LC-tank quality and consequently the spectral purity of the oscillations. A new proposed optimization of the integrated inductance is presented which proves to be very advantageous for quality factor enhancement at high frequencies. The quality factor improvement results from a diminution of skin and proximity effect by a geometrical mean.

The figure F.4 presents three inductances consuming the same area. The inductance 1 has a larger metal width than the inductance 2. It means, the structure 1 (S1) has a lower dc resistance than the structure 2 (S2). However S2 possesses with its lower conductor width and the larger distance between the two conductors a larger inductance value than S1. The longer the current path, the larger the inductance. The broader the conductor, the less resistivity has the conductor. To have a good quality factor the designer should maximize the inductance value and at the same time minimize the resistance, and all this in a minimum area. The structure 3 in figure F.4 proposes a compromise between the two antagonist way of optimization.

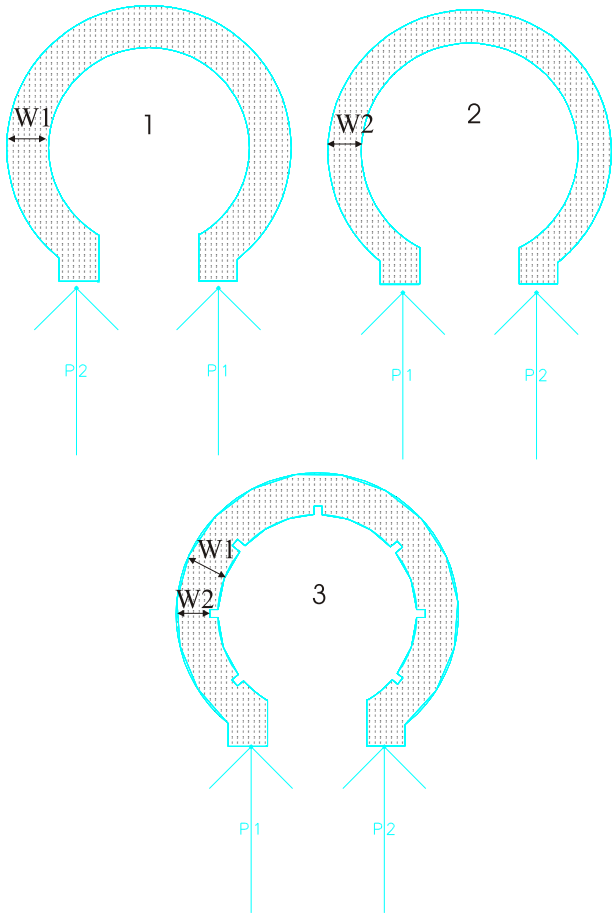


Figure F.3: Different layouts of inductance with the same area consumption in each case.

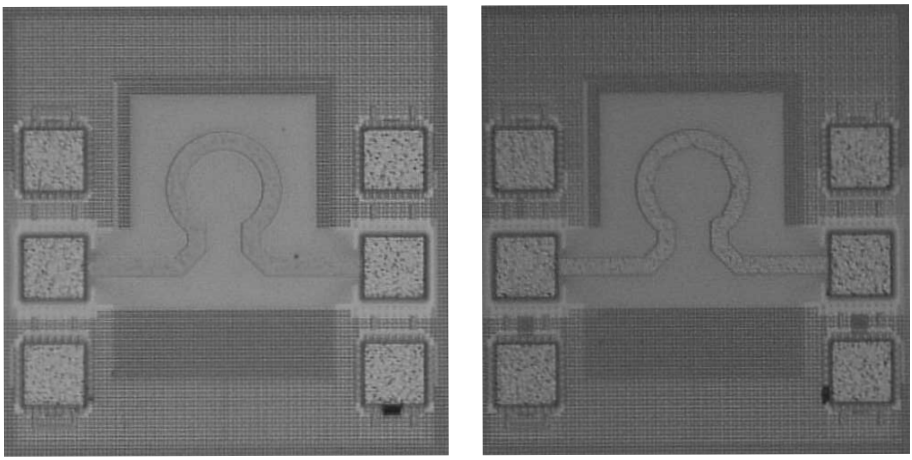


Figure F.4: Layouts of inductances measured.

The notched structure S3 is a mixture of S1 and S2. The holes at the inside forces the current to take a longer path than in the structure S1 and the width of the conductor is only locally reduced so that the total dc resistance is only slightly increased. The major improvement of the notched structure concerns the quality factor at high frequency. Indeed the forced current path decreases the adverse effects of proximity effect (the distance between the two current path is increased) and it also decreases the skin effect which is at high frequencies the dominant effect of losses. The two structure have been made on the metal 8 layer, the target inductance was 200pH. The figure F.4 shows the two layouts. Measurement were performed on-wafer with deembeding structures (Short, Thru, Open). The results are given figure F.4. The enhancement of inductor value is visible but the most interesting result concerns the quality factor. An improvement of 10 points in the quality factor is achieved.

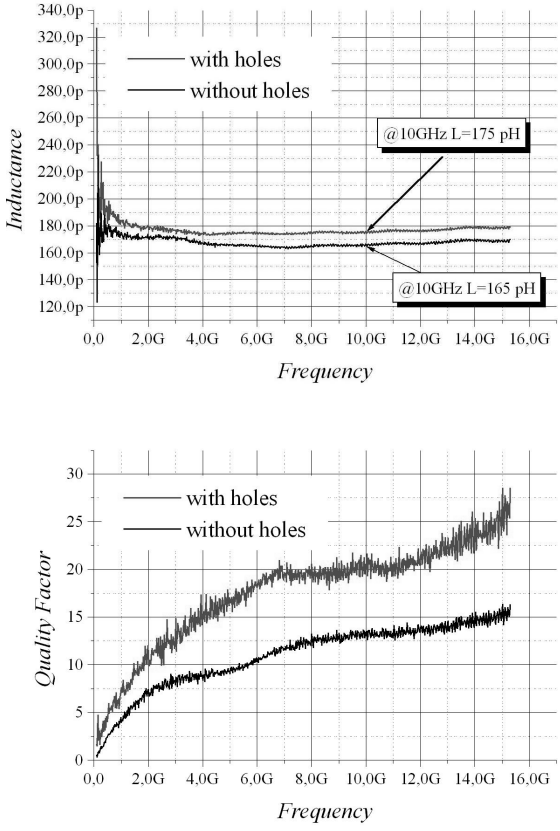


Figure F.5: Comparison of inductance values and quality factors measured for the standard structure and the notched one.

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