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Low Voltage Hot-Carrier Issues in Deep-sub-micron Metal-Oxide-Semiconductor Field-Effect-Transistors

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Abstract

Hot-carrier effects in silicon n-channel MOSFETs were investigated as a function of drain voltage (V_D) and gate voltage (V_G). Impact ionization, gate injection and interface degradation have been observed for qV_D (ballistic energy limit) below the threshold energies for these processes. Detailed investigations were done for qV_D near and below the threshold energies in conventional (CON) uniformly doped channel, and laterally asymmetrical channel (LAC) and vertical MOSFETs.

For large V_D, the substrate current (I_{SUB}) due to impact ionization shows a negative temperature dependence, whereas at low V_D it shows a positive temperature dependence. A detailed investigation of channel length (L) and gate bias (V_G) dependence of this effect in CON devices is presented.

Impact ionization in CON and LAC devices are investigated for V_D near and below bandgap voltage. Two peaks are observed in I_{SUB} vs V_G characteristics at low V_D in CON devices. In LAC devices operated in the forward mode, three peaks are visible. For reverse mode of LAC, signatures of a second peak are observed. Extensive experimental data on L and temperature dependence of these anomalous observations are presented. In all the cases, the first peak was found to be suppressed as the temperature is reduced from 300 to 77 K. The second peak was more distinctly visible at lower temperature and enhanced upon decrease in L. The third peak in the case of LAC operated in the forward mode, enhanced as L and temperature are reduced. Experimental data are analyzed based on Monte-Carlo (MC) simulation data available in the literature and verify the presence of a lattice temperature dependent tail (LTDT) in electron energy distribution (EED) and its broadening due to short-range electron-electron interactions (SREEI). LTDT supports the presence of an electron-phonon interaction (EPI) induced tail to EED. EPI and SREEI can populate the EED beyond the ballistic limit of qV_D. It is shown that the anomalous second peak in I_{SUB} vs V_G is due to SREEI. We find that SREEI is weakened in long channel devices and for large V_G values. SREEI is essentially a mechanism that redistribute energy gained from electric field and it is weakened due to increase in L and V_G which reduce the peak electric field.

By employing one-dimensional self-consistent Poisson-Schrödinger simulations, we have shown that inversion layer quantization can result in an increase in the lowest energy of the electrons near the source side of the channel. This may lead to an effective energy gain of about 40 meV or more depending on V_G.

Two-dimensional drift-diffusion analysis has shown that LAC devices operated in the forward mode has a second high field region near the source. The third peak in I_{SUB} vs V_G is related to this high field region. In this case, since the source electrons are injected directly into a high field region, it is expected that LAC in this mode can be used to experimentally investigate modifications of source EED due to long-range electron-electron interactions predicted by some MC simulation groups.

We have also demonstrated gate injection and interface degradation for V_D lower than the $Si - SiO_2$ barrier height. It was found that the worst case degradation condition depends strongly on gate oxide thickness.

The results presented suggest that hot-carrier effects may continue to be important even when the supply voltages are reduced below the threshold energies for the physical processes responsible for these effects.

Zusammenfassung

Der Hot-Carrier-Effekt in n-Kanal Silizium-MOSFETs wird als Funktion der Drain- (V_D) und Gate-spannung (V_G) untersucht. Stoßionisation, Injektion in den Isolator und Degradation der $Si - SiO_2$ Grenzfläche lassen sich für qV_D (ballistische Maximalnergie) unterhalb der Energieschwelle für diese Prozesse beobachten. Detaillierte Untersuchungen werden im konventionellen (CON), einheitlich dotierten Kanal, im lateral asymmetrischen Kanal (LAC) und an vertikalen MOSFETs durchgeführt.

Bei hohem V_D zeigt der Substratstrom (I_{SUB}), der durch Stoßionisation erzeugt wird, eine negative Temperaturabhängigkeit. Bei niedrigem V_D beobachtet man eine positive Temperaturabhängigkeit. Eine detailierte Untersuchung dieser Phenomene wird präsentiert.

Stoßionisation in CON- und LAC-MOSFETs werden für V_D nahe und unterhalb der Bandgap-Spannung untersucht. In den $I_{SUB} - V_G -$Kurven von CON-MOSFETs sind zwei Maxima bei niedrigem V_D zu beobachten. Bei in Vorwärtsrichtung betriebenen LAC-MOSFETs sind drei Maxima sichtbar. Im Rückwärtsbetrieb sind Anzeichen eines zweiten Maximums zu beobachten. Umfangreiche experimentelle Daten über Kanallängen- und Temperatur-Abhängigkeit dieser anomalen Beobachtungen werden vorgestellt. Senkung der Temperatur von 300 K auf 77 K lässt das erste Maximum schwächer werden. Das zweite Maximum jedoch wird deutlicher sichtbar und erhöht sich mit einer Verkleinerung von L. Das bei Vorwärtsrichtung gepolten LACs auftretende dritte Maximum steigt, wenn L und die Temperatur verringert werden. Die experimentellen Daten werden auf der Grundlage der in der Literatur verfügbaren Monte Carlo Simulationsdaten analysiert. Diese bestätigen die Tatsache, dass der Ausläufer der Energieverteilung der Elektronen (Electron Energy Distribution = EED) und dessen Verbreiterung auf Grund kurzreichweitiger Elektron-Elektron-Wechselwirkungen (Short-Range Electron-Electron Interactions = SREEI) von der Gittertemperatur abhängen (Lattice Temperature Dependent Tail = LTDT). LTDT unterstützt das Erscheinen eines durch die Elektron-Phonon Wechselwirkung (Electron-Phonon Interaction = EPI) induzierten Ausläufers in der EED. EPI und SREEI können dazu führen, dass die Elektronen energetische Zustände jenseits des ballistischen Limits von qV_D einnehmen können. Es wird gezeigt, dass das anomale zweite Maximum in der $I_{SUB} - V_G -$Kurve auf SREEI zurückzuführen ist. Es ist festzustellen, dass SREEI in Langkanal-MOSFETs und bei sehr großen $V_G -$Werten schwächer ist. SREEI ist im Wesentlichen eine Wechselwirkung, die die aus dem elektrischen Feld gewonnene Energie neu verteilt. Die Zunahme von L und/oder V_G reduziert das Maximum des elektrische Feldes und reduziert dadurch den Einfluss von SREEI.

Unter Verwendung eindimensionaler selbstkonsistenter Poisson - Schrödinger Simulationen wird gezeigt, dass Quantisierung in der Inversionsschicht zu einer Zunahme der niedrigsten Energie der Elektronen nahe der Source-Seite des Kanals führen kann. Dies kann zu einem effektiven Energiegewinn in der Größenordnung von 40 meV oder mehr führen, abhängig von V_G.

Die zweidimensionale Drift-Diffusionsanalyse zeigt, dass in Vorwärtsrichtung betriebene LAC - MOSFETs eine zweite Hochfeldregion nahe Source aufweisen. Das dritte Maximum in den $I_{SUB} - V_G -$Kurven steht in Zusammenhang mit dieser Hochfeldregion. Da in diesem Fall die Source-Elektronen direkt in eine Hochfeldregion injiziert werden, können in diese Richtung betriebene LAC MOSFETs genutzt werden, um experimentell die von einigen MC Simulationsgruppen vorausgesagte Source EED aufgrund von langreichweitigen Elektron-Elektron Wechselwirkungen zu untersuchen.

Injektion ins Gate und Interface-Degradation für Drainspannungen niedriger als die $Si - SiO_2$ Barrierenhöhe werden ebenfalls gezeigt. Es zeigt sich, dass die "worst case" Degradationsbedingung stark von der Dicke des Gateoxides abhängig ist. Die präsentierten Ergebnisse lassen vermuten, dass Hot-Carrier-Effekte - wegen der ihnen zu Grunde liegenden physikalischen Prozesse - auch künftig von Bedeutung bleiben, wenn die Versorgungsspannung unter die Einsatzenergie gesenkt wird.

Key words **:** electron-electron interactions, electron energy distribution, electron-phonon interactions, hot-carrier, impact ionization, MOSFET, silicon, thermal tail

Contents

Nomenclature

α	impact ionization rate, in cm^{-1}
α^{∞}	impact ionization rate at infinite electric field, in cm^{-1}
β	ion implant tilt angle
$\Delta\Psi$	potential barrier between the source and the channel, in $Volt$
$\Delta\Psi_S$	difference in the surface potential between the quantum mechanical and classical cases for identical inversion layer charge density, in $Volt$
δg_m	% degradation in transconductance
δI_{CP}	% increase in charge pumping current due to stress
δI_D	% degradation in drain current due to stress
ΔV_D	incremental step in drain voltage, in $Volt$
ΔW_C	silicon to gate dielectric conduction band discontinuity, in $electron\,Volt$
ϵ_o	permittivity of free space, $8.854 \times 10^{-14}\ Farad\,.\,cm^{-1}$
ϵ_{Si}	relative permittivity of silicon, 11.9
$\vec{J_n}$	Current density, in $Ampere\,.\,cm^{-2}$
$E_{LATpeak}$	peak lateral electric field, in $Volt\,.\,cm^{-1}$
E_{LAT}	lateral electric field, in $Volt\,.\,cm^{-1}$
E_n^{crit}	critical value of E at which electrons initiate impact ionization, in $Volt\,.\,cm^{-1}$
E_{sat}	critical E_{LAT} for velocity saturation of the electrons, in $Volt\,.\,cm^{-1}$
g_m	transconductance, dI_D/dV_G, in $Ampere\,.\,Volt^{-1}$
G_n^{II}	Impact ionization generation rate for electrons, in $cm^{-3}\,.\,sec^{-1}$
I_{CP}	charge pumping current, in $Ampere$
I_D	drain current, in $Ampere$
I_G	gate current, in $Ampere$

$I_{SUBpeak}$	I_{SUB} corresponding to the maxima in I_{SUB} vs V_G plots, in $Ampere$
I_{SUB}	substrate current, in $Ampere$
k	Boltzmann constant, 8.62×10^{-5} $electron\,Volt\;Kelvin^{-1}$
L	drawn channel length, in μm
L_{eff}	effective channel length determined by electrical methods, in μm
M	impact ionization quantum yield given by I_{SUB}/I_D
n	volume density of inversion layer electrons, in cm^{-3}
N_{INV}	inversion layer electron density, in cm^{-2}
q	elementary charge, 1.60218×10^{-19} $Coulomb$
T	temperature, in $Kelvin$ or $^oCentigrade$
T_E	effective temperature, in $Kelvin$
T_L	lattice temperature, in $Kelvin$
t_{OX}	thickness of gate oxide, in nm
V_{Dmin}	minimum V_D for which bell shaped I_{SUB} vs V_G plots could be measured, in $Volt$
V_{Dsat}	drain voltage at which the drain current saturates in I_D vs V_D, in $Volt$
V_D	drain voltage, in $Volt$
V_{Gpeak}	gate voltage corresponding to $I_{SUBpeak}$ in I_{SUB} vs V_G plots, in $Volt$
V_{GT}	gate over-drive given by $V_G - V_T$, in $Volt$
V_G	gate voltage, in $Volt$
V_{SUB}	substrate voltage, in $Volt$
V_T	threshold voltage, in $Volt$
V_{XOVER}	cross-over voltage, V_D at which I_{SUB} or M is independent of T, in $Volt$
W	energy, in $electron\,Volt$
W_C	bottom of the conduction band
W_G	bandgap energy, in $electron\,Volt$
W_K	average kinetic energy of electrons, in $electron\,Volt$
BTE	Boltzmann Transport Equation
CON	CONventional (MOSFET)

DIBL	Drain Induced Barrier Lowering
EED	Electron Energy Distribution
EEI	Electron-Electron Interaction
EPI	Electron-Phonon Interaction
HET	High Energy Tail
ILQ	Inversion Layer Quantization
IV	current - voltage characteristics
LAC	Laterally Asymmetrical Channel (MOSFET)
LEM	Lucky Electron Model
LREEI	Long-Range Electron-Electron Interaction
LTDT	Lattice Temperature Dependent Tail
MBD	Maxwell-Boltzmann Distribution
MBE	Molecular Beam Epitaxy
MC	Monte-Carlo
MOSFET	Metal Oxide Semiconductor Field Effect Transistor
RIE	Reactive Ion Etching
SIMS	Secondary Ion Mass Spectroscopy
SREEI	Short-Range Electron-Electron Interaction
TEM	Transition Electron Microscopy
UCB	University of California Berkeley

Chapter 1

Introduction

1.1 The Problem

Hot-carrier issues have been of serious concern for Complementary-Metal-Oxide-Silicon (CMOS) technologies for the last three decades [1]. Hot-carriers cause impact ionization which leads to substrate current and device breakdown in bulk CMOS devices, and floating body effects like kink and hysteresis in silicon-on-insulator (SOI) technologies. Injection of hot-carriers into gate dielectric causes a gate current and leads to degradation of drain current and transconductance, and changes in threshold voltage of the devices. Hot-carrier injection is also used for programming flash memory devices. Hot-carrier injection at operating voltages (in contrast to programming bias) raise serious concerns about long-term data retention reliability of such devices.

Aggressive scaling of device dimensions have been an enabling factor for CMOS devices to keep the lead in large scale integrated circuits (LSI) [2]. Even in a constant field scaling, the peak electric field in the device is increasing because of an increase in doping density. In generalized scaling (which is more common), the channel length is scaled more aggressively than the supply voltage, and this compound the hot-carrier issues.

To cause impact ionization and to surmount the silicon - silicon dioxide barrier (gate injection) the electrons must have minimum threshold energies which are bandgap energy (W_G) and 3.1 eV respectively. It was believed that hot-carrier effects will disappear once for ever when the supply voltages are reduced below these thresholds.

However there have been many reports of hot-carrier effects in n-channel silicon Metal-Oxide-Semiconductor Field-Effect-Transistors (nMOSFET) for supply voltages below the thresholds. For sub-100 nm devices, silicon dioxide will be replaced by higher permittivity dielectrics as gate dielectric. All the candidate materials have a significantly lower threshold for electron injection from silicon to dielectric [3]. Hot-carrier injection can be expected to be higher for such systems. In this context it is important to study hot-carrier effects at low supply voltages. A detailed understanding of the underlying physics is required to address the issues concerned. Specifically, (i) the presence of secondary energy gain mechanisms besides field heating (ii) methods to experimentally identify them and assess their strength (iii) impact of device scaling on them (iv) their impact on device performance and reliability, are issues that need attention. Such investigations will lead to better understanding of physics and accurate modeling.

1.2 State of the Art

Low voltage hot-carrier issues have been extensively investigated in the literature as demonstrated in chapter 2. Experimental data on almost all aspects of hot-carrier effects, namely impact ionization, gate injection and interface damage are reported for supply voltages lower than the threshold voltages for the respective processes. At low voltages, a reversal in the temperature dependence of substrate current (cross-over effect) is also reported.

However, many of the experimental investigations were aimed at checking the lowest supply voltages at which hot-carrier effects can be observed. Some investigations also tried to verify the applicability of empirical high voltage reliability projection techniques at low voltages. However there is still considerable controversy regarding this point. Experimental investigations of hot-carrier effects near respective thresholds are also marred by interfering leakage currents and low sensitive instrumentation employed in many cases. This had lead to reports of inconsistent data. There are very rare experimental attempts to understand the physical mechanisms involved.

Theoretical analysis based on simplifying assumptions have considerably advanced the theory of hot-carriers at low voltages. For example, absorption of optical phonons by electrons has been advanced to explain the possibility of electrons in MOSFETs with energy greater than the applied drain voltage. The resulting thermal tail in electron energy distribution (EED) was thought of as the reason for the cross-over effect. Sophisticated simulation using Monte-Carlo (MC) methods have also supported the idea of a thermal tail to EED. However, MC simulations have shown that the cross-over effect is due to an increase in the threshold energy for impact ionization. MC simulations have also proposed short and long-range electron-electron interactions (EEI) as mechanisms populating the EED beyond the applied drain bias.

Even though the idea of a thermal tail to EED is nearly two decades old, there seems to be no experimental proof for it. The role of short-range EEI is experimentally verified. But its strength is still debated. The role of long-range EEI on EED is still uncertain.

Even though MC simulations combined with experimental data have verified the role of short-range interactions in extending the tail of EED beyond the applied voltage, its inherent noise problems have prevented researchers from identifying experimental signatures of secondary energy gain mechanisms like EEI. Finer, but important, details like channel length and gate bias dependence of EEI broadening are still matters of guess work. Whether EEI will have any serious implications for device reliability is controversial.

1.3 Scope of the Present Work

In this work, first we have addressed the issue of cross-over effect in substrate current of conventional n-channel devices. Deficiencies in the understanding of cross-over effect are pointed out. Channel length and gate bias dependencies of cross-over effect in deep-sub-micron devices are experimentally investigated. We provide a graphical interpretation of the present understanding of cross-over effect. Two-dimensional drift-diffusion analysis is combined with the graphical method to interpret the experimental data. The analysis establish the utility of electric field as an indicator of various regions of the electron energy distribution.

Impact ionization in conventional n-channel MOSFETs for drain voltages near the bandgap voltage ($\sim 1.1\,V$) is investigated using substrate current as monitor. The incomplete understanding of carrier heating beyond the applied bias is pointed out. We observe anomalous substrate current versus gate voltage plots with two peaks as the drain bias approaches the bandgap voltage. Channel length dependence of this behavior was studied. The presence of a lattice temperature dependent tail (LTDT) in EED is experimentally verified. Based on the experimental observations and one-dimensional quantum mechanical simulations, we have identified inversion layer quantization as an energy gain mechanism. Temperature sensitivity of the thermal tail has been used to assess the drain voltage below which the tail is important for impact ionization. The presence of the second peak in substrate current versus gate voltage plots is correlated to short-range EEI. Channel length dependence of the second peak is explained based on two-dimensional drift-diffusion simulations. Gate bias dependence of short-range EEI is established, and shows that it does not follow a monotonous positive gate bias dependence as is widely assumed. We show that, impact of short-range EEI increases with down scaling of channel length.

Impact ionization in laterally asymmetric n-channel MOSFETs were also investigated. These devices have a heavy boron doping at one end of the channel. They can be operated in two modes, forward mode in which the highly doped channel region is near the source junction, and reverse mode in which the highly doped channel region is near the drain junction. Anomalous substrate current versus gate voltage curves with three peaks are presented for the forward mode of operation. In the reverse mode, only one peak was observed. However we identify features that suggest a second peak in this case as well. A detailed study of the channel length dependence of these features are presented for both forward and reverse modes of operation. These results were also compared with that obtained for the conventional devices. From two-dimensional drift-diffusion simulations, it was found that, for the forward mode of operation, there are two peaks in the lateral field distribution whereas in the reverse mode, there is only one peak. The first and third peaks in the substrate current versus gate voltage in the forward mode are correlated to field heating in the two high field regions. It is shown that the second peak is due to short-range EEI in the drain side high field region. We have discussed the differences in carrier heating at the source and drain ends of the channel. We propose the forward mode of operation of these devices as a suitable testing tool to investigate the role of long-range EEI on the tail of EED.

We also present experimental data on the impact of hot-carriers on device operation and reliability. Kink effect is demonstrated in vertical floating body devices for drain voltages less than 1.1 V. We also demonstrate gate injection for drain bias as low as 2.2 V. Hot-carrier degradation was observed in lateral conventional channel devices for drain voltages nominally below the silicon-silicon dioxide conduction band discontinuity. Even though signature of short-range EEI could be seen in the substrate current data at low drain voltages, the degradation does not increase monotonously with increasing gate bias as reported in the literature.

1.4 Organization of the Thesis

In chapter 2, we present a literature review of low supply voltage hot-carrier issues in n-channel MOSFETs. A detailed channel length and gate bias dependence study of crossover phenomenon in conventional n-channel MOSFETs is presented in chapter 3. Chapter 4 treats impact ionization in conventional n-channel devices at drain voltages close to and below bandgap voltage. A detailed investigation of impact ionization at low voltages in laterally asymmetric n-channel MOSFETs is presented in chapter 5. In chapter 6, operational and degradation issues related to hot-carrier effects in vertical and lateral devices are presented.

An overview of the process flow for the devices used in chapters 3, 4 and 5 is given in appendix A, along with a comparison of simulated doping profiles, terminal characteristics and properties of source and drain contacts. Appendix B provide the process flow and manufacturability of vertical MOSFETs discussed in chapter 6. Appendix C provide information about the measurement techniques employed.

Chapter 2

A Review of Low Voltage Hot-Carrier Issues in nMOSFETs

In this chapter a literature review is presented to highlight hot-carrier effects at low voltages in n-channel MOSFETs. We point out the deficiencies in the understanding of the physics of low voltage hot-carriers and thereby set the back ground for the work presented in this thesis. We concentrate on n-channel devices and hence on hot-electron issues. This is justified because hot-carrier issues are less severe in p-channel MOSFETs. The holes are much heavier than the electrons and hence the energy gained by them during transport is smaller than that by electrons. For injection into SiO_2, holes face nearly $1\,eV$ higher barrier than electrons.

2.1 Hot-Carrier Effects in n-channel MOSFETs

Hot-Carrier effects in silicon n-channel MOSFETs are schematically shown in figure 2.1 [4]. Hot-electrons can produce electron-hole pairs by impact ionization. In the extreme case this leads to device break down. The generated holes flow towards the substrate and can be measured as a substrate current (I_{SUB}). I_{SUB} is extensively used for the investigation of hot-carrier effects.

Those electrons which have energy higher than the silicon-dielectric conduction band discontinuity (ΔW_C) may get injected into the gate causing a gate current (I_G) to flow. This is an important process for flash memory programming and retention reliability.

Hot-electrons can cause interface damage which effect the device performance parameters like drain current (I_D), transconductance (g_m) and threshold voltage (V_T). To ensure proper device operation, these parameters have to remain within given limits during the specified lifetime of the device.

Hot-carrier effects are threshold processes and it was considered that they will not pose significant problems when the device operating voltages are scaled down below the thresholds. However these expectations do not seem to be well founded.

For sub-100 nm devices with high relative permittivity gate dielectrics, ΔW_C is much smaller than that of the $Si-SiO_2$ system [3] and hence hot-carrier injection and interface degradation may be a more serious problem for these futuristic devices.

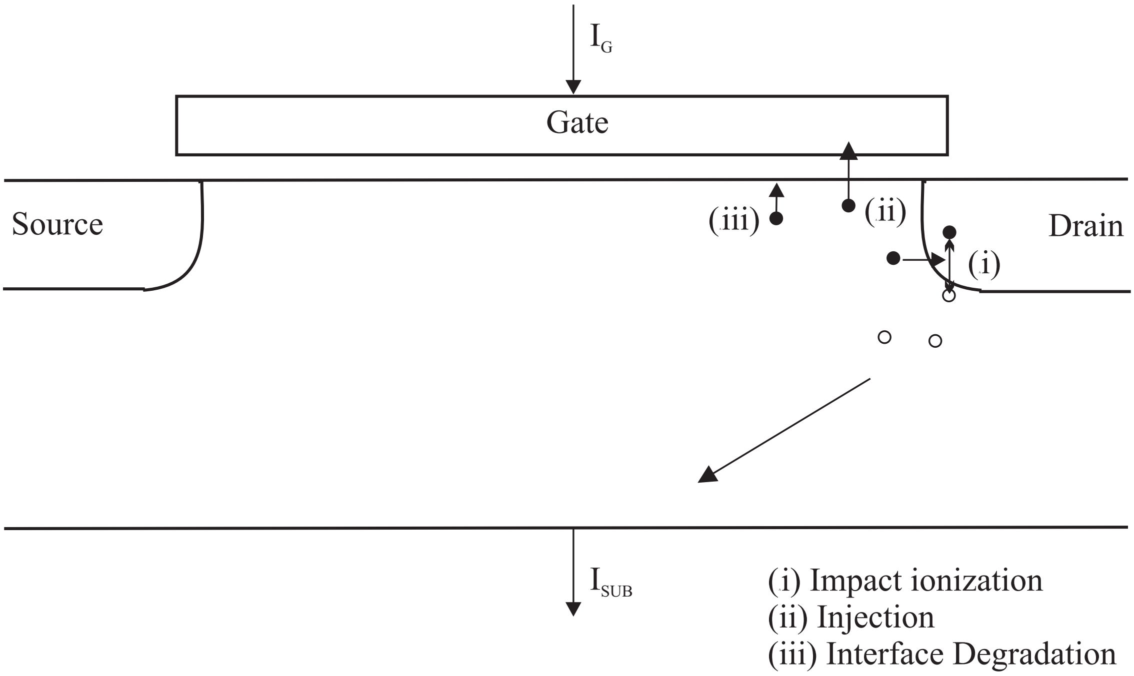


Figure 2.1: Schematic illustrating hot-carrier effects in n-channel MOSFETs. Filled circles represent electrons and open circles represent holes.

2.2 Models of Carrier Heating

In this section various modeling approaches to carrier heating in semiconductors is briefly reviewed.

2.2.1 Heating by Electric Field

Early attempts to understand hot-carrier effects, especially impact ionization, in semiconductor devices were based on an electric field perspective [5, 6, 7]. This approach is still the most widely used one for modeling of hot-carrier effects. One reason for the popularity of this approach is because, consistent solutions of drift-diffusion approximation of the Boltzmann Transport Equation (BTE) and Poisson equation provide electric field distributions in addition to carrier concentration distributions [8]. Numerical solutions of drift-diffusion equations have good and fast convergence and hence are less time consuming than physically more accurate methods like Monte-Carlo simulations.

From an electric field perspective, impact ionization is characterized by an impact ionization rate, α, which is defined as the number of electron-hole pairs generated by a hot-carrier in unit length. The relevant impact ionization generation rate equations for hot-electrons can be written as

$$G_n^{II} = \alpha_n \frac{|\vec{J}_n|}{q} \tag{2.1}$$

where, G_n^{II} is the generation rate, $\vec{J}_n$ is the current density and q the elementary charge and

$$\alpha_n = \alpha_n^{\infty} \exp(-(\frac{E_n^{crit}}{E})^{\beta_n}) \tag{2.2}$$

where, the prefactor is the impact ionization rate for infinite electric field, E the electric field in the direction of current flow, E_n^{crit} is the critical electric field for electrons to cause impact ionization, and the exponent β_n varies between 1 and 2 [5, 6, 7]. Values of E_n^{crit} found in the literature varies from 10^6 to $5.87\times10^6\ Vcm^{-1}$ and α_n^{∞} from 6.2×10^5 to $3.8 \times 10^6 cm^{-1}$ (for a compilation of literature values, refer to Selberherr [8].

Shockley [7] related G_n^{II} to the probability that an electron travels enough length through silicon without phonon scattering to gain the threshold energy for impact ionization. Shockley's model was termed the "lucky electron model" (LEM) for this reason. The electric field based models discussed so far were termed by Shockley as empirical because "a theoretical model should take into account the energy-band structure for energies greater than 1 eV (for silicon) from the band edges and should make use of the appropriate effective masses for hot-carrier effects."

When E is varying rapidly and also for low E values, the models based on local values of E overestimate impact ionization [9]. Impact ionization at any space coordinate will depend not only on the value of E at that particular location but also on its spacial distribution.

Hu et al. [4] applied LEM to the hot-carrier problems in nMOSFETs. Impact generated I_{SUB}, hot-electron emission current into the gate dielectric (I_G) and interface damage were correlated to the peak lateral electric field ($E_{LATpeak}$) through LEM. $E_{LATpeak}$ was related to bias voltages and device parameters. Hot-carrier life time prediction algorithms based on this model are widely used [10].

The models discussed so far have the consequence that the maximum energy gained by any electron in a MOSFET is limited by the applied drain voltage (V_D). This is because the current is flowing along the direction of the lateral field. The maximum energy gained by any single electron is given by,

$$\begin{aligned} W &= -q \int_0^L \vec{E}.\vec{dl} && (2.3) \\ &= -q.(V_D + \Delta\Psi) && (2.4) \end{aligned}$$

where L is the channel length and $\Delta\Psi$ is the small electrostatic barrier between the source and the channel [11, 12, 13]. If we neglect $\Delta\Psi$, there should not be any impact ionization in silicon devices for qV_D less than the impact ionization threshold energy, which is equal to the bandgap energy (W_G) [7, 14], and no gate currents for qV_D less than ΔW_C.

2.2.2 The Energy Balance Perspective

In short channel nMOSFETs, the lateral electric field (E_{LAT}) is very high and the thermal equilibrium condition assumed in drift-diffusion formulations need not be valid over a significant portion of the channel. The electrons will have an effective temperature (T_E) that is much higher than the lattice temperature (T_L). Carrier temperature gradient leads to thermal diffusion currents [15]. This can be accommodated by consistently solving the energy balance equations along with the drift-diffusion equations and the Poisson equation. Energy balance equations include energy lost through phonon emission. The impact ionization generated I_{SUB}, and I_G can be modeled as functions of carrier temperature [15, 16, 17]. Energy conservation equations accommodate nonlocal nature of carrier heating. However, the details of the band structure are not taken into consideration. Further, this model assumes that the electron energy distribution (EED) can be represented by a Maxwell-Boltzmann distribution (MBD) with a single effective temperature.

Since the EED is represented by a MBD with a single T_E, it will extend much beyond the applied V_D. This is considered an inherent short coming of the energy balance formulations [17].

2.2.3 The Monte-Carlo Method

State-of-the-art approach to carrier transport in semiconductor devices is to solve BTE using Monte-Carlo (MC) techniques [18, 19, 20]. In MC, trajectories of one or more carriers is traced at the microscopic level in a given device structure subject to the action of electric fields, device geometry and various scattering mechanisms. Carrier flight and scattering are stochastically treated in accordance with probabilities describing the physical processes. Consistent MC solutions also solve the Poisson equation. The outputs of MC are carrier energy distributions. Since the carriers are treated as particles, and BTE is a classical formulation, MC is essentially a classical approach to simulation.

The material physics can be correctly modeled by including full-band structure [21]. However, the band structure models used by various MC groups are different. For example, Fischetti et al. [22] and Bude et al. [12] employ full-band structure obtained using pseudopotential method, whereas Ghetti et al. [23] use an analytical band structure. The probabilities describing scattering mechanisms are determined empirically to fit experimental observations. For example, Cartier et al. determined impact ionization rate as a function of carrier energy by fitting empirical models to soft x-ray photoemission spectroscopy data [24]. Bude et al. [25] used impact ionization rates evaluated theoretically. Ghetti et al. [23] used the impact ionization rates from Bude et al. Since the band structures used by both the groups are different, Ghetti et al. have fine tuned deformation potentials to match experimental quantum yield data.

Since MC is a stochastic approach, the number of carriers to be simulated must be sufficiently high to obtain reliable statistics. Various statistical enhancement schemes and iteration schemes employed in MC simulations also result in varying degrees of simulation noise. Specifically C. Jungemann and B. Meinerzhagen [26, 27] warn that "without proper analysis of the stochastic error it is not possible to assess the accuracy or efficiency of MC device simulations and misleading results might be obtained". This problem is prohibitively serious in MOSFETs operating in the subthreshold regime, due to the low number of inversion layer carriers, and no reliable results can be obtained for this regime [28].

Despite the inconsistency in the models used by various groups and the inherent noise problems, MC method is fairly established and applied to investigate inversion layer transport at the limits of MOSFET scaling [29]. The technique has also been applied to identify novel flash memory programming mechanisms [12], and to investigate hot-carrier reliability issues [23, 30]. The technique is highly suited to study processes with energy thresholds since the outcome of the simulations is EED. In the following sections, we will review results published by MC groups on MOSFET operation to understand the physics of low voltage hot-carrier effects.

2.3 Low Voltage Hot-Carrier Effects in nMOSFETs

In this section, a review of the reports of hot-carrier effects found in the literature is given. Cross-over effect in impact generated I_{SUB}, impact ionization and interface degradation for voltages below threshold voltages for the respective processes are discussed.

At high V_D, inversion layer electrons in an nMOSFET can gain sufficiently high energy and cause impact ionization. The generated secondary electrons flow towards the drain and the holes flow towards the substrate contact [31]. The hole current measured at the substrate (I_{SUB}) can be used to study impact ionization in nMOSFETs. I_{SUB} vs gate voltage (V_G) curves have a characteristic bell shape [32, 33].

2.3.1 The Cross-over Effect

I_{SUB} in MOSFETs for large V_D shows a negative temperature dependence (increases as the temperature is decreased and vice versa). This is because of the less frequent energy losing electron-phonon scattering events and hence higher average energy of the electrons [10].

Eitan et al. [11] studied impact ionization in n-channel MOSFETs of channel length $2.7\,\mu m$ with gate oxide thickness of $32.5\,nm$ for V_D down to 1.05 V and reported a positive temperature dependence of I_{SUB} for $V_D < 1.7\,V$. This was contrary to the observations till then. The phenomenon has since been studied by many researchers [23, 34, 35, 36, 37, 38, 39] and has lead to a better understanding of hot-carrier transport at low V_D.

Henning et al. [34] christened the phenomenon as "cross-over" effect and termed the V_D at which I_{SUB} is independent of temperature as the "cross-over voltage" (V_{XOVER}). For $V_D < V_{XOVER}$, I_{SUB} increases with increase in temperature and for $V_D > V_{XOVER}$, it decreases with increase in temperature. The value of V_{XOVER} reported in the literature varies from 1.75 to 2.6 V [11, 23, 35, 36, 37]. Henning et al. [34] reported that V_{XOVER} increases with channel length. Essani et al. [36] found that V_{XOVER} decreases with increasing V_G.

The experimental data reported in the literature on cross-over effect are summarized in table 2.1. Research groups other than cited in the table have also reported a reduced I_{SUB} at low V_D for low temperatures, for example [40]. The data given in table 2.1 is selected on the basis that, V_{XOVER} values are reported.

For quite some time it was speculated that the cross-over effect is due to the presence of a thermal tail in EED [11, 34]. Thermal tail means that the EED has an extension beyond qV_D, with a slope inversely proportional to the lattice temperature. Since impact ionization is caused by electrons having energy greater than W_G, the tail also contribute significantly to the process as qV_D approaches W_G. The thermal tail is greatly suppressed as the temperature is reduced, and hence I_{SUB} has to decrease with

Table 2.1: Summary of representative data on cross-over effect reported in the literature.

Ref.	L_{eff} (μm)	t_{OX} (nm)	V_{XOVER} (V)
[11]	2.7	25	1.75
[34]	33 to 0.95	38.5	2.6 to 1.8
[35]	5 to 0.09	4.8	2.3*
[36]	0.4 to 0.2	12	V_{GT} dependent
[23]	0.22	12	2

* for $L_{eff} \leq 0.14\,\mu m$ I_{SUB} is reported to be consistently lower at 77 K than at 300 K for V_D upto 3V.

temperature at low V_D.

Essani et al. [36, 37] employed I_G measurements on floating gate structures along with I_{SUB} measurements for V_D down to $1.4\,V$, which is well below V_{XOVER}. Even though I_{SUB} showed a cross-over, I_G did not show any cross-over. Since for this range of V_D, I_G is caused by injection of the electrons occupying the tail of the EED into SiO_2 from the channel, it should also show a cross-over if the thermal tail was behind the cross-over in I_{SUB}. Sano et al. [39] employing MC simulations argued that the widely reported V_{XOVER} of 2 V can not be explained by a thermal tail. The contribution of the field heated part of the EED, from $W_G \sim 1.1\,eV$, to $qV_D = 2\,eV$, to I_{SUB} would be much higher than that from the thermal tail for the temperature range usually investigated (77 to 300 K). This is because the effective temperature of the field heated part is much higher than T_L. Thermal tail alone could explain cross-over effect if qV_{XOVER} is close to W_G.

Fischetti and Laux, employing MC simulations, proposed that the cross-over effect is due to the increase in W_G of silicon as the temperature is reduced [38]. W_G increases by about 40 meV when the temperature is reduced from 300 to 77 K [41, 42, 43]. MC simulations of Sano et al. [39] and Ghetti et al. [23] have since supported such a model. Ghetti et al. [23] could also reproduce the experimental I_{SUB}/I_D, referred to as quantum yield (M) hereafter, using their simulation model for n-channel MOSFETs of effective channel length $0.22\,\mu m$ and having gate oxide of thickness $10\,nm$. However, Sano et al. used a $65\,meV$ increase in W_G in their simulations, which is much higher than the widely accepted value of $40\,meV$.

A careful look at table 2.1 reveals that : (i) V_{XOVER} varies from 1.75 to 2.6 V for various technologies. (ii) the bias conditions used for the determination of V_{XOVER} are different. As is evident in the data in [36], V_{XOVER} may depend on bias conditions. (iii) For ultra-short channel devices, I_{SUB} is consistently low at low temperature upto large V_D values.

The channel length and gate voltage dependencies of V_{XOVER} remain unexplained. Also there is insufficient data in the literature on devices with ultra thin oxides.

2.3.2 Sub Bandgap Impact Ionization

From first order theory one would expect no impact generated I_{SUB} for $qV_D < W_G$. This is because, the net movement of inversion layer electrons are along the channel direction and the total potential drop experienced by them is qV_D.

Eitan et al. [11] reported bell shaped I_{SUB} vs V_G plots for V_D down to 1.05 V, for $L = 2.7\,\mu m$ at 300 K. Tam et al. [44] reported I_{SUB} for V_D down to $0.85\,V$ at 300 K. Chung et al. [45] reported I_{SUB} for V_D down to $0.7\,V$ at 300 K. The last two papers have reported I_{SUB} vs V_D curves. I_{SUB} consists of impact generated hole current and drain junction leakage current. At very low V_D, the former component may be comparable or lower than the later and hence it can not be unambiguously said that the data are indications of sub-bandgap impact ionization.

Manchanda et al. [46] reported bell shaped I_{SUB} vs V_G plots for V_D down to $0.6\,V$ at 170 K and $0.8\,V$ at 300 K. There is an inconsistency with the reported cross-over effects in this case. Since at such low V_D, I_{SUB} is reported to decrease with temperature, for a given measurement resolution, we would expect bell shaped I_{SUB} vs V_G for lower V_D at 300 K than at 170 K. According to the authors, "we observed simultaneous reductions in the threshold voltage for impact ionization and the impact ionization current at low temperatures". One of the reasons for this obvious discrepancy may be the dominance of the component of drain junction leakage in I_{SUB}, which is the thermal generation current of the reverse biased drain-substrate junction and hence decreases with temperature. They also reported an increase in the minimum V_D at which impact ionization could be measured (V_{Dmin}), as the channel length was increased.

Koyanagi et al. [40] reported bell shaped I_{SUB} vs V_G for V_D down to $1\,V$ at 300 K. They also reported a decrease in I_{SUB} as the temperature was reduced to 77 K. Balestra et al. [47] reported bell shaped I_{SUB} vs V_G data for V_D down to $1\,V$ at 300 K and $1.2\,V$ at 77 K. At 77 K they also observed an anomalous increase in the V_G at which I_{SUB} peaks (V_{Gpeak}) as the V_D was reduced. However this behavior was not explained.

A. Hori et al. [48] investigated low voltage impact ionization in devices with gate oxides of thickness 4 and 8 nm. They could measure bell shaped I_{SUB} vs V_G for V_D down to $0.9\,V$ for the thinner oxide device and down to $0.8\,V$ for the thicker oxide device. An increase in V_{Gpeak} at low V_D can be discerned in their data even though they have not noted this in the paper.

Odanaka and Hiroki [49] compared the reliability performance of conventional and laterally asymmetric channel devices of channel lengths $0.15\,\mu m$. They could measure bell shaped I_{SUB} vs V_G for V_D down to $1V$. Anomalous increase in V_{Gpeak} is discernible in their data as well, even though they have not noted it in their paper.

Saraya et al. [50] reported observation of kink in the output characteristics of SOI devices for V_D down to $0.75\,V$.

Except for Eitan at al. [11], none of the above reports have considered why and how there can be hot-carriers with energy higher than the applied drain bias. Emphasis in most of these studies was whether impact ionization can be observed for $qV_D < W_G$, not on the physical mechanisms responsible. Eitan et al. suggested that the EED has a thermal tail because the EED keep a "memory" of its initial equilibrium distribution. This point will be considered in detail later.

2.3.3 Sub-barrier Electron Injection into the Gate Dielectric

When direct tunneling is negligible and oxide field is low so that Fowler-Nordheim tunneling can be ignored, only those electrons having energy higher than ΔW_C get injected into the dielectric. From first order considerations we would expect no I_G for

$qV_D < \Delta W_C$. For the $Si - SiO_2$ system, we would expect no injection for $V_D < 3.1\,V$.

Ricco et al. [51] measured significant charging of the floating gate of floating gate nMOSFETs for V_D down to 1.4 and 1.8 V at 77 and 300 K respectively. They attributed it to hot-electron injection. Similar measurements were also reported by Sangiorgi et al. [52] and Essani et al. [36]. Gate oxide thicknesses in all these case were more than 10 nm. Chung et al. [45] reported gate currents for V_D down to 1.8 V using sensitive direct current measurement techniques.

ΔW_C can be smaller than the theoretical values due to the presence of charges at the interface [43]. However the lowest value for $Si - SiO_2$ is about 2.5 eV [53]. This means that I_G reported at such low voltages as in the previous paragraph are caused by electrons having energy much higher than the applied V_D.

Electron injection at such low V_D has serious consequence for long-term retention reliability of flash memory cells. V_D values discussed in the previous paragraphs lie in the operating voltage range of such devices. Long term operation of the devices at such voltages can change a stored “one” (no charge on the floating gate) to “zero” by cumulative low voltage electron injection [23].

2.3.4 Hot-Carrier Reliability at Low Drain Voltages

There have been many microscopic models of hot-carrier degradation proposed in the past. A review of them is interesting from the perspective of threshold energy for degradation.

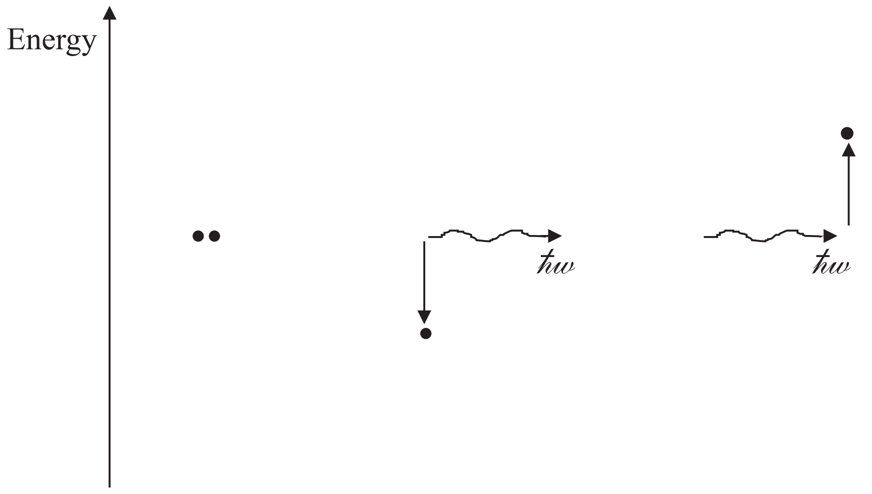
Hot-electron model suggested that energetic electrons break $Si-H$ bond to produce trivalent silicon (interface traps) and interstitial hydrogen atom. Threshold energy associated with the process is equal to bond energy plus the barrier energy, about 3.7 eV [4].

According to trapped hole recombination model, hot holes are injected into the dielectric and get trapped. Subsequently they capture an electron and recombine. The energy released in this process breaks $Si-H$ bonds [54]. This process is limited by hot hole injection and with a valance band discontinuity of about 4.1 eV for the $Si - SiO_2$ system [43] has a higher threshold than the hot-electron injection model.

Bude et al. [30] investigated threshold energy for hot electron induced interface state generation using MC simulations. MC simulations were used to obtain EED. An empirical interface state generation model which has a tunable threshold energy was used to correlate the simulated EED to measured degradation data. Best fit of model to experiment was found for a threshold of 3.5 eV for interface state generation. Recently, Mu et al. [55] applying an extension of LEM to degradation data, found a value of 3.2 eV for the threshold energy.

K. Hess et al. [53] suggested that the breaking of $Si - H$ bonds is through vibrational excitations. The bonds can also be broken by multiple vibrational excitations. This model was prompted by the improvement of hot carrier robustness of interfaces annealed in deuterium compared to those annealed in hydrogen [56, 57]. Since the bonding energy of $Si - H$ and $Si - D$ are the same, a chemical picture should give identical interface qualities for both the isotopes. Multiple vibrational excitations, if the real reason for the improved robustness of deuterium annealed interfaces, can make the process a soft threshold one.

Takeda et al. [58] reported degradation of $Si-SiO_2$ interface for V_D down to 2.5 V.



(i) electrons before interaction

(ii) electron relaxation by optical phonon emission

(iii) electron excitation by optical phonon absorption

Figure 2.2: Schematic illustrating EPI as a process that can extent the EED tail beyond the applied bias [62]. (i) monoenergetic electrons having energy equal to the applied bias, assumed for ease of understanding, before interactions. (ii) one of the electrons relax by emitting an optical phonon. (iii) Another electron absorb the emitted phonon extending the EED beyond the applied bias.

Rauch et al. [59] reported measurable degradation for V_D down to 2 V. Mahapatra et al. [60] deported degradation down to 1.9 V.

Even though threshold energy for the degradation process is controversial, high energy electrons are bound to cause greater damage. From this perspective it is important to know carrier heating beyond applied biases for deep-sub micron devices.

2.4 Carriers with Energy Greater than qV_D

In this section, possible mechanisms that populate the EED beyond the applied V_D are reviewed. Most of the discussion center around simulation results published by MC groups.

2.4.1 Electron-Phonon Interactions as an Energy Redistribution Mechanism

Eitan et al. [11], assuming impact ionization as the only scattering in the pinch-off region of MOSFETs, derived an expression for I_{SUB} that depends exponentially on T_L. They argued that EED keeps “memory” of its source side equilibrium condition. However, no physical explanation was given.

Mahan [61] analytically solved BTE in silicon in one dimension, accounting for ionized impurity scattering and electron-phonon interactions. Electrons with MBD launched into a uniform field emerges with a distribution that has two parts. For

$W < qV$, the distribution was described by MBD with $T = T_E$, where T_E is the effective temperature. For $W > qV$, the distribution was described by an MBD with $T = T_L$, where T_L is the lattice temperature. Since the maximum energy that can be gained by the electrons from the field is qV, that part of the EED beyond qV is called the tail. When the tail has an effective temperature equal to the lattice temperature it is called a thermal tail.

Analytical treatments of Lacaita [63] also predicted a thermal tail. The explanation for the presence of the thermal tail according to Lacaita, as understood by the present author, is as follows. An electron ensemble which is in thermal equilibrium with the lattice follows a distribution which has a tail that is well described by MBD with $T = T_L$. The energy gained by the electron ensemble from the lattice by phonon absorption is balanced by the energy lost to it by phonon emission. When a high electric field is applied, the rate at which the electrons gain energy from the field exceeds the electron-optical phonon scattering rate multiplied by phonon energy. The electron ensemble is no more in equilibrium with the lattice. The maximum energy that any electron in the ensemble can gain from the field is qV. Now we consider those electrons which have energy equal to qV, as in figure 2.2(i). One of the electrons losses part of its energy by emitting an optical phonon, figure 2.2(ii). Of the various possibilities available to the emitted phonon, we consider the case of it being absorbed by another electron as shown in figure 2.2(iii). The result of the sequence of the processes depicted is an extension of the distribution beyond qV. Step (iii) in the process can at best have the same rate as the step (ii), because the inverse condition would imply cooling of the lattice. The electrons in an interaction involving a phonon can either emit or absorb a phonon. We assume that the events have equal probabilities. For the electrons beyond qV edge, this would mean a quasi-equilibrium with the lattice in the sense that the phonon absorption and emission are balanced. Consequently the distribution beyond qV has an effective temperature equal to the lattice temperature.

MC simulations have supported the presence of a thermal tail in the EED [23, 38, 39, 64, 65, 66, 67, 68, 69].

The energy exchanged in EPI are limited to the energy of optical phonons. In silicon, the highest optical phonon energy is $63\,meV$ [43].

A minor comment about the nomenclature is in order. MC simulation groups refer to EPI as an energy gain mechanism. The phonon absorbed by any electron in the interaction was emitted by some other electron which in turn gained this energy from field heating. Describing the mechanism as an energy redistribution mechanism is more appropriate and closer to the physical process involved and hence the title of the subsection. Electron energy is redistributed with the phonons acting as intermediary.

2.4.2 Electron-Electron Interactions as an Energy Redistribution Mechanism

Ensemble MC simulations have also predicted EEI as a major energy gain mechanism that would extend the distribution much beyond the qV limit [23, 38, 67, 68, 69]. Two kinds of EEI are identified, namely a short-range component and a long-range component. Except in the work of Fischetti and Laux [38, 70, 71], the long-range component is not explicitely included in any of the MC codes reported in the literature.

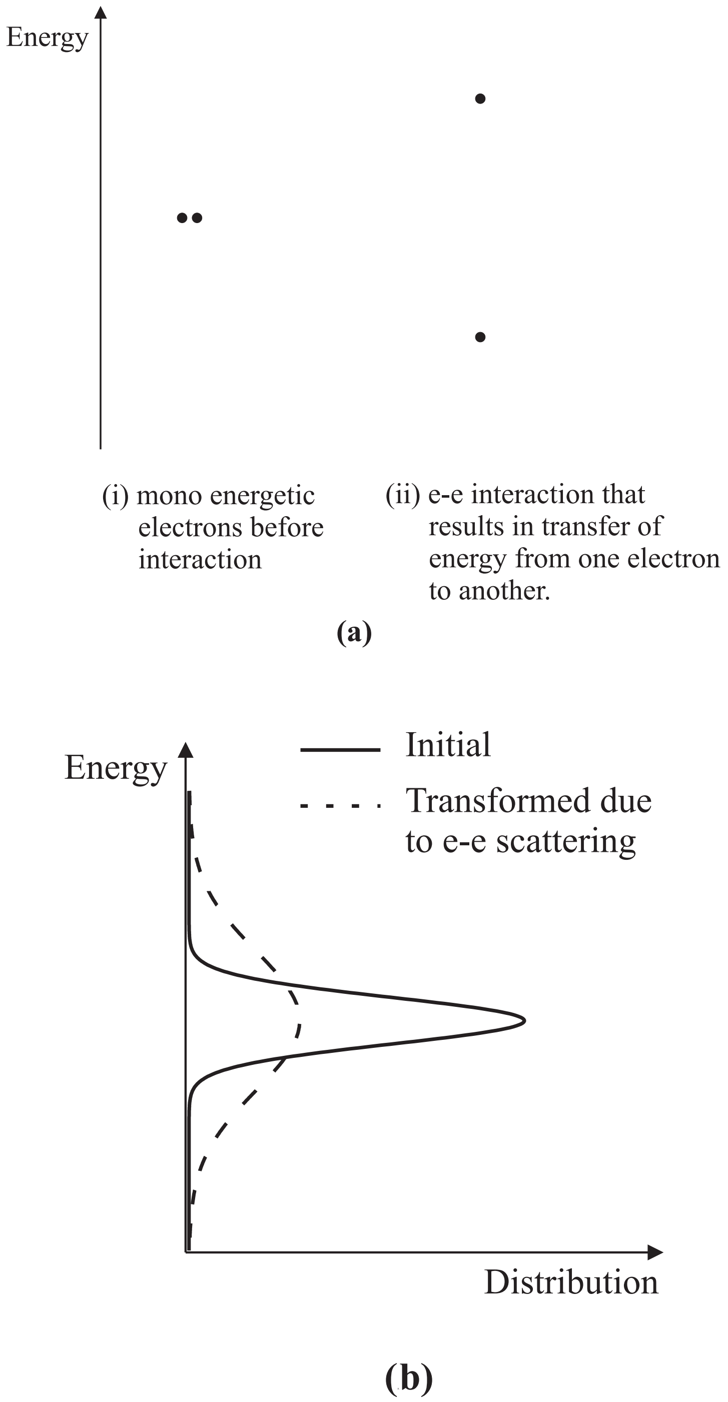


Figure 2.3: Schematic illustrating the short-range electron-electron Coulomb interactions as an EED broadening mechanism [62]. (a) (i) two monoenergetic electrons before interaction (ii) after interaction. One of the electrons have relaxed by transferring part of its energy to the other electron. (b) an initially narrow EED broadened by EEI.

2.4.2.1 Short-Range Electron-Electron Interactions

One-to-one interaction of electrons are termed short-range interactions (SREEI). How SREEI influence the distribution is schematically illustrated in figure 2.3. Let us consider monoenergetic electrons as depicted in figure 2.3a(i). The interaction between these two electrons can result in one of the electron relaxing by giving a part of its excess energy to the other electron, figure 2.3a(ii). If we consider an ensemble of electrons with a narrow initial energy distribution as depicted by the solid line in figure 2.3b and also considering the fact that the interacting electrons need not have equal initial energies, the consequence of the interactions would be a broadening of the distribution as depicted by the dotted line in the same figure.

Higher the energy of the interacting electrons, greater the extent of population beyond the qV limit. Consequently, SREEI are important in the high field region of the MOSFET. In contrast to EPI, where the energy exchanged is limited by the optical phonon energy, SREEI are more effective since the energy exchanged can be the excess energy of the higher energy electrons, which can be significantly higher than that of an optical phonon.

For a given field distribution, SREEI increases with increasing electron density [65, 68]. This is because, with increasing electron density electron-electron interactions become more frequent.

In the case of SREEI also, the energy gained by the electrons from the field is redistributed within the ensemble due to the interactions. MC groups have termed the mechanism as an energy gain mechanism. As mentioned in [72] "energy redistribution mechanism" is probably a more self describing phrase.

2.4.2.2 Long-Range Electron-Electron Interactions

Long-range electron interactions (LREEI) arise due to the fact that the Coulomb interaction extent beyond one Debye length [73]. LREEI is usually treated as plasma excitations induced by a high energy electron in an electron bath in equilibrium. A typical example is the interaction of high energy channel electrons with the cold electrons in the drain region of an n-channel MOSFET. MC simulations by Fischetti and Laux have shown that LREEI component can have a significant impact on the tail of the distribution function [38]. For example, the high energy channel electron entering the drain in a sequence of interactions with the cold electrons involving absorption of the energies of the cold electrons can gain a significantly high energy. Since average energy of the cold electrons in the drain is $1.5kT_L$, the efficiency of this mechanism compared to SREEI may not be significant.

The LREEI can also indirectly effect the distributions [74, 75]. The long-range nature implies that the Coulomb force of the drain electrons can be felt even in the pinch-off region of the MOSFET. This repulsive force can randomize the trajectories of the channel electrons reducing their effective mobility. The slowed down electrons have more time for interactions. In short, the long-range interaction can enhance SREEI and EPI.

MC simulations by Fischetti and Laux [74] have also predicted that LREEI in heavily doped silicon can increase the average energy of the electrons. The simulations were done for zero electric field condition. The increase in average kinetic energy was given by

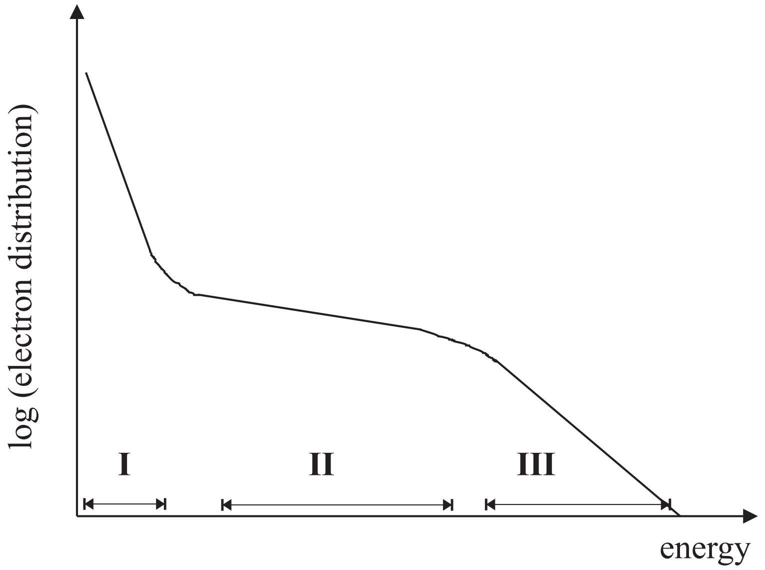


Figure 2.4: Schematic of electron energy distribution near the drain junction of an n-channel MOSFET, based on the results published by MC simulation groups [23, 38, 39]. The distribution can be divided into three regions which are marked as I, II and III. Region I represent electrons that are in thermal equilibrium with the lattice. Region II represent electrons that can be described by an "effective temperature". Region III corresponds to electrons which have energy greater than qV_D, where V_D is the applied drain bias.

$$\delta W_K = 1.451\kappa n^{1/3} \tag{2.5}$$

where

$$\kappa = \frac{q^2}{4\pi\epsilon_{Si}\epsilon_0} \tag{2.6}$$

where n is the density of the electron gas, q the elementary charge, ϵ_{Si} the static relative permittivity of silicon and ϵ_0 the absolute permittivity of free space.

From equation 2.5, the increase in the average kinetic energy for doping of 10^{18} and $10^{21} cm^{-3}$ are 17.5 and 175 meV respectively.

Fischetti and Laux further predicted that LREEI can result in high energy tails in EED of a stationary electron gas. Such tails have effective temperatures much higher than the lattice temperature. They found effective temperature values of 390 and 1205 K for donor doping levels of 10^{19} and $10^{20} cm^{-3}$ respectively.

2.4.3 Electron Energy Distribution in n-channel MOSFETs

Schematic of EED near the drain junction of conventional n-channel MOSFETs published by MC simulation groups is shown in figure 2.4. It is based on the data published in [23, 38, 39]. EED is divided into three regions to facilitate understanding.

Region I is occupied by electrons which are in thermal equilibrium with the lattice and the line has a slope of $-1/kT_L$, where T_L is the lattice temperature. Region II correspond to the field driven high energy electrons. The slope of the segment is $-1/kT_E$, where T_E is the effective temperature of the electrons. Region II extends till energy approximately equal to qV_D for deep sub-micron structures. The vicinity of qV_D correspond to the electrons ballistically transported from the source to drain. Region III is beyond qV_D and is called the high energy tail of the distribution. As was discussed, the tail can be a thermal tail with slope of $-1/kT_L$ or EEI induced.

2.4.4 Discussion

Any numerical analysis of problems in physics is at best predictive. They either follow an experimental observation or predict physical phenomenon based on state-of-the-art understanding of physics. In the later case it is imperative to verify the predictions experimentally to confirm them. In the following we would review the literature to assess if there are sufficient experimental support to EPI, SREEI and LREEI as energy redistribution mechanisms.

The EED can be experimentally investigated using hot-carrier luminescence measurements [76, 77]. But this technique is not suited to investigate the tail of the EED beyond qV due to inadequate sensitivity.

Experimental support to SREEI broadening of EED tail has come from the observation that M is underestimated in comparison to measured data when SREEI is turned off in MC simulation [12, 23]. Interestingly, Bude and Mastrapasqua [25] could reproduce measured I_{SUB}/I_D down to a V_D of 1.2 V without including SREEI whereas in the work of Ghetti et al., M was underestimated for V_D below 1.6 V when SREEI were turned off in the simulations. Bude et al. [12] found that I_G/I_D was underestimated for V_D below 3.1 V when SREEI was not included. It should be noted that I_{SUB} is caused by the part of EED above 1.1 eV whereas I_G is caused by the part above 3.1 eV. I_G estimates have the additional complexity of accounting for the tunneling probability of electrons through the oxide [78]. Both the groups have modeled only SREEI in their code.

Bude et al. [30] found it necessary to include SREEI to correctly model threshold energy for interface degradation. Rauch et al. [59] reported that hot-carrier degradation in devices of 0.085 μm effective channel length showed increasing trend as V_G was increased. This is in contrast to the widely held view that the degradation is maximum for stress at maximum I_{SUB} condition or for $V_G = V_D/2$ bias [4, 55, 60, 79, 80]. Investigations of Mahapatra et al. [60] were also on devices with drawn channel length of 0.1 μm (effective channel length $\sim 0.08\,\mu m$). Rauch et al. explained their results as due to SREEI. Hess et al. [53] have expressed apprehensions whether SREEI can be so strong to produce observable degradation.

The assumption of Rauch et al. [59] that SREEI enhances as V_G is increased is justified for an unchanging electric field distribution. However, in the case of a MOSFET, even though the inversion layer charge density increases with V_G, field heating decreases with increasing V_G due to the reduction of $E_{LATpeak}$. Impact of V_G variations on SREEI is not clear.

There is yet to be any experimental proof for the thermal tail. SREEIs are important when the channel electron concentration is very high. Abramo et al. [65] and Ghetti et al. [23] have used a threshold of $10^{17} cm^{-3}$ for the electron concentration for SREEI to be significant. Based on this, MC simulations can provide a proof of the thermal tail by reproducing the measured M data for subthreshold V_G values in modern device structures. Unfortunately MC technique has serious convergence problems in the subthreshold regime of device operation as already pointed out.

Fischer et al. [78] investigated the bias and temperature dependencies of homogeneous hot-electron injection from silicon into silicon dioxide at low voltages. A method for extracting the slope of the tail of EED was analytically obtained in their work. Their theoretical work predicted that the thermal tail would show up at very low oxide fields because EEI were expected to be negligible in such investigations. However the experimentally extracted tails, from data measured on MOS structures, had effective temperatures ranging from 500 to 700 K depending on the oxide field. T_E of the tails were independent of T_L. They further speculated that the tail would show up for still smaller oxide fields (smaller than 2.08 MV/cm). There are practical and theoretical difficulties with such an approach. The injection probability in this case depends on the carrier distribution function and the transmission probability. For very low fields, the transmission probability is difficult to assess because there are two competing tunneling processes, namely Fowler-Nordheim and direct tunneling. On the practical front, by the authors' admission, floating gate measurement techniques they used did not provide reliable data for oxide fields below 2.08 MV/cm. Floating gate measurements are the most sensitive known I_G measurement technique presently available for MOS structures.

There is no experimental support for the role of LREEI on EED.

The lowest V_D for which measured hot-electron data were reproduced using MC simulations was 1.2 V by Bude and Mastrapasqua [25]. They found good match of simulated and measured M without accounting for EEI. They used M instead of I_{SUB} because simulated M data were less noisier than I_{SUB} data. The anomalous V_{Gpeak} increase reported by Balestra et al. [47] and discernible in the data of A. Hori et al. [48] and Odanaka and Hiroki [49] are not addressed by MC groups.

2.5 Summary

In this chapter, we have reviewed the literature related to low voltage hot-carrier effects in n-channel MOSFETs.

A brief overview of hot-carrier effects was given. Then we presented some of the most widely used theoretical approaches to hot-carrier effects. These include treatment based on electric field, energy balance equations and MC simulation techniques. From a field perspective, hot-carrier effects should disappear when the supply voltage is reduced below thresholds for the respective processes.

Experimental data on low voltage hot-electron effects found in the literature were then presented. A cross-over effect was reported in the temperature dependence of substrate current at low drain voltages and was attributed to the increase in the threshold energy for impact ionization. No detailed data is available in the literature on the channel length and gate voltage dependencies of the cross-over voltage.

Impact ionization for drain voltages below the threshold energy for the process was reviewed. We have pointed out some inconsistencies in published data that may be due to improper measurement resolutions and interference with leakage currents. We have also pointed out an anomalous increase in the peak substrate current bias condition observed in literature data which remain largely unnoticed and unexplained.

Controversy regarding the threshold energy for interface state damage was discussed. The threshold voltage values for the process found in the literature varies from 2.5 to 3.7 V. There are also suggestions of a soft threshold. Experimental data available on sub-barrier gate injection and interface damage for drain voltages as low as 1.4 and 1.9 V respectively were discussed. From this perspective, the tail of the EED has a significant role to play at low supply voltages.

Physical mechanisms that are thought to be responsible for populating the distribution beyond the applied drain voltage were discussed. Electron-phonon interactions and short and long-range components of electron-electron interactions are found to be the candidates. Even though the role of short-range interaction is established by matching experimental and MC simulation data, its strength remain a subject of debate. No experimental support was found for the role of electron-phonon interactions and long-range interactions.

The lowest drain voltage for which MC simulation results have been matched with experimental substrate current data is 1.2 V even though substrate current has been reported for drain voltage down to 0.6 V. Anomalous experimental observations already described remain unexplained. Effect of device scaling on mechanisms populating the tail of the distribution are also not clear.

Based on the review we address some of the issues which are not yet explored in the literature. In chapter 3, channel length and gate bias dependence of substrate current cross-over is presented and analyzed for a broad range of channel lengths. Chapter 4 discusses impact ionization in conventional lateral nMOSFETs at the lowest drain voltages at which substrate current could be measured. Presence of thermal tail is verified. Clear signatures of short-range interactions identified and its strength assessed. We have proposed inversion layer quantization as an energy gain mechanism that can be important at very low drain voltages. In chapter 5, we present data on low voltage impact ionization in laterally asymmetric channel nMOSFETs. The interpretations of chapter 4 are strengthened using extensive experimental data. We have also suggested the structure as a promising one to investigate the role of long-range interactions on EED. In chapter 6 we have presented data on low voltage gate injection and hot-carrier degradation.

Chapter 3

Temperature Dependence of Substrate Current in nMOSFETs

Substrate current (I_{SUB}) due to impact ionization increases with decreasing temperature as a consequence of reduced phonon scattering at low temperature. However, as discussed in chapter 2, there have been reports of a reversal in the temperature dependence of I_{SUB} at low drain voltages (V_D). This phenomenon is called “cross-over effect”. As was pointed out in chapter 2, there is insufficient data on the dependence of this effect on channel length (L) and gate bias (V_G). In this chapter, a detailed investigation of the channel length and gate bias dependencies of cross-over effect is presented. Experimental data are analyzed on the basis of the present understanding of the cross-over effect and two-dimensional drift-diffusion simulation data.

3.1 Devices

The devices used in this study have L ranging from 0.16 to 10 μm. The gate oxide has a thickness of 3.6 nm. Devices were made with a shallow source-drain extension technology. The source and drain contact resistances were optimized using a silicidation process involving a Germanium preamorphization implant. The details of the fabrication process can be found in [81] and is briefly outlined in Appendix A. The devices used in this study are called CON (short form of CONventional) devices to distinguish them from the asymmetric devices discussed in chapter 5.

The simulated doping profile in the channel of the device is shown in figure 3.1. A source/drain extension junction depth of 50 nm was also obtained from simulations. Typical measured output characteristics of the smallest devices used in these investigations, $L = 0.16\, \mu m$, at 300 and 77 K are shown in figure 3.2 for various gate over-drives ($V_{GT} = V_G - V_T$, where V_T is the threshold voltage). The devices show fairly good characteristics.

3.2 Experimental Results

Cross-over effect was experimentally investigated for channel lengths of 0.16 to 10 μm by measuring the I_{SUB} as a function of V_G and V_D. Different bias conditions were employed in the investigations.

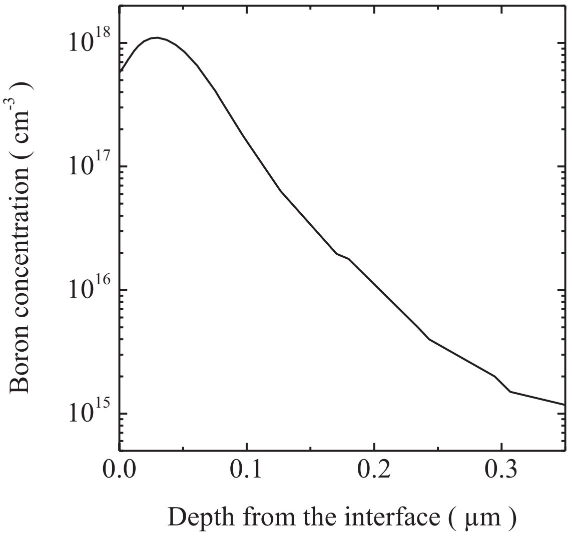


Figure 3.1: Simulated boron depth profile in the channel.

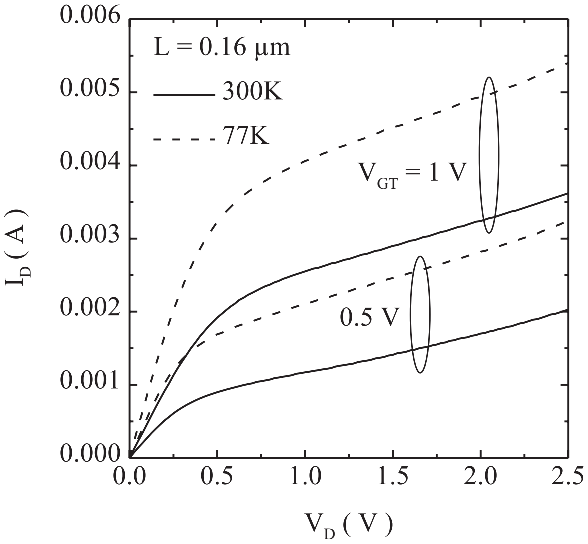


Figure 3.2: Measured output characteristics of devices of channel length $0.16\,\mu m$ and width $10\,\mu m$ at 300 and 77 K.

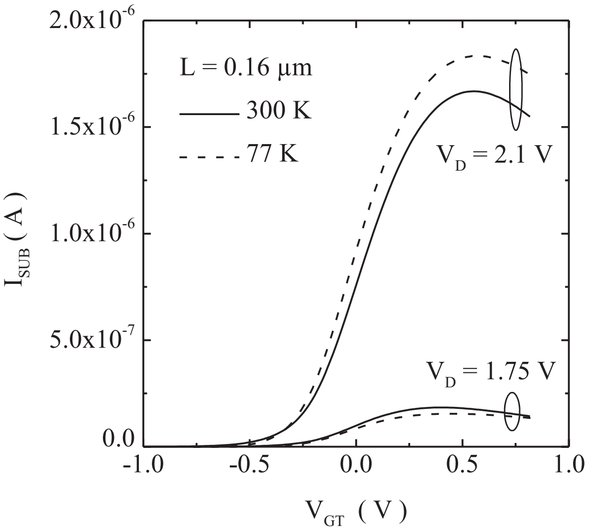


Figure 3.3: I_{SUB} vs V_{GT} illustrate the cross-over effect. For $V_D = 2.1\,V$, I_{SUB} is higher at 77 K than at 300 K whereas for $1.75\,V$ it is higher at 300 K.

3.2.1 Cross-over in Substrate Current

Figure 3.3 shows I_{SUB} vs V_G characteristics for $V_D = 1.75$ and $2.1\,V$ for $L = 0.16\,\mu m$. For a V_D of 2.1 V, I_{SUB} is higher at 77 K than at 300 K. Such a behavior is well known and is attributed to the less frequent scattering of electrons by optical phonons at low temperature [10, 22]. For $V_D = 1.75\,V$, the behavior is reversed. I_{SUB} is lower at 77 K than at 300 K. It can be expected that for a specific V_D between these values, I_{SUB} is independent of temperature.

V_D at which I_{SUB} is independent of temperature is defined as the cross-over voltage, V_{XOVER}. Alternatively, it can also be defined as the drain voltage at which the ratio of I_{SUB} to I_D is independent of temperature. Both definitions are used in the literature. Monte-Carlo simulation groups in particular prefer the later, due to the reduced noise of the ratio, to the actual I_{SUB} value [25].

Figure 3.4a shows $I_{SUBpeak}$ vs V_D data at 300 and 77 K for $L = 0.16$ and $5\,\mu m$. A cross-over of I_{SUB} is observed for V_D around $2\,V$, the $5\,\mu m$ device showing a higher V_{XOVER} than the shorter device. Figure 3.4b shows similar data for a fixed gate overdrive (V_{GT}) of $0.5\,V$. In this case also V_{XOVER} is higher for the longer device. For both the bias conditions, the difference in I_{SUB} values at 300 and 77 K becomes smaller as L is reduced.

Channel length dependence of V_{XOVER} for various bias conditions was studied. Figure 3.5 shows V_{XOVER} vs L data for $I_{SUBpeak}$ and $V_{GT} = 0.5\,V$ bias conditions. For both the bias conditions, V_{XOVER} increases as L is increased. V_{XOVER} vs $\log(L)$ data can be fitted with a parabolic function for the range of L studied, indicating a strong dependence. L dependence is stronger for $V_{GT} = 0.5\,V$ bias condition than $I_{SUBpeak}$ bias condition. This point was further investigated by plotting L dependence of the V_G corresponding to $I_{SUBpeak}$ at V_{XOVER}, as shown in figure 3.6. The line corresponding to $V_{GT} = 0.5\,V$ is also shown. The difference between V_{Gpeak} corresponding to V_{XOVER} and $V_{GT} = 0.5\,V$ increases as L increases.

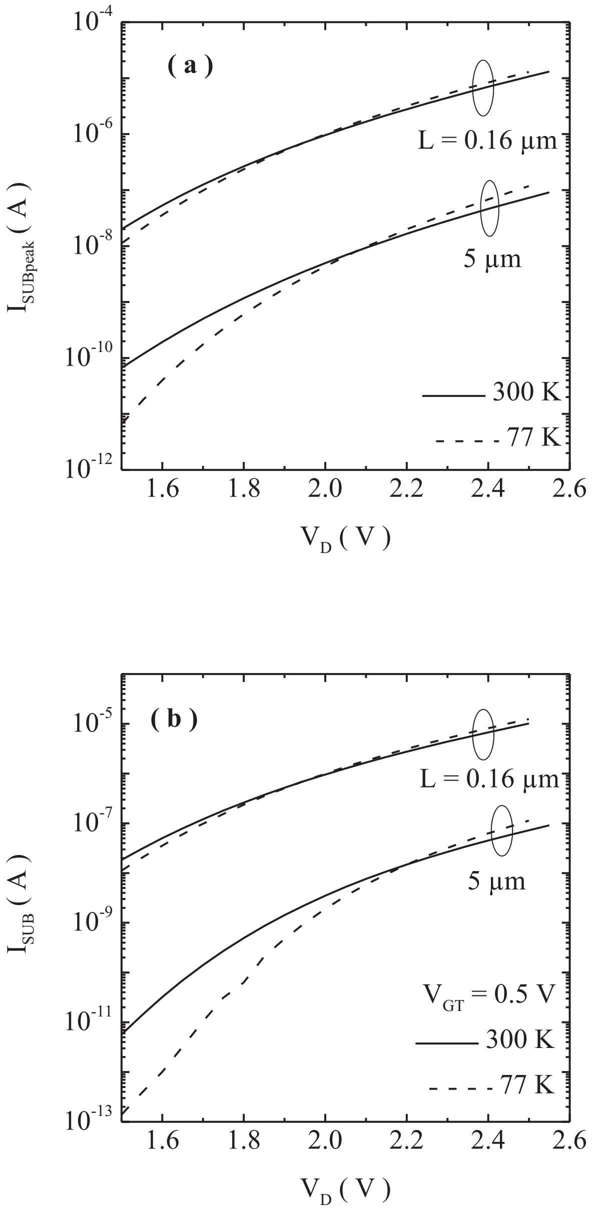


Figure 3.4: The cross-over in I_{SUB} for devices of $L = 0.16$ and $5\,\mu m$ for two different bias conditions. Bias condition of (a) $I_{SUBpeak}$ and (b) $V_{GT} = 0.5\,V$.

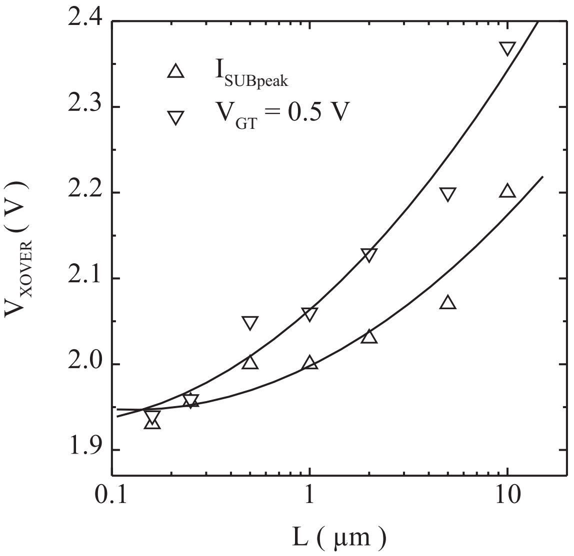


Figure 3.5: Channel length dependence of V_{XOVER} for $I_{SUBpeak}$ and $V_{GT} = 0.5\,V$ bias conditions.

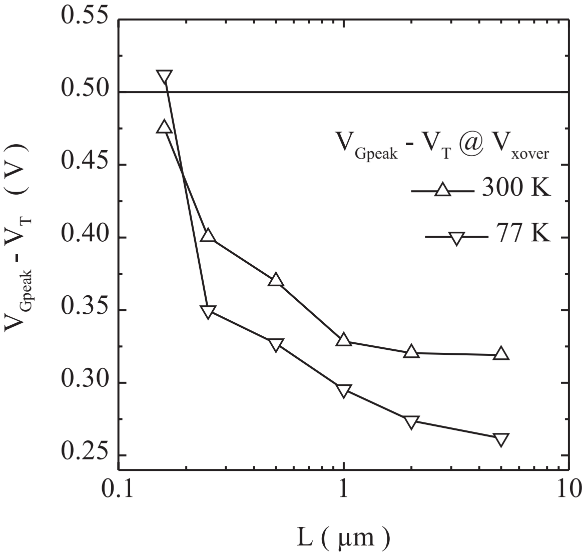


Figure 3.6: L dependence of V_{GT} corresponding to $I_{SUBpeak}$ at the cross-over voltage shown in figure 3.5. $V_{GT} = 0.5\,V$ line is also shown for comparison.

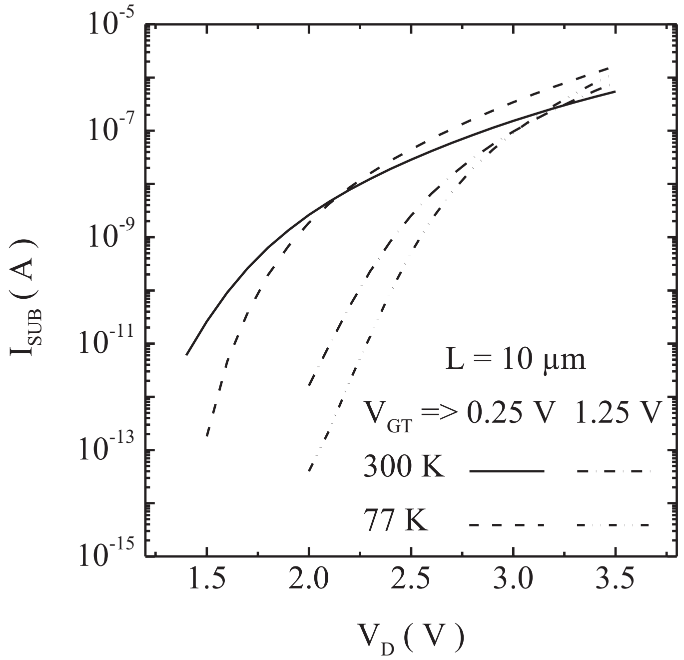


Figure 3.7: I_{SUB} vs V_D for $V_{GT} = 0.25$ and $1.25\,V$ for $L = 10\,\mu m$ at 300 and 77 K. V_{XOVER} shifts to higher values as V_{GT} is increased.

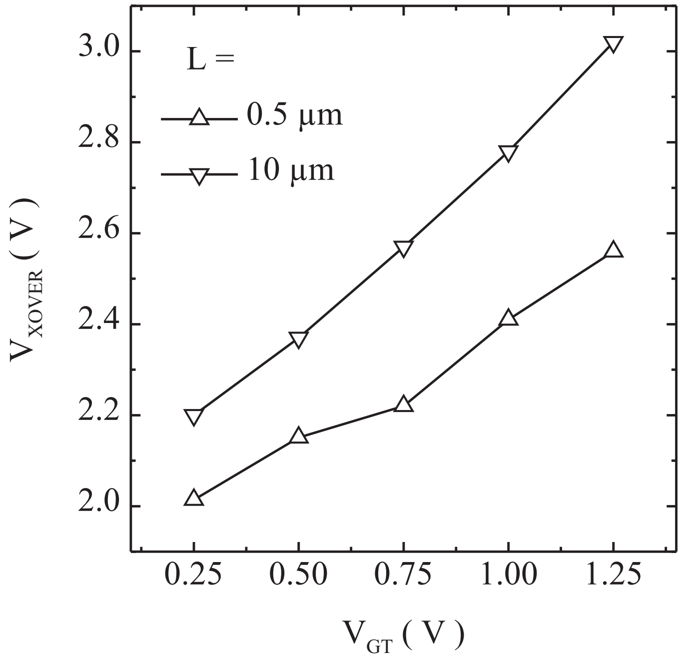


Figure 3.8: Dependence of V_{XOVER} on V_{GT} for $L = 10$ and $0.5\,\mu m$.

Dependence of V_{XOVER} on V_{GT} was investigated. Figure 3.7 shows I_{SUB} vs V_D data for $V_{GT} = 0.25$ and $1.25\,V$ for $L = 10\,\mu m$ at 300 and 77 K. V_{XOVER} is found to shift to higher values as V_{GT} is increased. A more systematic investigation of this was carried out for various values of V_{GT} for various channel lengths. Figure 3.8 shows the data for devices of channel lengths 10 and $0.5\,\mu m$. V_{XOVER} increases as V_{GT} increases. The dependence on V_{GT} is stronger for the $10\,\mu m$ device.

3.2.2 Summary of Experimental Results

1. A Cross-over was observed in I_{SUB} vs V_D characteristics.
2. For identical bias conditions, V_{XOVER} increases with L.
3. For a given L, V_{XOVER} increases with increasing V_{GT}.

3.3 Analysis and Discussion

In this section, the present day understanding of the cross-over effect will be presented, based on the electron energy distributions shown in figure 2.4. L and V_{GT} dependence of V_{XOVER} will then be examined using a two-dimensional drift-diffusion simulation tool, MINIMOS 6 [82]. In the process we gain useful insights into the channel length and gate voltage dependencies of EED above W_G.

3.3.1 Theory of the Cross-over Effect

The present understanding of the cross-over effect is that it is caused by the increase in the impact ionization threshold (which is equal to W_G) as the temperature is reduced [23, 38, 39]. In the following we would examine our results based on this model. The strong L and V_{GT} dependencies of V_{XOVER} are explained.

The idea of Fischetti and Laux [38] is simplified and shown in figure 3.9. The figure shows the schematic of the electron energy distribution (EED) at two temperatures T1 and T2. T1 is greater than T2. EED is assumed to have a thermal tail in the present case. This assumption has no bearing on the model. Impact ionization is initiated by electrons lying beyond W_G. The value of W_G increases with temperature [41, 42, 43]. It should be emphasized here that the EED shown in figure 3.9 is that at a point in the high field region of the channel, near the drain junction. There will be contributions from different locations of the high field region and the EEDs at all such points may differ in details but not in general nature. The schematic shown can be taken as representative and would suffice for qualitative analysis. But it should be kept in mind that the impact ionization rate is decided by integrating the contributions from the EED, in the entire active area of the device.

The field heated part of EED has higher occupation at low temperature due to reduced phonon scattering. But there is also an increase in the impact ionization threshold energy as the temperature is reduced. The later part is material dependent and the former depends on the electric field distribution and hence on the device structure and bias conditions. I_{SUB} is decided by the area under the EED above W_G. From figure 3.9 the condition for cross-over can be graphically determined. Gain in the

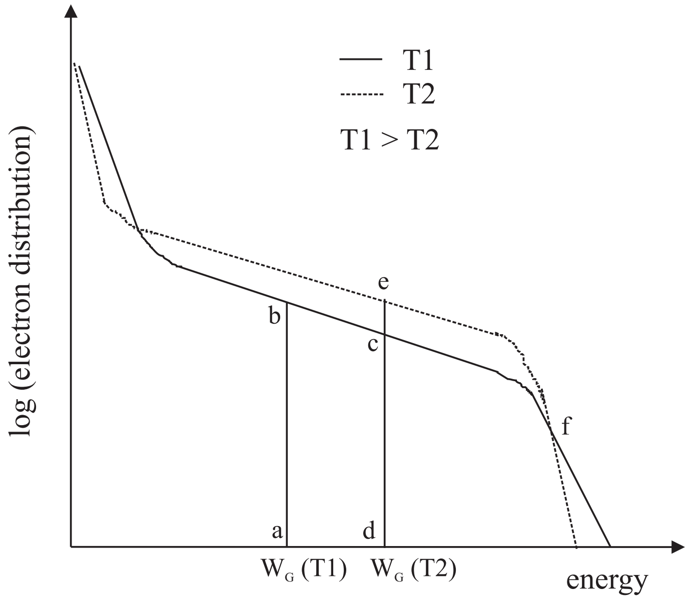


Figure 3.9: Schematic of the electron energy distributions at two different temperatures illustrating the basis of the cross-over effect. I_{SUB} is higher at lower temperature when the area **cefc** is greater than the area **abcda** and vice versa.

area due to the reduced scattering at low temperature correspond to the area enclosed by **cefc**. The area loss is given by region enclosed by **abcda**. When the drain bias is large, the field heated part of EED is broad and the area increase, **cefc** supercedes the area decrease **abcda**. Consequently I_{SUB} is higher at lower temperature. As V_D (and hence the field) decreases, the field heated part of EED becomes narrower and the area decrease **abcda** becomes comparable and even larger than the area increase **cefc**, resulting in a reduced I_{SUB} at low temperature. Cross-over occurs when the contribution of the areas **cefc** over the active device domain equals the contribution of the areas **abcda**.

It can be stated that, cross-over occurs when the enhancement of impact ionization due to the suppressed phonon scattering is not sufficient to compensate for its suppression due to the increase in threshold energy.

Dependence of the areas **abcda** and **cefc** on the device structure and bias conditions is complex due to the complex nature of the energy gain and loss mechanisms outlined in chapter 2. State of the art approach to such a problem would be using Monte-Carlo simulation tools incorporating models for all the important scattering mechanisms. Nevertheless we would attempt to qualitatively explain the L and V_{GT} dependencies of V_{XOVER} based on lateral electric field (E_{LAT}) distributions obtained from 2-dimensional drift-diffusion simulations.

3.3.2 Channel Length and Gate Over-drive Dependencies of Cross-over Voltage

2-dimensional device simulations were performed on device structures of various channel lengths under various bias conditions using MINIMOS 6. The models used were

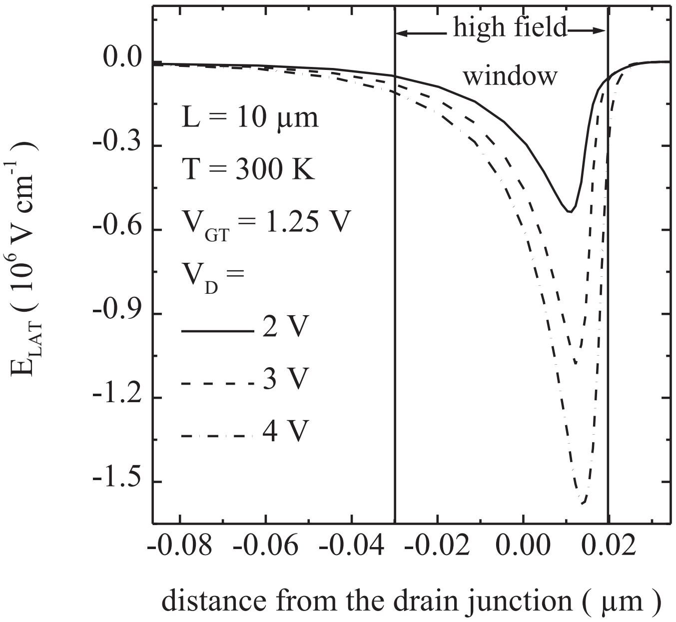


Figure 3.10: E_{LAT} near the drain junction at a depth of 1 nm from the interface for a device of channel length $10\mu m$ at 300 K for various V_D. The high field window has a length of approximately 50 nm, very close to the energy relaxation length, 40 nm, quoted by Sano et al.[39].

the default models outlined in MINIMOS 6 manual [82]. Drift-diffusion approximation of Boltzmann Transport Equation (BTE) as implemented in simulation tools like MINIMOS or PISCES [83] does not provide an EED, which is of great importance to theoretically investigate the problem at hand. The Monte-Carlo module in MINIMOS 6 does not provide EED.

Since the major contribution to impact ionization for the V_D range of interest comes from the field heated part of the distribution, qualitative information can still be obtained based on the lateral electric field (E_{LAT}). In the present work, peak lateral electric field ($E_{LATpeak}$) is taken as representative of the effective electron temperature (T_E) which decides the slope of region II of figure 2.4. This can be heuristically supported the following way. If we consider a device of channel length 10 μm in saturation, most of the applied V_D is dropping in the pinch-off region which is about 50 nm in length for a V_D of 2 V for the technology (channel doping profile) under consideration. This point was confirmed by simulations, figure 3.10. A significant number of the electrons transported across such a high field region will not be in thermal equilibrium with the lattice. This will be reflected as a flatter region II in figure 2.4. The same device for the same V_D, operating in the linear region, the channel can safely be assumed as a resistor and the applied V_D is dropping uniformly along the channel. That means a 25 mV drop ($\sim kT/q$ at 300 K) over a length of 125 nm, which is much larger than the widely accepted values of the mean free path of electrons ($\sim 9\, nm$) in silicon at 300 K. The electrons are in thermal equilibrium with the lattice, EED can be approximated by a Maxwellian with the lattice temperature. As the device is driven from saturation to the linear region of operation by increasing V_G, $E_{LATpeak}$ and T_E are decreasing. We can conclude that the $E_{LATpeak}$ can be taken as a qualitative representative of T_E of the electrons in the sense that they show similar trends as V_G or L are varied for a given V_D.

We would like to caution that the scheme outlined above may not be used to compare devices of identical channel lengths originating from different technologies as the details of the channel doping profiles can have a significant effect on EED [70]. Devices of extremely short channel length in which significant ballistic transport can be present, $L < 100\,nm$, can also not be analyzed by the qualitative arguments presented in the previous paragraph.

Figure 3.11 shows the change of $E_{LATpeak}$ as L is varied for identical bias conditions of $V_D = 2\,V$ and $V_{GT} = 0.5\,V$ at 300 and 77 K. The devices are biased in the saturation regime of operation, $V_D > V_{GT}$. $E_{LATpeak}$ decreases as L is increased. The fall is more pronounced at 77 K than at 300 K. Consequently T_E decreases as L is reduced.

Figure 3.12 shows $E_{LATpeak}$ for a device of channel length 0.5 μm for $V_D = 2\,V$ and for various V_{GT} at 300 and 77 K. In this case, $E_{LATpeak}$ decreases as V_{GT} is increased. Following the arguments advanced previously, T_E of the electrons decreases as V_{GT} is increased.

Referring to figures 3.5, 3.8, 3.11 and 3.12, it can be noted that V_{XOVER} and $E_{LATpeak}$ show exactly opposite trends. V_{XOVER} increases with increasing L and V_{GT} whereas $E_{LATpeak}$, and by implication T_E, decreases with increasing L and V_{GT}. In the following we would attempt to explain L and V_{GT} dependencies based on this observation.

Figure 3.13 shows the schematic of EED corresponding to regions II and III, which were identified in figure 2.4. Distributions at two lattice temperatures and corresponding to different $E_{LATpeak}$ but identical V_D are shown. The variations in $E_{LATpeak}$ can be due to variations in V_{GT} or L as we have already seen. For example, at $T_L = T1$, the line passing through **bc** represent the distribution for a $E_{LATpeak}$ that is higher than that for the distribution passing through **b'c'**. Reduced $E_{LATpeak}$ implies lower T_E and hence a steeper slope of the distribution. When the field heating is reduced due to the reduction of $E_{LATpeak}$, the distribution skew in such a way that the population of the higher energy region reduces.

Now let us assume that a particular field, represents a cross-over condition for a device of given channel length. i.e., **abcda** = **cefc**. When $E_{LATpeak}$ is reduced by increasing V_{GT}, the condition to be satisfied for cross-over to be present is **ab'c'da** = **c'e'fc'**. It should be noted that the vertical axis of the distributions shown so far are in logarithmic scale whereas the areas of interest to us are obtained by integrating the distribution function itself, not its logarithm. This would imply that the area loss **e'efe'** is most likely higher than the loss **b'bcc'b'** violating the condition for crossover. i.e., **ab'c'da** > **c'e'fc'**. I_{SUB} in such a case would be lower. For the new, higher V_{GT} the cross-over condition is re-established upon increasing V_D. This explains the increase in V_{XOVER} as V_{GT} is increased, figure 3.8.

The channel length dependence of V_{XOVER} seen in figure 3.5 can be explained along similar lines. This is because the increasing V_{GT} keeping V_D constant and increasing channel length for identical drain and gate bias conditions result in decreasing $E_{LATpeak}$ and hence lower T_E.

Figure 3.5 also shows that L dependence of V_{XOVER} is weaker for $I_{SUBpeak}$ bias

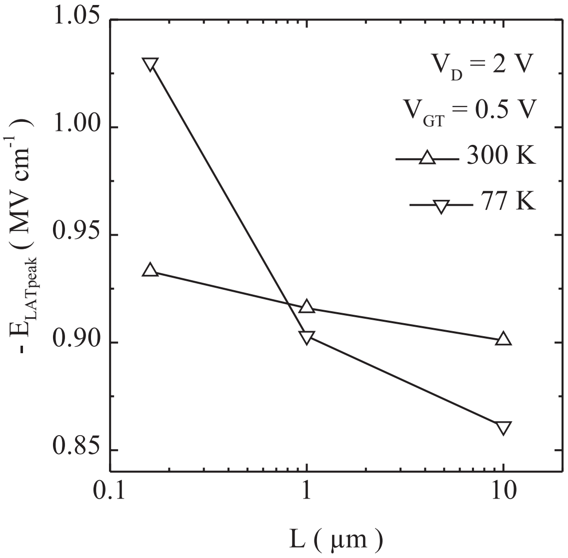


Figure 3.11: $E_{LATpeak}$ at a depth of 1 nm from the interface for identical V_D and V_{GT} as a function of L at 300 and 77 K. The peak field decreases as L is increased.

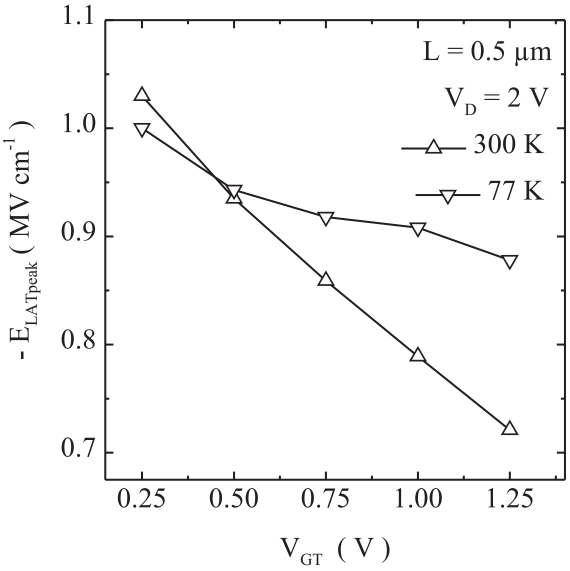


Figure 3.12: $E_{LATpeak}$, at a depth of 1 nm from the interface for a device of channel length $0.5\,\mu m$, versus V_{GT} at 300 and 77 K. The peak field decreases as V_{GT} is increased.

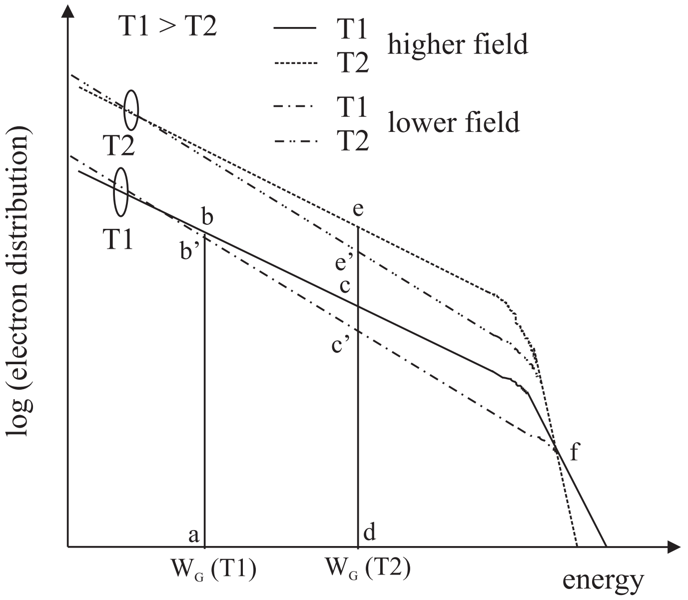


Figure 3.13: Schematic of EED for identical V_D but different $E_{LATpeak}$. Only the regions II and III of figure 2.4 are shown. The lines passing through **bc** and **b'c'** are distributions at a higher T_L, the former at a larger $E_{LATpeak}$ than the later. The lines passing through **e** and **e'** are distributions at a lower T_L and the former at a larger $E_{LATpeak}$ than the later.

condition than for $V_{GT} = 0.5\,V$. The data in figure 3.6 shows that V_{GT} at V_{XOVER} for $I_{SUBpeak}$ bias condition decreases as L is increased. i.e., $I_{SUBpeak}$ bias condition represents a lower V_{GT} than $0.5\,V$ fixed over-drive for the long channel devices, consequently V_{XOVER} is lower in the former case than in the later case. This strengthens our arguments further.

3.4 Conclusions

In this chapter, a detailed experimental investigation of channel length and gate bias dependencies of the cross-over phenomenon was presented. Devices of channel length from 0.16 to 10 μm were employed in the investigations.

The substrate current cross-over voltage showed an increase with increasing gate over-drive. It also increased with increase in channel length. We have explained these observations assuming the present understanding of the crossover effect, that it is caused by an increase in bandgap energy as the temperature is reduced, is valid. Both the experimental observations were explained by the gate bias and channel length dependence of the peak lateral electric field. The peak lateral field decreases, with increasing gate bias for identical channel length, and with increasing channel length for identical gate and drain biases.

Very useful qualitative insight was obtained about the electron energy distribution and its dependence on the gate voltage changes and channel length by correlating the experimental data to simulated peak lateral electric field. This information is extensively used in the subsequent chapters.

Chapter 4

Near Threshold Impact Ionization in Conventional nMOSFETs

In chapter 3, we had seen that an increase of 40 meV in the threshold energy for impact ionization, which is equal to the bandgap energy (W_G) in the case of silicon, is sufficient to cause a change in the temperature dependence of substrate current (I_{SUB}) at low drain voltages (V_D). The negative temperature dependence at high V_D turned to a positive temperature dependence at low voltages due to such a small change in W_G. This fact points to the need for exploring and understanding all possible energy gain and loss mechanisms accurately if impact ionization near and below the bandgap voltage is to be correctly understood. Any threshold phenomenon has increasing complexity as it near its threshold due to the fact that physical mechanisms, otherwise considered secondary, may play a significant role, some times as significant a role as the primary mechanisms.

One of the major short coming in the understanding of impact ionization near and below the threshold V_D is the non-availability of data that clearly identify experimental signatures of secondary energy gain mechanisms. Monte-Carlo (MC) simulation of measured I_{SUB} data for $qV_D < W_G$ are also not available in the literature.

In this chapter, we present a comprehensive experimental investigation of the impact ionization phenomenon near and below the threshold voltage for the process in n-channel MOSFETs of channel lengths (L) ranging from 0.16 to 5 μm. The experimental data is analyzed on the basis of Monte-Carlo simulation results available in the literature to bring out clearly identifiable features of secondary energy gain mechanisms for the first time in the literature. Possible implications of inversion layer quantization (ILQ) on electron energy distribution (EED) are also investigated.

The chapter is organized as follows. Novel experimental data on near threshold impact ionization are presented in section 4.1. I_{SUB} vs gate voltage (V_G) characteristics with two peaks were measured. The experimental results are analyzed in section 4.2. In that section, experimental verifications of a lattice temperature dependent tail (LTDT) and electron-electron interaction (EEI) induced broadening of the tail are provided. An experimental method is presented to quantitatively assess the relative contributions of the thermal and EEI tails to I_{SUB}. Based on one dimensional Poisson-Schrödinger simulations, we also propose ILQ as an energy gain mechanism. L dependence of I_{SUB} data is analyzed and suggest a correlation between field heating and the energy exchanged in short range EEI. The chapter is concluded in section 4.3 where the results are summarized and their implications for device reliability are speculated.

4.1 Experimental Results

I_{SUB} was measured as a function of V_G with V_D as a parameter for n-channel MOSFETs of $L = 0.16$ to $5\,\mu m$. The gate oxide thickness was 3.6 nm. The devices have a conventional structure with source and drain extensions. The structural details of the devices and the characteristics were already presented in chapter 3. The measurements were performed at temperatures varying from 300 to 77 K in well shielded measurement setups. Low level measurement techniques and practices were employed to ensure a measurement accuracy in the femto Ampere range [84].

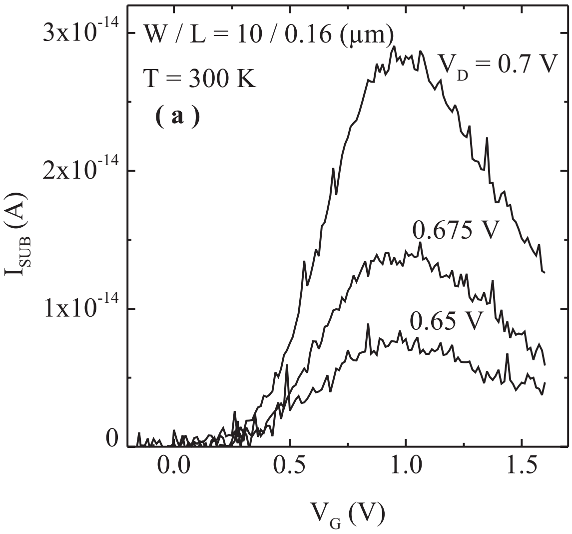
4.1.1 I_{SUB} vs V_G Characteristics

Bell shaped I_{SUB} vs V_G characteristics, which is identified as a signature of impact ionization in MOSFETs [32, 33, 46], measured for a device of $L = 0.16\,\mu m$, are shown in figure 4.1. Signature of impact ionization is visible for $V_D = 0.65\,V$ at 300 K and $V_D = 0.8\,V$ at 77 K. The value of W_G at 300 and 77 K are 1.12 and 1.16 eV respectively [43]. If we assume that the electrons initiating impact ionization have gained all their energy from the lateral electric field (E_{LAT}), there should not be any impact ionization for V_D below 1.12 V at 300 K and 1.16 V at 77 K.

The lowest V_D for which such bell shaped curves could be measured, V_{Dmin}, was investigated for devices of L upto $5\,\mu m$. V_D steps used in the measurements were 25 mV. The results are shown in figure 4.2. Bandgap voltages at the two temperatures are also shown in the figure. There is an increase in V_{Dmin} as L is increased. The changes are more prominent in the lower L regime. At 300 K, V_{Dmin} tend to saturate for longer devices. Impact ionization is observed in all the devices for sub-bandgap V_D at 300 K. At 77 K, we observe a shift in the data upwards. The saturation seen in the longer devices at 300 K is no more visible, suggesting that the upward shift in the data is not only due to the poorer measurement resolution. No sub-bandgap impact ionization is observed in 2 and $5\,\mu m$ devices at 77 K.

The results of I_{SUB} measurements on $L = 5$, 1 and $0.5\,\mu m$ devices are shown in figures 4.3, 4.4 and 4.5. The purpose of the figures is to capture any distinguishable features that may be present in the I_{SUB} vs V_G data. With this in mind, the data are shown only for V_D sufficiently large to unambiguously bring out distinguishable features above noise level. Figure 4.3 shows the data at 300 K. Clear bell shaped I_{SUB} vs V_G are observed. The plots for the $1\,\mu m$ device, figure 4.3b, is broader on the falling part than that for the $5\,\mu m$ device, figure 4.3a.

Figure 4.4 shows I_{SUB} vs V_G data at 77 K for devices of $L = 5$ and $1\,\mu m$ and figure 4.5 shows the same for $L = 0.5\,\mu m$. The rising part of the curves is steeper than at 300 K. This is due to the higher subthreshold slope at 77 K. The falling part for the data for the $5\,\mu m$ device, figure 4.4a, shows a knee at the lowest V_D shown. The knee becomes less visible as V_D is increased. In the case of the $1\,\mu m$ devices, figure 4.4b, plots for the lowest V_D shows a bump on the rising part of the characteristics. This bump increases in prominence as V_D is increased and becomes a peak. In fact, two peaks can be discerned for a V_D of 1.35 V in figure 4.4b. This is more clearly shown in



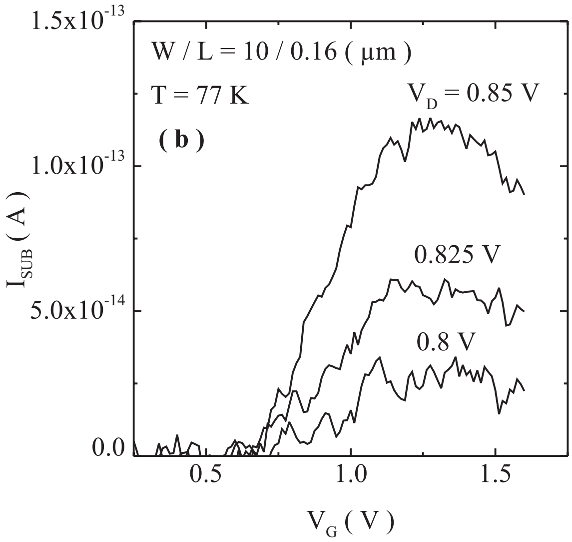


Figure 4.1: Bell shaped I_{SUB} vs V_G characteristics, a signature of impact ionization in MOSFETs, measured for n-channel devices of $L = 0.16\,\mu m$. (a) at 300 K and (b) at 77 K. Impact ionization is observed for V_D of 0.65 V at 300 K and 0.8 V at 77 K. These voltages are much below the bandgap voltages of silicon at either temperature.

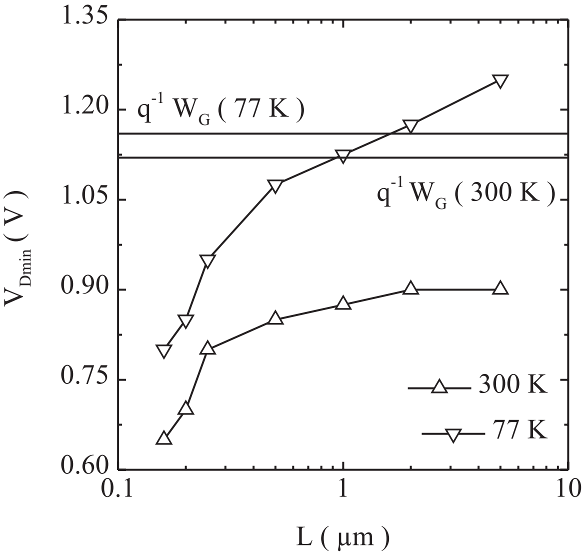


Figure 4.2: The smallest V_D at which discernible bell shaped I_{SUB} vs V_G characteristics could be measured at 300 and 77 K as a function of L. The bandgap voltage ($q^{-1}W_G$) at the two temperatures are also shown by horizontal lines.

figure 4.6 where the vertical axis is in linear scale. For the 0.5 μm devices, figure 4.5, I_{SUB} peak gradually moves to higher V_G as V_D is reduced.

These results can be summarized as follows. The I_{SUB} vs V_G characteristics show two peaks for V_D values near the bandgap voltages at 77 K. The second peak is less prominent for the longer devices and becomes less visible as the V_D is increased. As the L is reduced, the transition between the two peaks becomes less discernible.

4.1.2 V_{Gpeak} vs V_D Plots

I_{SUB} vs V_G characteristics are reported to peak for the bias condition, $V_D/3 \leq V_G \leq V_D/2$ [85]. A careful look at the figures 4.1a and 4.1b shows that this is not true of the devices under study. This observation and the anomalous double peak behavior motivated a study of the variations in V_G at which I_{SUB} peaks with variations in V_D for devices of various L at 300 and 77 K. The peak I_{SUB} is represented by $I_{SUBpeak}$ and the corresponding value of V_G is represented by V_{Gpeak} hereafter.

V_{Gpeak} vs V_D plots are shown in figure 4.7. For this analysis, the higher peak was considered where two maxima were present. V_T is subtracted from V_G to account for the variations in V_T with L. V_T was extracted using the linear slope method [86] for a V_D of 0.05 V. Figure 4.7a shows the data at 300 K for devices of $L = 5$, 0.5, 0.25 and 0.16 μm. For the 5 μm device,$V_{Gpeak} - V_T$ shows a nearly linear relationship with V_D, with a slope of 1/3. V_{Gpeak} is even below V_T at the lowest V_D for devices of L below 0.5 μm. An abnormal increase in V_{Gpeak} is observed as V_D approaches the bandgap voltage for $L \leq 0.25\,\mu m$. For the 0.25 μm device, V_{Gpeak} increases as V_D is reduced below 1 V whereas such a reversal happens for the 0.16 μm device as V_D is reduced below 1.25 V. For the 0.16 μm device, $V_{Gpeak} - V_T$ nearly flattens to about 0.4 V for $V_D \leq 1\,V$.

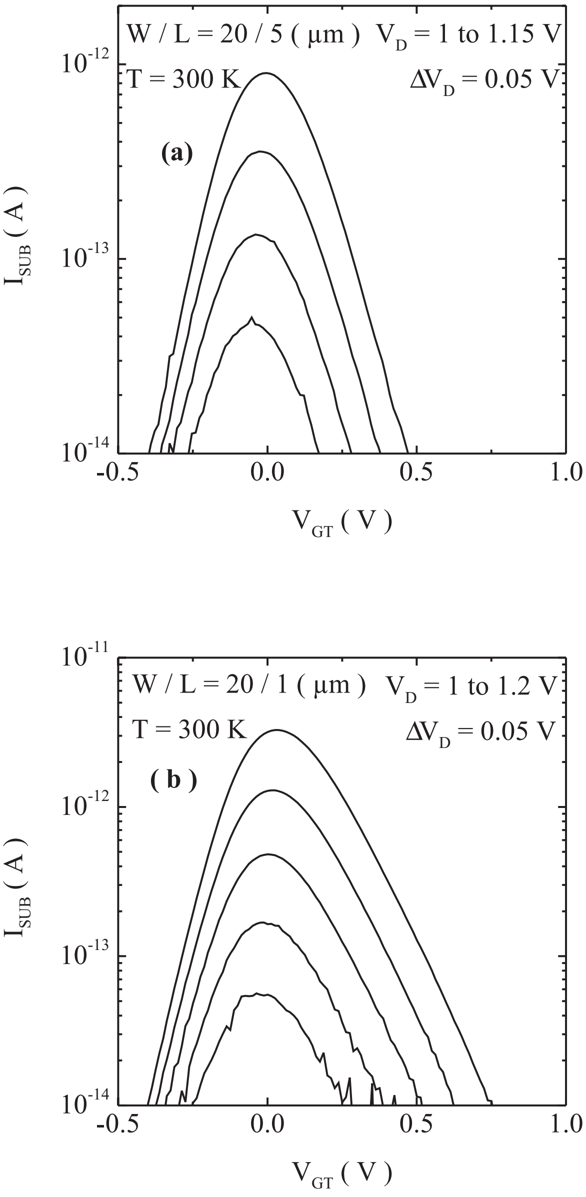


Figure 4.3: I_{SUB} vs V_G characteristics at 300 K near bandgap voltages in n-channel MOSFETs of L equal to (a) $5\,\mu m$ and (b) $1\,\mu m$. The curves for $1\,\mu m$ device are broader.

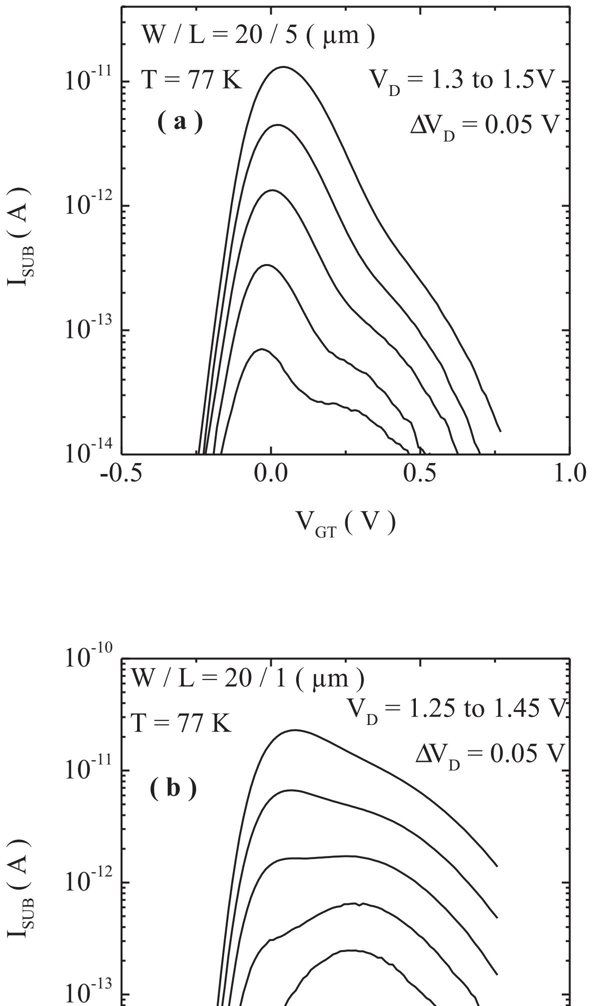


Figure 4.4: I_{SUB} vs V_G characteristics at 77 K near bandgap voltages in n-channel MOSFETs of L equal to (a) $5\,\mu m$ and (b) $1\,\mu m$. The curves for $5\,\mu m$ device shows a knee on the falling part. The data for the $1\,\mu m$ device show two peaks.

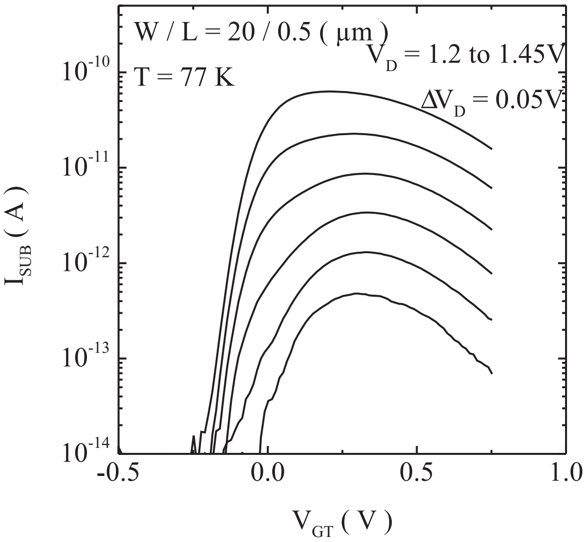


Figure 4.5: I_{SUB} vs V_G characteristics at 77 K near bandgap voltages in n-channel MOSFET of $L = 0.5\,\mu m$.

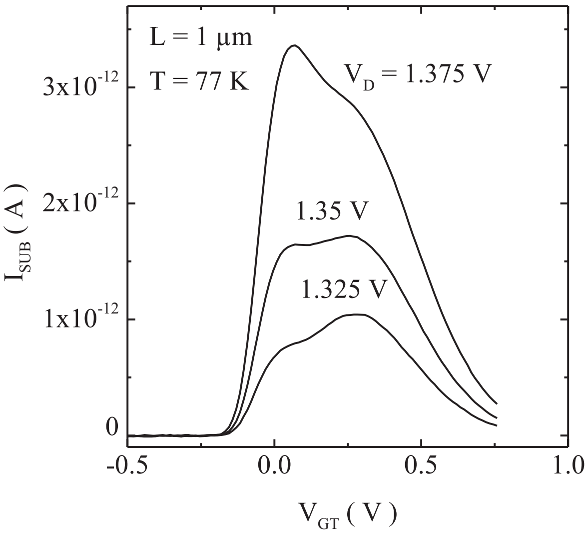


Figure 4.6: I_{SUB} vs V_G characteristics at 77 K near bandgap voltages in n-channel MOSFET of $L = 1\,\mu m$. The y-axis is linear.

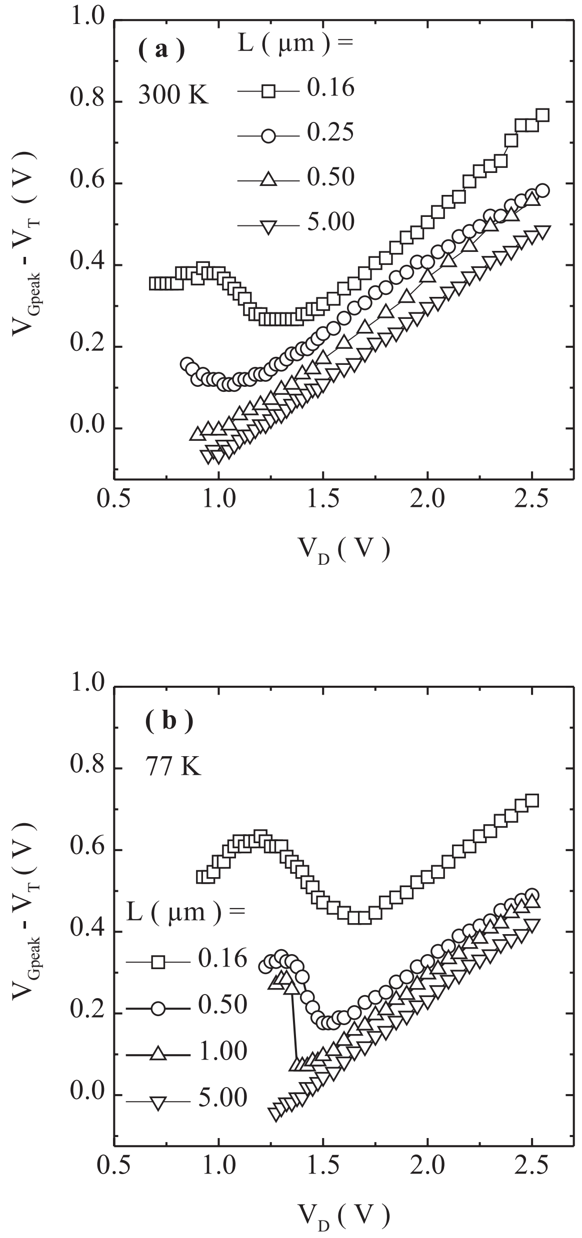


Figure 4.7: V_G at which I_{SUB} peaks as a function of V_D for devices of various Ls at (a) 300 K and (b) 77 K.

Figure 4.7b shows the data at 77 K for devices of $L = 5$, 1, 0.5 and 0.16 μm. For the 5 μm device, $V_{Gpeak} - V_T$ vs V_D is nearly linear with a slope of 1/2.5 . For the 1 μm device, V_{Gpeak} decreases for V_D down to 1.375 V and jumps to a higher value at 1.35 V, reflecting the two peak behavior depicted in figure 4.6. As L is reduced through 0.5 to 0.16 μm, the reversal in V_{Gpeak} occurs for higher V_D values and also the changes become smoother as compared to the 1 μm case.

Comparison of V_{Gpeak} vs V_D data at 300 and 77 K is also interesting. For the same L, (i) $V_{Gpeak} - V_T$ is higher at 77 K (ii) the abnormal reversal in V_{Gpeak} happens for longer devices at 77 K (iii) the reversal in the behavior occurs at larger V_D at 77 K (iv) for the 0.16 μm device, for $V_D < 1.25\,V$, the V_{Gpeak} is found to decrease again as the V_D is reduced at 77 K whereas it remains nearly constant for $V_D \leq 1\,V$ at 300 K.

The above results suggest that the abnormal reversal of V_{Gpeak}, as V_D is reduced, and the double peak in I_{SUB} vs V_G for the long channel devices at 77 K are manifestations of the same physical mechanisms.

4.1.3 Discussions

I_{SUB} vs V_G characteristics with two peaks were reported for n-channel MOSFETs by the University of California Berkeley (UCB) group [87, 88, 89]. In devices with weak gate to source overlap, double peaks were reported at room temperature [87, 88]. Similar characteristics were also reported for split gate devices at room temperature and 85 K [89]. The second peak in these cases was more prominent than in the results presented here. The second peak was reported for V_D even upto 6 V and $I_{SUBpeak}$ (for the second peak) values as high as 1 μA. I_{SUB} vs V_G in these cases could be split into two bell shaped curves. The bell shaped curve corresponding to the first peak lay in the saturation regime of the device characteristics whereas that corresponding to the second peak lay in the linear regime. These abnormal characteristics were explained by the UCB group as follows. The weak gate-to-source overlap devices have a high resistance region in the channel where the weak overlap is present. When the device is in the saturation regime, E_{LAT} peaks close to the drain junction. When V_G is increased, the peak lateral field ($E_{LATpeak}$) near the drain junction reduces. Consequently I_{SUB} also reduces. A second peak in E_{LAT} appears at the high resistance weak overlap region as the device is driven to linear regime. Impact ionization now start happening also in the weak overlap region giving rise to a second peak in I_{SUB} vs V_G characteristics. This was also shown to be true by 2-D drift-diffusion simulations.

I_{SUB} vs V_G characteristics with double peaks presented in this chapter is significantly different from the results of the UCB group in that (i) the double peaked behavior is observed only at 77 K (ii) the $I_{SUBpeak}$ corresponding to the second peak reported by the UCB group was in the range of micro Ampere whereas in our case, it is in the pico Ampere range (iii) the second peak, in our case, is observed within the saturation regime of device operation.

The last point assumes that the definition of saturation used in long channel device theory, $V_D > V_G - V_T$ [86], is valid for our devices. This is the case atleast for the long channel devices presented.

The kind of I_{SUB} vs V_G characteristics reported by the UCB group were observed for asymmetrical channel devices and will be discussed at length in a subsequent chapter where we make a clear distinction between the physical mechanisms responsible in either cases.

F. Balestra et al. [47] reported an anomalous increase in the V_{Gpeak} for n-channel devices of $L = 0.15\,\mu m$ for low V_D at 77 K. A careful inspection of the data reported by A. Hori et al. [48] and by S. Odanaka and A. Hiroki [49], though not seems to have caught the attention of the authors, also reveal such an anomalous behavior. However, these observations remain largely neglected and unexplained.

The discussion above suggest that the present work is the most comprehensive experimental investigation of impact ionization in n-channel MOSFETs for V_D values near the impact ionization threshold voltages known to the author. It is desirable to look for possible explanations for the novel results presented. This is attempted in subsequent sections.

4.2 Analysis

The maximum potential drop that an electron experience as it is transported from source to drain is qV_D. In addition, the source to channel barrier sample the source distribution at a higher energy than the conduction band bottom and this should also be added to the average energy of the electrons [11, 12, 13]. As pointed out in chapter 2, additional energy gain or redistribution mechanisms must be considered in explaining impact ionization for $V_D < 1\,V$. Electron-electron interactions (EEI) and electron-phonon interactions (EPI) were proposed my Monte-Carlo (MC) simulation groups as potential candidates. The strength of the former is widely debated and the existence of the later is yet to be confirmed experimentally. In the following we will analyze the data presented so far to provide experimental evidence for LTDT and assess the strength of short-range EEI (SREEI).

4.2.1 Experimental Verification of the Nature of the Tail of EED

EED predicted by MC simulation groups are central to the experimental design and discussions that follow. We had briefly discussed the EED in figure 2.4. The high energy part of EED based on the data in [23, 38] is shown in figure 4.8. The part upto point A in the figure represents field heating and the tail is either dominated by EPI when the electron concentration is low or by EEI when there are sufficiently high density of electrons [23, 65]. The temperature dependence of EEI tail is controversial. The simulations of Fischetti et al. [13, 38] show a tail that is independent of lattice temperature. The results of Ghetti et al. [23] show a broader tail at lower temperatures. The conclusions derived here are independent of the temperature dependence of EEI broadening of the tail. Thermal tails for two temperatures T1 and T2 are shown. Point A where the EED changes from field heated part to the tail is referred to as TC (stands for “Transition Corner”) hereafter.

According to the definition in [90], I_{SUB} can be estimated as the integral of the product of electron current density and the ensemble average of impact ionization rate over the spacial domain in which impact ionization occurs. The later is evaluated by integrating the product of EED and the microscopic impact ionization rate of electrons having energy above W_G in the system. The microscopic impact ionization rate can be

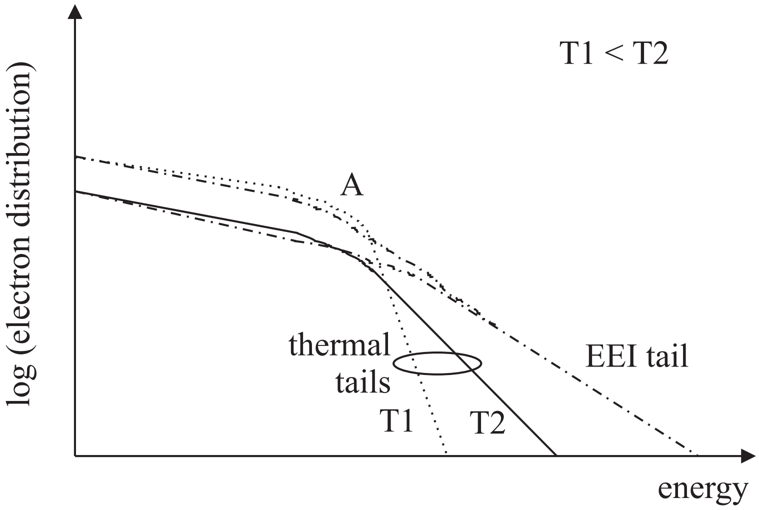


Figure 4.8: Schematic of EED showing the thermal tail at two temperatures and EEI broadening of the tail. Based on the data published in [23, 38]. The point A shows the transition of the distribution from the field heated part to the tail and is called the transition corner.

experimentally determined [24]. The ratio of I_{SUB} to I_D (M) can be used as a sensitive probe of the ensemble average of the impact ionization rate and hence the integral of EED above W_G.

For a chosen V_D, the population of the high energy part of EED decreases as V_G is swept from subthreshold to above threshold. This is easily established. When V_G is low, significant part of V_D drops over a small length near the drain junction. In our devices, this length is as low as $50\,nm$ (refer to figure 3.10) which is of the order of one energy relaxation length in silicon. Consequently a significant number of the electrons can gain an energy that is nearly qV_D. When V_G is very high so that the device is in the linear region, V_D drops over the entire length of the channel. For a $0.2\,\mu m$ device, that implies many energy relaxation lengths. The number of electrons gaining qV_D of energy will be significantly lower. We can state that TC moves to the left due to the reduced population beyond W_G. If V_D is chosen so that during such a sweep of V_G, TC is located in the vicinity of W_G, I_{SUB} is dominated by contribution from the tail which is either due to EEI or thermal tail, if the ensemble MC simulation predictions are correct. For an appropriate choice of V_D, EEI dominated tail can be probed at V_G much higher than V_T. The thermal tail can be effectively probed by measurements at different temperatures in the subthreshold region or just around V_T.

I_{SUB} and M measured at different temperatures for $V_D = 1.1\,V$ are shown in figure 4.9a. V_T values measured for $V_D = 1.1\,V$ are subtracted from V_G. The decrease in I_{SUB} as the temperature is reduced in this range of V_D is well known and MC simulations have reported that it is due to the increase of W_G [38]. Corresponding values of M are shown in figure 4.9b.

In figure 4.9b, M decreases as the temperature is reduced. M vs V_{GT} data show distinctly different behavior in the subthreshold and above threshold regions as the temperature is varied. For $V_{GT} > 0.3\,V$, M decreases consistently as V_G is increased and the data are nearly parallel for all the temperatures. For $V_{GT} < 0.1\,V$, M decreases

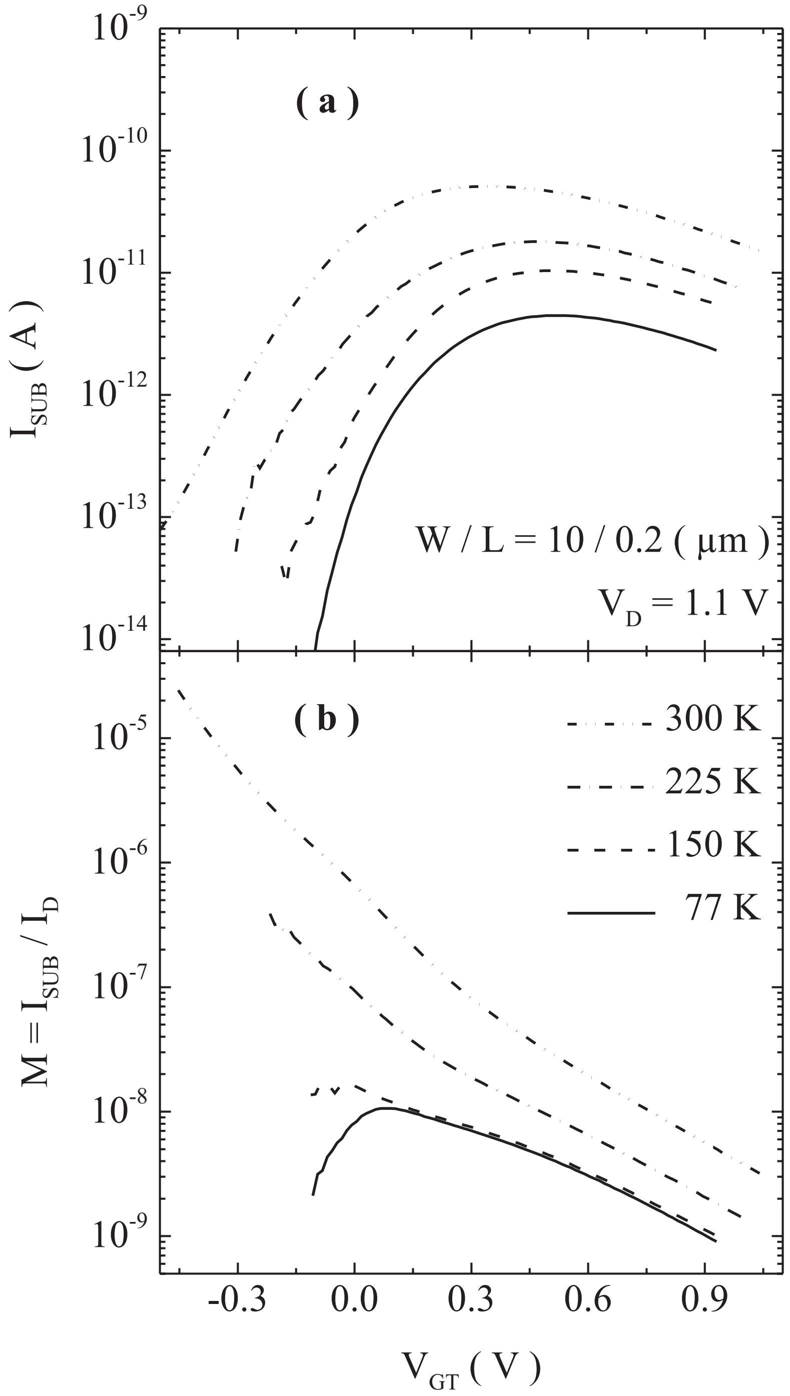


Figure 4.9: I_{SUB} measured for a V_D of 1.1 V, which is close to the bandgap voltage of silicon, at various temperatures, (a). M is shown in (b). M is significantly suppressed in the subthreshold regime as the temperature is lowered.

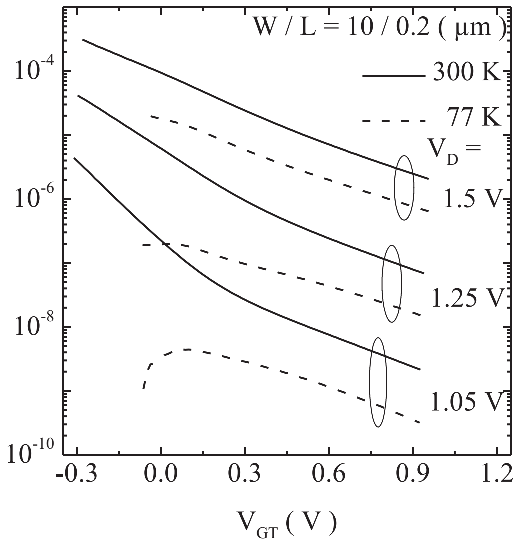


Figure 4.10: M measured as a function of V_G for various drain biases at 300 and 77 K. The peak in the data at 77 K in the low V_D case disappears as V_D is increased, reflecting the diminishing contribution of the tail to impact ionization.

for 300 K whereas it increases for 77 K as V_G is increased. M is greatly suppressed in the subthreshold region at 77 K compared to 300 K. For example, at $V_{GT} = 0.9\,V$, the ratio M_{300K}/M_{77K} is about 5.4, whereas at $V_{GT} = -0.1\,V$, it is about 624. The data at 150 K and 225 K show that the variations are systematic with variations in temperature. It may be noted that such differences are not apparent in I_{SUB} data.

Figure 4.10 compares M vs V_{GT} for $V_D = 1.05$, 1.25 and $1.5\,V$ at 300 and 77 K. For $V_D = 1.5\,V$, the data at 300 and 77 K are nearly parallel. As V_D is reduced the difference between M at 300 and 77 K widens dramatically for $V_{GT} < 0.1\,V$ regime compared to $V_{GT} > 0.3\,V$ regime. For $V_D = 1.05\,V$ at 77 K, the data show a peak just as in the case for 1.1 V.

For $V_D = 1.5\,V$, the contribution to I_{SUB} comes predominantly from the field heated part of the EED. The higher population of the field heated part at 77 K due to the reduced phonon scattering is not sufficient to compensate for the loss in the area under the EED beyond W_G due to the increase in W_G resulting in a reduced I_{SUB} and M at 77 K. The monotonous decrease of M as V_G is varied from subthreshold to much above threshold is due to the decreasing population of the EED beyond W_G as was discussed previously.

The great reduction of M in the subthreshold regime for $V_D = 1.1\,V$ and below, at 77 K can be explained as follows. In this regime of V_G, the major contribution to the area under EED beyond W_G is from the thermal tail as the contribution of EEI is insignificant due to the low electron concentration in the channel. So, the dramatic reduction of M in the subthreshold regime as the temperature was reduced is a signature of the thermal tail of the EED. However, the results presented do not verify the slope of the tail. The result verifies the presence of a lattice temperature dependent tail in the EED experimentally for the first time in the literature.

The peak in M data at 77 K seen in figure 4.9 is now easy to comprehend. As V_G is increased, TC in EED is moving towards the left. Even though the tail is expected to broaden due to EEI, the movement of TC to the left dominates, consequently the area under the EED above W_G decreases, causing the monotonous decrease of M. But at 77 K, LTDT is steeper and consequently the area under EED above W_G is significantly suppressed in the subthreshold regime. If only LTDT was present for the entire range of V_G, M should have decreased monotonously. As V_G is increased, even though TC is moving towards the left, there is a small range of V_{GT} in which the increase in the area mentioned above due to the movement of TC to the left is superseded by the increase in the area contributed by EEI. The suppression of LTDT at low temperatures gives a greater visibility to EEI broadening of the tail at such temperatures. The peaks in M at 150 and 77 K are clear signatures of EEI broadening of the tail. As V_D is increased, the significance of the tail decreases in comparison to the field heated part of EED.

4.2.2 Relative Strength of the Thermal and EEI Broadened Tails

The works of Abramo et al. [65] and Ghetti et al. [23] predicted that EEI broadening of the tail is important for electron concentrations above $10^{17} cm^{-3}$. In figure 4.9, at 77 K, M vs V_G has a positive slope for $V_{GT} = -0.1\,V$, suggesting that EEI broadening of EED tail is important even in the subthreshold regime and may be stronger than predicted in [23, 65].

V_D below which the contribution of the tail is significant in comparison to the field heated part of EED is controversial [23, 25]. We investigated this by comparing M for various bias conditions.

To illustrate the impact of EEI on the tail of the EED, MC simulation groups have compared EED obtained with and without EEI [23, 38, 65, 68]. In fact, experimental evidence to the role of EEI was provided by the observation that, when EEI is turned-off in simulations, M was underestimated in comparison to measured data [23]. Good match of simulation and measurement was found when EEI was turned-on. An experimental variant of this technique is to investigate M in the subthreshold regime (turn-off EEI) and in the above threshold regime (turn-on EEI).

M measured for $0.2\,\mu m$ device for $V_{GT} = -0.1$ and $0.5\,V$ at 300 and 77 K are shown in figure 4.11. M decreases as V_D is decreased for all the cases and this is due to the decreasing population of the EED beyond W_G. A careful examination reveals that M at 77 K falls much faster in the subthreshold regime than in the above threshold regime in comparison to the data at 300 K. Since for identical V_D, M in subthreshold regime is greater than that in the above threshold regime for most of the V_D range, we take the ratio $M_{77\ K}/M_{300\ K}$ to highlight the temperature dependence. Figure 4.19 shows M_{77K}/M_{300K} for $V_{GT} = -0.1$ and $0.5\,V$. The ratio shows how fast M at 77 K falls in comparison to that at 300 K when V_D is reduced. Below a V_D of about 1.6 V, the ratio for the subthreshold regime falls dramatically in comparison to that for the above threshold regime. From the behavior of the ratio in the subthreshold regime, we can deduce that LTDT contribute significantly to the impact ionization process for V_D below 1.6 V. For $V_{GT} = 0.5\,V$, the tail is dominated by the EEI broadened part. EEI broadening is less sensitive to temperature and hence the ratio of M's is showing lesser variations at low V_D. The experimental estimate of the V_D below which contribution of the tail is significant, found here is comparable to the $1.6\,V$ reported in [23] and

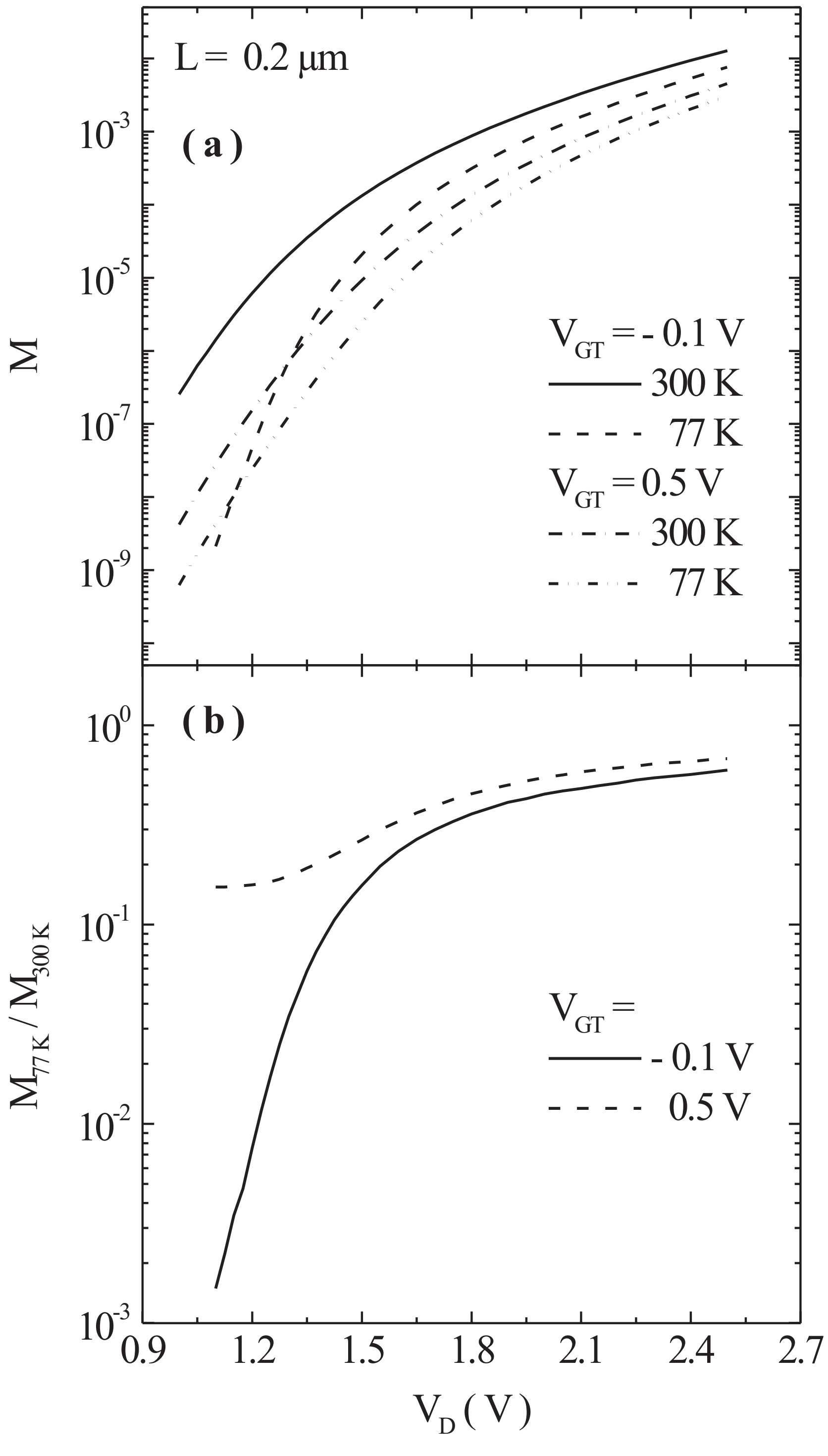


Figure 4.11: Relative strength of the tail. (a) M as function of V_D for $V_{GT} = -0.1$ and $0.5\,V$ at 300 and 77 K. At 77 K, M decreases more rapidly as V_D is decreased in the subthreshold regime compared to the above threshold regime. (b) the ratio $M_{77\text{ K}}/M_{300\text{ K}}$ shows the temperature sensitivity of the tails more clearly.

higher than the 1.2 V reported in [25].

One minor comment regarding the relative contributions of the SREEI and LREEI is in order. The direct contribution to EEI tail from the long-range component, as discussed earlier, is independent of the concentration of the electrons transported across the high field region, which is proportional to the inversion layer electron concentration. The clear V_{GT} dependencies observed in figures 4.9, 4.10 and 4.19 does not favor a direct role for the long-range component as an efficient process that can broaden the EED tail for the device structure investigated in this work. This is in disagreement with the predictions of Fischetti and Laux [38]. An indirect role for LREEI by enhancing the SREEI can not be ruled out.

4.2.3 Inversion Layer Quantization as an Energy Gain Mechanism

ILQ has non negligible effects on the characteristics of scaled MOSFETs [86]. The depletion region at the surface of the device is effectively a potential well. This well gets narrower as the doping concentration increases, as required by device scaling, leading to significant quantization in modern VLSI devices. Stern and co-workers at IBM studied the effects of ILQ on device characteristics by analytically solving the Schrödinger wave equation assuming a triangular potential well for the depletion region [91, 92]. Dorda provided an experimental verification for the ILQ by studying changes in effective mass of electrons in inversion layers observed by piezo resistance [93]. Triangular potential well approximation is valid in the subthreshold and weak inversion regimes of device operation. A more accurate method of investigating the issue is by consistently solving Poisson and Schrödinger equations [94]. ILQ leads to increase in V_T [92], mobility degradation [95] and consequent degradation in the drive current of MOSFETs.

In this section, we investigate the possible impact of ILQ on EEDs and hence the hot-carrier effects by employing SCHRED, a one dimensional consistent Poisson-Schrödinger solver developed at the Arizona State University. The details of the simulator are described in [94] and the references there in. $Si - SiO_2$ interface is parallel to the $< 100 >$ plane in most of the MOS devices. Consistent with this, two sets of parabolic subbands, one with a 2-fold degeneracy and another with 4-fold degeneracy, were assumed in the simulation model. A maximum of 10 and 8 energy levels can be simulated in the 2-fold and 4-fold subbands respectively. In all the simulation results presented below, Fermi-Dirac statistics were used. The simulator can handle arbitrary doping profiles in silicon region. In the results presented below, doping profiles obtained from process simulations corresponding to the experimental devices have been used. A metal gate has been assumed in the simulations. This does not have any impact on the conclusions of this section.

Figure 4.12 shows quantized energy levels in the conduction band as V_G is varied. The conduction band edge is used as the reference. 9 levels in the 2-fold subband and 7 in the 4-fold subband were simulated. Only those energy levels which have a minimum occupation of 1% are shown. The solid lines correspond to the energy levels in the 2-fold subband and the dashed lines those in the 4-fold subband. The numbers on the right are the corresponding eigen values. The unprimed ones correspond to the 2-fold subband and the primed ones to the 4-fold subband. The levels have increasing energy

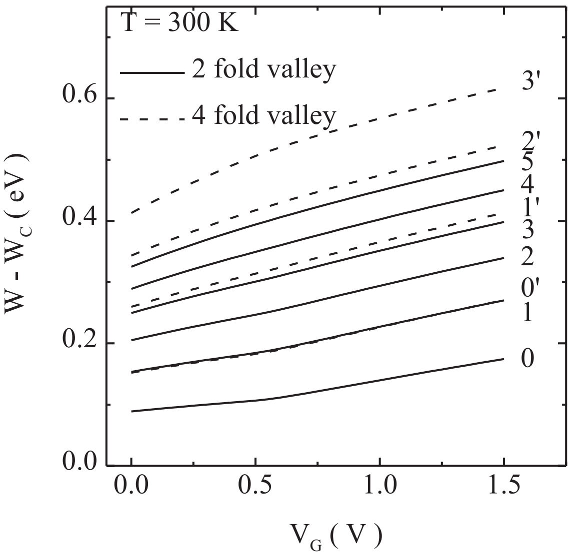


Figure 4.12: The quantized energy levels in the 2-fold and 4-fold valleys in a parabolic conduction band structure approximation obtained using a consistent 1-D Poisson-Schrödinger solver, SCHRED [94]. Doping profile used was obtained by process simulations corresponding to the experimental process flow. The eigen values corresponding to the energy levels are shown on the right hand side. The unprimed ones correspond to the levels in the 2-fold valley and the primed ones correspond to the levels in the 4-fold valley.

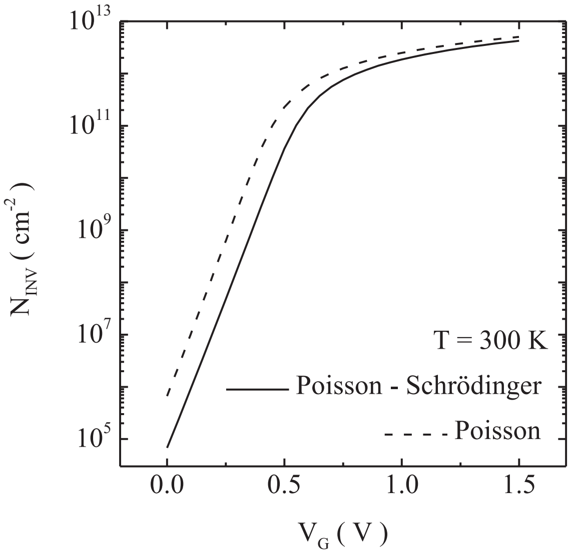


Figure 4.13: The difference in the inversion layer charge densities obtained by consistent Poisson-Schrödinger and Poisson solutions. Quantization result in a shift in V_T.

as V_G is raised. The lowest level has energy of 90 to 180 meV for a V_G variation of 0 to 1.5 V. Also note that the highest level occupied has an energy of about 600 meV.

Figure 4.13 shows inversion layer charge density obtained by classical and quantum mechanical simulations. ILQ result in a shift of the charge vs V_G curve to higher V_G. This is because the lowest energy level that the electrons can occupy is higher by the $W_0 - W_C$ off-set compared to the classical case. Since the same distribution functions are assumed in both the cases, the band bending has to be higher in the quantum mechanical case to obtain the same inversion layer charge as in the classical case. This requires a higher V_G in the quantum case and consequently V_T increases.

Figure 4.14 compares the off-set of the lowest energy level from the conduction band edge with the additional band bending required in the quantum case to obtain the identical inversion layer charge density. The additional band bending, $q\Delta\Psi_S$, was obtained by subtracting the band bending obtained for the classical case from the band bending for the quantum mechanical case for identical inversion layer density. The condition of identical inversion layer density is important because when measurements are done on real devices, there is no way of “turning off” the quantization effect and the effect of quantization is embedded in the measured variables. So it can be argued that V_T include the additional band bending and hence the lowest energy level. van Dort et al. [96] proposed a model for the increase in V_T by considering the lowest energy level as the new conduction band edge. The additional band bending required for identical inversion charge using such a model is greater than $W_0 - W_C$. The self consistent simulation results presented in figure 4.14 shows that such an approximation is not always valid. The additional band bending required is smaller than the $W_0 - W_C$ off-set.

This is more clearly illustrated in the schematic shown in figure 4.15. The conduction band edge in the depletion region is shown for the classical and quantum mechanical cases. Identical inversion layer charge condition is enforced. The lowest energy of the electrons in the quantum mechanical case is higher than the classical case by

$$\Delta W = W_0 - W_C - q\Delta\Psi_S \tag{4.1}$$

Eitan et al.[11], Bude et al. [12] and Fischetti and Laux [13] noted that the maximum energy that can be gained by the electrons on being accelerated from the source to drain is qV_D plus the source to channel barrier height. The results presented in this section so far suggest that the effective barrier height is enhanced by ΔW, given by equation 4.1, due to ILQ. This concept is further illustrated in figure 4.16. The figure shows the schematic of a MOSFET in saturation regime of operation. The channel region is quantized due to the high vertical field. The minimum energy of the electrons is higher even though the electrons are in equilibrium with the lattice. In the pinch-off region, electron confinement perpendicular to the $Si - SiO_2$ interface is insignificant due to the high E_{LAT}. The direction of the effective field in this region is lateral.

The effect of the increasing V_G is to enhance the electron confinement in the channel region resulting in higher minimum energy for the electrons. The increase in V_{Gpeak} reported in figures 4.7a and 4.7b may partly be due to this enhanced energy gain resulting from ILQ.

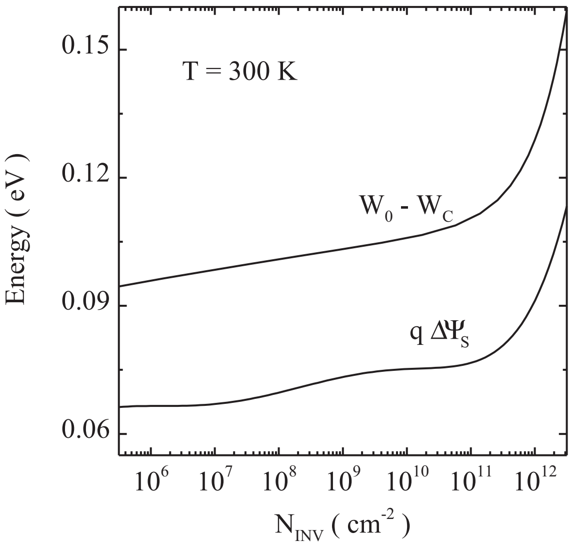


Figure 4.14: The off-set of the lowest energy level in the 2-fold valley from the conduction band edge compared to the additional band bending required to obtain identical inversion layer charge density as V_G is varied.

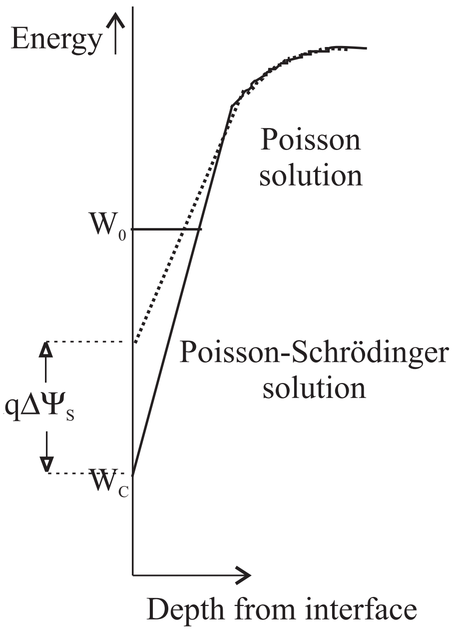


Figure 4.15: Schematic of the conduction band edge in the silicon inversion layer for both Poisson (dotted line) and Poisson-Schrödinger (solid line) solutions for identical inversion layer charge density. An additional band bending is required in the quantized case to obtain identical inversion layer charge as in the classical case. The lowest energy level that can be occupied by the electrons is higher compared to the conduction band edge in the classical case.

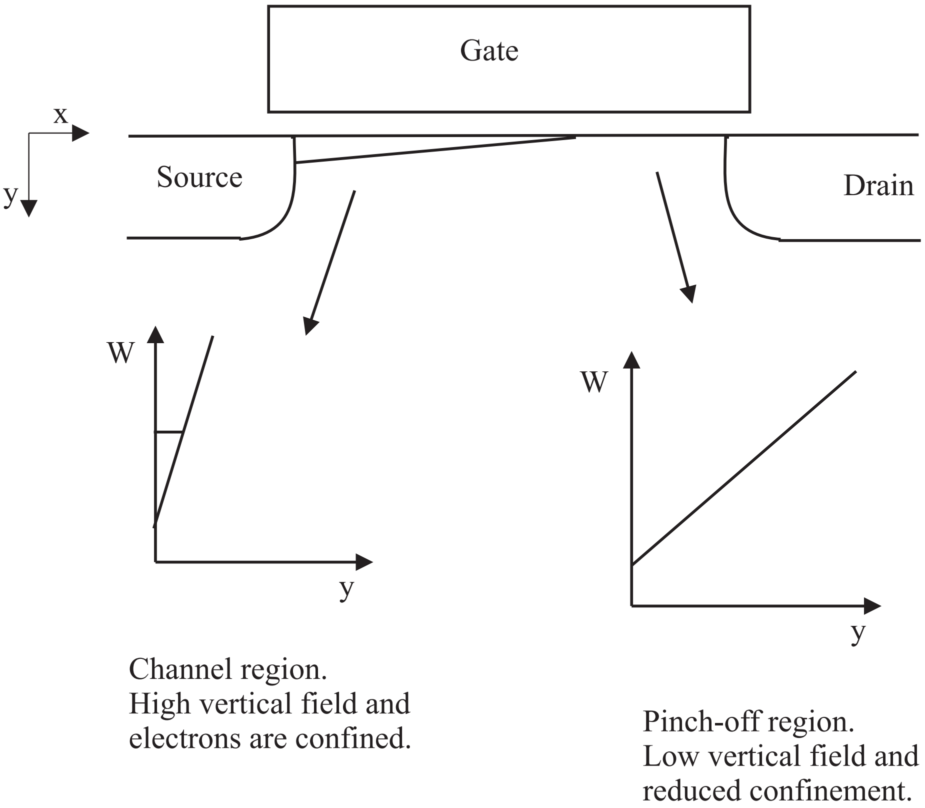


Figure 4.16: Schematic illustrating the concept of ILQ as an energy gain mechanism in the saturation regime of device operation. In the channel region of the device, the conduction band is quantized. In the pinch-off region, due to the high lateral field, the electron confinement is significantly lower.

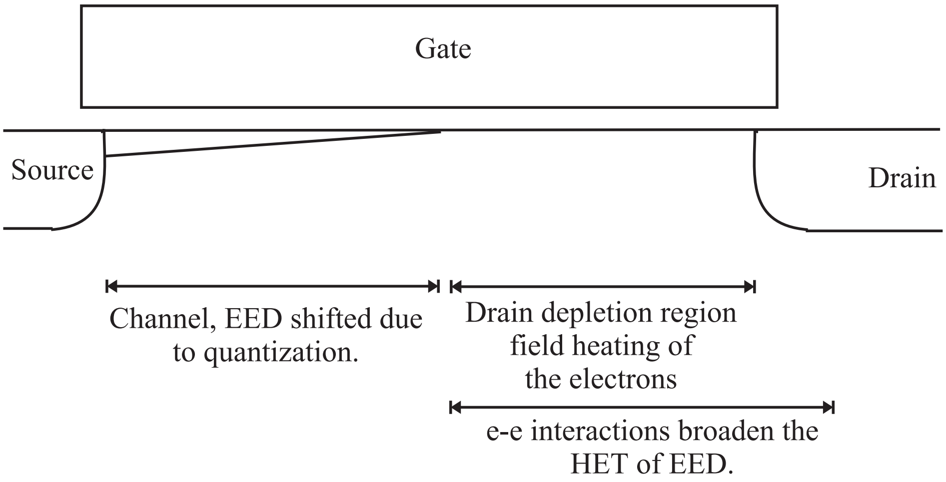


Figure 4.17: Energy gain and redistribution mechanisms discussed in this chapter and their physical location of importance in a MOSFET.

The additional energy, ΔW, due to quantization varies from about 30 to 50 meV as the gate is driven from the subthreshold regime to above threshold, figure 4.14. Whether such small contributions are important is a valid question. We have already seen in chapter 3 the impact of a 40 meV increase in W_G on I_{SUB}. We are discussing a process near its threshold where every tiny contribution is to be counted.

The results presented in this section so far have suggested that the EED can have an initial off-set due to ILQ and this can be a significant energy gain process at very low V_D. Quantitative assessment of this contribution would require simulation tools that self consistently handle Poisson-Schrödinger simulations and MC technique. Two dimensional Poisson-Schrödinger simulations remain a challenge. One of the alternate approaches to the problem is to apply a quantum correction to the potential obtained from the solution of the Poisson equation in a Poisson-Monte Carlo self consistent scheme. Ferry et al. recently reported such a scheme with illustrative simulations on 50 nm channel length MOSFETs [28]. They reported a 10% increase in the average energy of electrons in the channel, for a V_D of 1 V, when the quantum correction to the potential was applied. This is higher than the ΔW values we have obtained. The reasons may be the following. The channel doping in the devices simulated in their work was $10^{18} cm^{-3}$, higher by a factor of 2.5 than in our experimental devices. The oxide thickness was 2 nm, whereas our devices have an oxide thickness of 3.6 nm. This means stronger quantization effects in their devices. The work of Ferry et al. lend support to the ideas presented in this section.

4.2.4 Location of Action of Various Energy Gain and Redistribution Mechanisms

All the energy gain and redistribution mechanisms discussed so far and the regions of their action in a MOSFET are schematically shown in figure 4.17. The EED is shifted due to ILQ in the channel region. These electrons are accelerated in the high lateral electric field in the pinch-off region. The EED is further broadened by EEIs.

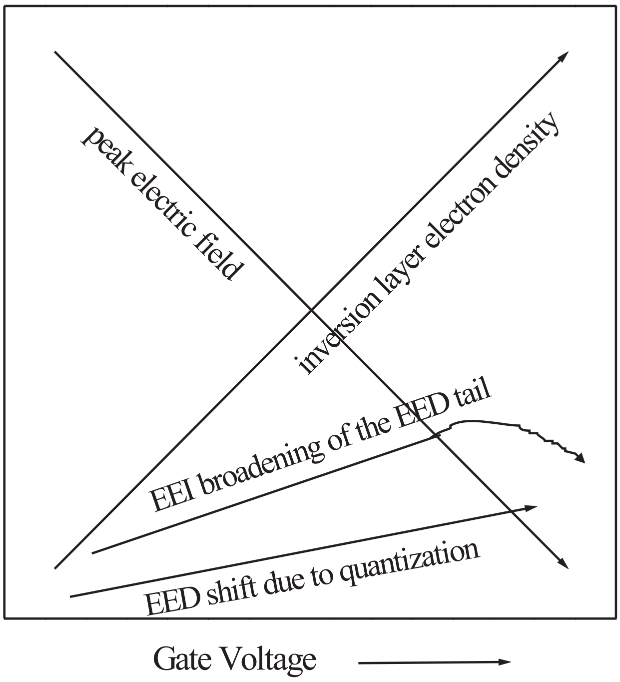


Figure 4.18: Schematic of V_G dependencies of various energy gain and redistribution mechanisms for a given V_D. Schematic of V_G dependence of the inversion layer charge is also shown. The differences in the dependencies may lead to multiple peaks in I_{SUB} vs V_G curves.

We have already seen that the SREEI are effective in broadening the EED only when the electrons have sufficiently large energy to exchange. So they are important in the pinch-off region and the drain region close to the junction. Even though we could not confirm the role of LREEI in broadening the EED tail, they may be important in the drain region close to the junction, where the high energy channel electrons interact with the cold drain electrons. A possible means to investigate the role of LREEI is suggested in the following chapter.

4.2.5 Explanation of the Peaks in I_{SUB} vs V_G

In this section we would attempt to provide an explanation for the double peaks observed in I_{SUB} vs V_G characteristics presented in a previous section.

The well known single peaked I_{SUB} vs V_G characteristics are explained as follows in the literature [32, 34]. When $E_{LATpeak}$ is sufficiently large, the channel electrons initiate impact ionization in the high field region near the drain junction. As V_G is increased, two things happen. The number of the channel electrons and hence the channel current increases which means an increase in the electrons that are potential candidates to initiate impact ionization. Simultaneously, $E_{LATpeak}$ is also decreasing, reducing the impact ionization rate. I_{SUB} peaks for that V_G for which these two controlling factors optimize.

This picture can be easily rewritten from the perspective of EED as follows. The number of electrons that are potential candidates to initiate impact ionization increases as V_G is increased. Simultaneously, the population of the EED beyond W_G, responsible for impact ionization, decreases. This monotonously decreasing relative occupation of the high energy part of the EED and the monotonously increasing number of electrons available to initiate impact ionization as V_G is increased, result in a bell shaped I_{SUB} vs V_G curve. The peak in such a curve is the point at which the contributions of decreasing field heating and increasing electron concentration optimize. It is well known that a monotonously increasing function and a monotonously decreasing function of the same variable has a single optimization point in a given interval of the variable. It is assumed that the functions have finite values in the interval.

We have already seen that such a conventional picture is valid only when V_D is significantly high. As V_D approaches the bandgap voltage, contributions of EEI broadening of the tail and EED shifting due to ILQ may not be ignored.

A schematic of V_G dependencies of the various energy gain and redistribution mechanisms, for a given V_D, is summarized in figure 4.18. V_G dependence of the inversion layer charge is also shown. The schematic does not show exact functional dependencies. $E_{LATpeak}$ decreases with increasing V_G and hence the field heating decreases. The inversion layer charge increases as V_G increases. For high V_D, this leads to a single peak in the I_{SUB} vs V_G characteristics. When V_D approaches the bandgap voltage, EEI broadening of the EED tail and the shift in EED due to ILQ contribute significantly to populating the EED beyond W_G. The later contribution increases as V_G is increased. As discussed in section 2.4.2, EEI is an energy redistribution mechanism and will be less effective in populating the EED beyond W_G, as the energy gained from the field becomes very small. Eventually EEI induced filling of the high energy tail may reduce. This point will be experimentally proved in section 4.2.8. When all these factors are considered, the shape of I_{SUB} vs V_G is an optimization problem involving four functionals of V_G and hence can have multiple peaks.

The above arguments suggest the possibility of observing multiple peaks at all temperatures. But experimentally we have observed the double-peaked I_{SUB} vs V_G only at 77 K, not at 300 K. This can be explained as follows. When EEI are still weak, in the subthreshold region or just about V_T, that part of EED beyond W_G is dominated by the thermal tail and field heating. The two peak data for the 5 μm device at 77 K can be conceptually split into two bell shaped curves. If we compare the bell shaped curve at 77 K corresponding to the first peak to the bell shaped curve at 300 K, it is apparent that the former is narrower than the later. The steeper rising part is due to the increased subthreshold slop at 77 K. The steeper falling part arguably signifies the contribution of the thermal tail. At 300 K, the broader thermal tail result in a smooth transition from the electric field dominated regime to the EEI dominated regime in the EED. The narrower thermal tail at 77 K result in a sharper fall of the first bell shaped part making the EEI dominated regime distinctly visible with a characteristic peak. The lower bound of the tail is the thermal tail. Consequently, the tail has greater maneuverability at 77 K than at 300 K.

4.2.6 Correlation between Electron-Electron Interactions and Anomalous V_{Gpeak} Behavior

We have already seen the temperature dependence of M for various V_{GT} conditions and evaluated the strength of EEI. Figure 4.19 correlate $M_{77\,K}/M_{300\,K}$ to the trend of V_{Gpeak} as V_D is varied. The data are shown for a device of channel length $0.2\,\mu m$. At 77 K, V_{Gpeak} reverses for $V_D < 1.6\,V$. We see that M ratio in subthreshold also start its rapid fall around $V_D = 1.6\,V$. We had already identified this value of V_D as that at which the contribution of the tail start showing up at 77 K. We had also seen that the reversal of V_{Gpeak} is a manifestation of the second peak in I_{SUB} vs V_G. This strong correlation between the ratio of M values and V_{Gpeak} reversal support the idea that the second peak is due to EEI. At 300 K, V_{Gpeak} reversal happens for $V_D < 1.2\,V$. This is because the thermal tail is stronger at 300 K and the EEI tail in comparison, gain importance at smaller V_D values than at 77 K.

4.2.7 Channel Length Dependence of I_{SUB} vs V_G Curves

Experimentally observed L dependence of the shape of I_{SUB} vs V_G curves can be summarized as follows. At 300 K, the curves became broader with decreasing channel length. An anomalous V_{Gpeak} turn around for $L \leq 0.25\,\mu m$ was observed. At 77 K, the $5\,\mu m$ device showed a knee on the falling part of the curve and the knee became a distinctly visible peak for $L = 1\,\mu m$. As L was decreased through 0.5 to $0.16\,\mu m$, the two peaks merged with one another. This reflect as a transition of abrupt jump in V_{Gpeak} vs V_D for the $1\,\mu m$ device to the smooth data for the $0.16\,\mu m$ device. For smaller devices, V_{Gpeak} vs V_D first increases as V_D is increased and then decreases and then increases again.

We have also observed an increasing difference between the lowest V_D at which impact ionization occurs at 300 and 77 K as L is increased, figure 4.2.

In the following we explain these L dependencies based on E_{LAT} profiles obtained from 2-dimensional drift-diffusion simulations done using MINIMOS. The simulation model used was already described in chapter 3.

Measured M for a V_D of 2.5 V for devices of $L = 0.5$ and $5\,\mu m$ at 300 K are compared with simulated $E_{LATpeak}$ in figure 4.20. $E_{LATpeak}$ shown are at 1 nm below the $Si-SiO_2$ interface. L and V_G dependencies of M are replicated by $E_{LATpeak}$. M is nearly independent of L in the subthreshold regime. As V_G is increased, M decreases, but the decrease is slower for the shorter device than the longer one. For example, for $V_{GT} = 0.9\,V$, $E_{LATpeak}$ and hence M, is larger for the $0.5\,\mu m$ device than the $5\,\mu m$ device.

Temperature dependence of $E_{LATpeak}$ is shown in figure 4.21. The figure shows data at 300 and 77 K for $V_D = 1.3\,V$. $E_{LATpeak}$ in the subthreshold regime is slightly lower at 77 K than at 300 K. This may be due to the reduced ionized impurity concentration due to partial freeze out at 77 K [39]. For the $5\,\mu m$ device, as V_G is increased, the fall in $E_{LATpeak}$ is slower at 77 K, and at sufficiently high V_G, the 77 K values catch up with the 300 K values. For the $0.5\,\mu m$ device, $E_{LATpeak}$ is higher at 77 K than at 300 K for $V_{GT} > 0.5\,V$. The important point here to note is that at 77 K, $E_{LATpeak}$ decreases at a lower rate than at 300 K with increase in V_G.

For the shorter device, $E_{LATpeak}$ is higher than the longer device in the above

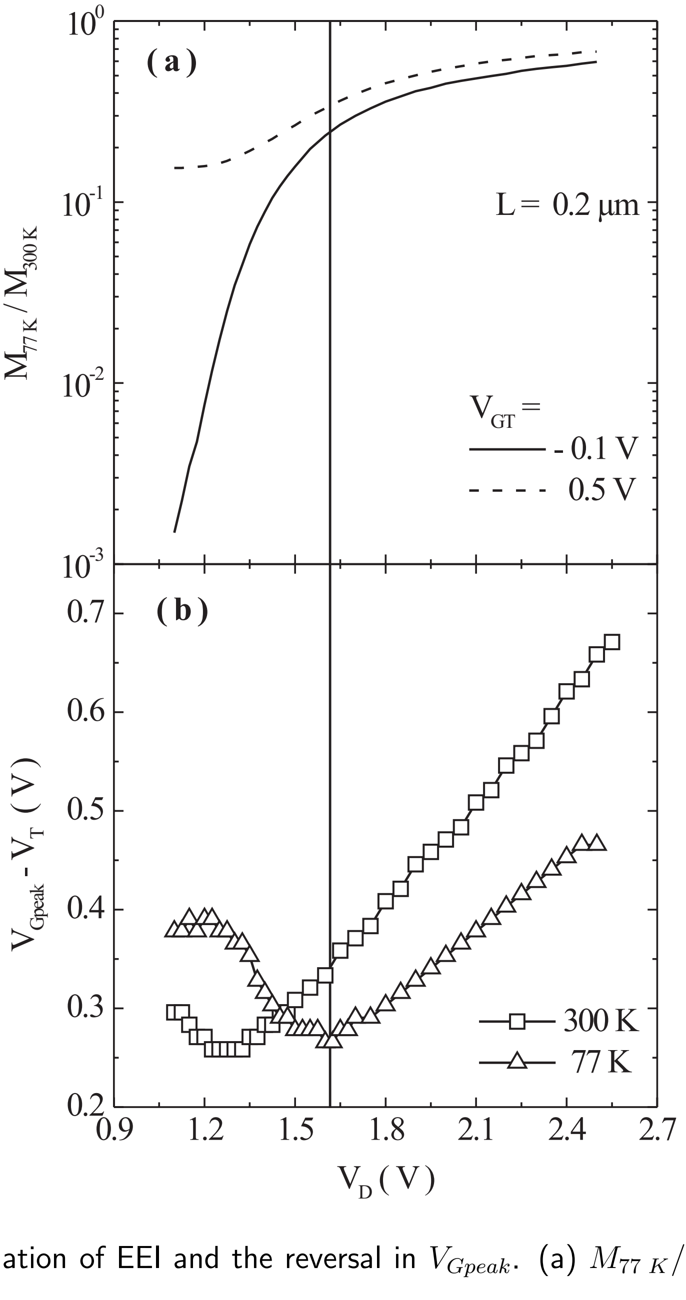


Figure 4.19: Correlation of EEI and the reversal in V_{Gpeak}. (a) $M_{77\ K}/M_{300\ K}$ (b) V_{Gpeak} vs V_D.

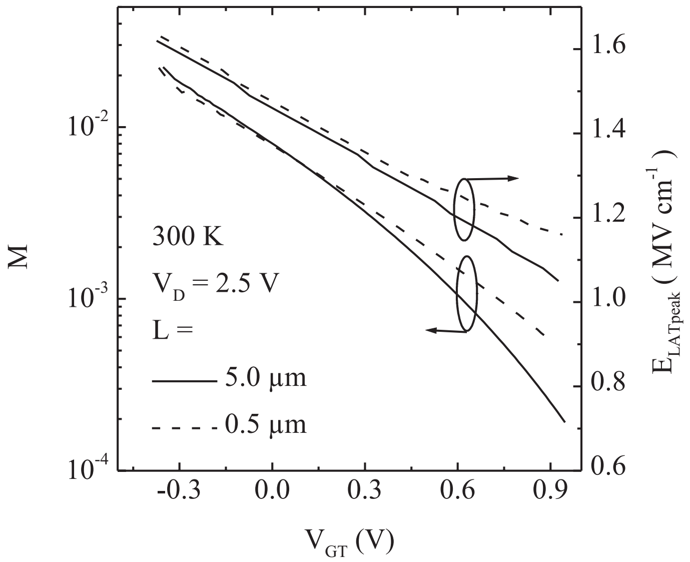


Figure 4.20: Comparison of the measured M, left vertical axis, and simulated $E_{LATpeak}$, right vertical axis. The trends in $E_{LATpeak}$ replicate the trends in M for the long and short channel devices.

threshold regime. This is true both at 300 and 77 K. This means that in the above threshold regime, high energy part of the EED is more occupied in the case of the shorter device. Since EEI is an energy redistribution mechanism, broadening of the EED tail will be stronger for the shorter device. These factors result in a broader I_{SUB} vs V_G as L is reduced. The second peak is strengthened as the device channel length is reduced, because of the favorable increase in $E_{LATpeak}$ and the consequent strengthening of EEI. Due to the slower rate of the fall of $E_{LATpeak}$ with increasing V_G as the channel length is reduced, the transition from the first peak to the second peak become less distinguishable. Also the second peak can occur at larger V_G for the shorter devices because EEI is strengthened due to the increasing electron concentration without as significant reduction in $E_{LATpeak}$, unlike in the case of the long channel devices.

The discussion so far suggest that the EEI broadening of the EED tail weakens as the channel length is increased. This point is confirmed in figure 4.22. The figure shows the ratio of M at 77 K to that at 300 K for $L = 0.5$, 1, 2 and 5 μm for $V_{GT} = 0.5V$. We have already seen in the discussions relating to figure 4.19 that such comparisons can be used to identify the bias conditions for which the EED tail is important. In that case we identified significant EEI broadening of the EED for $V_{GT} = 0.5\,V$. Identical V_{GT} means identical channel electron density. If only the channel electron density was the factor determining the strength of EEI interactions, then the ratio of M's should be independent of L. That is not the case is clear from figure 4.22. As V_D is lowered, the ratio of M's decreases significantly for the $5\mu m$ device in comparison to the $0.5\mu m$ device. The variations are also systematic as L is reduced. This signifies the weakening of the EEI as L is increased.

The broadening difference in the lowest V_D at which impact ionization occurs at 300 and 77 K as L was increased, observed in figure 4.2 can also be explained based on the

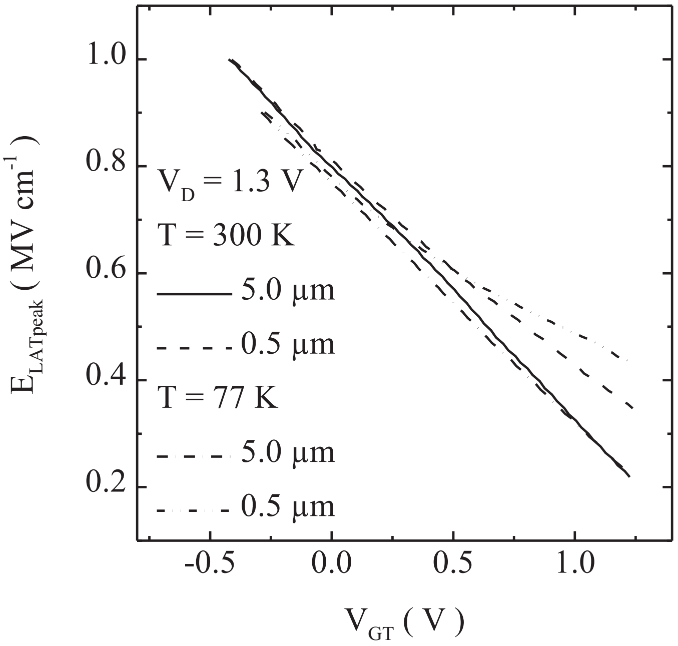


Figure 4.21: Simulated $E_{LATpeak}$ for devices of channel length 0.5 and $5\,\mu m$ at 300 and 77 K.

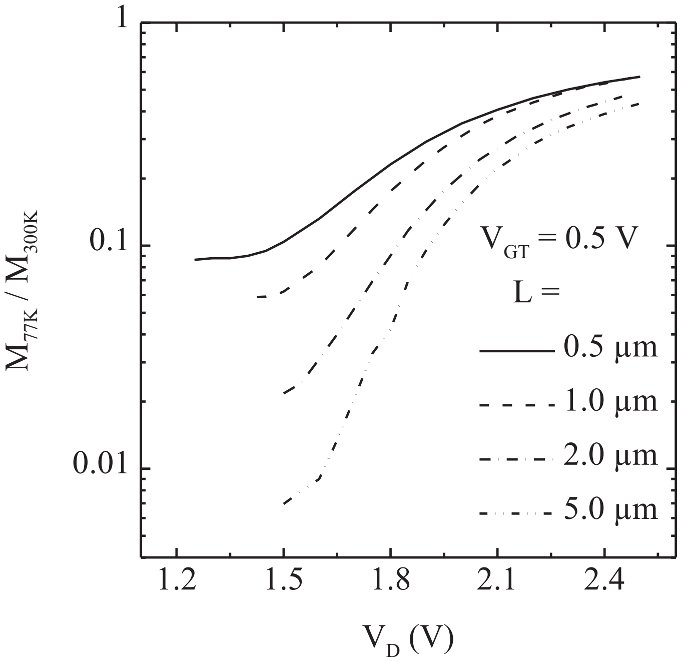


Figure 4.22: Comparison of the ratio of M at 77 K to that at 300 K for $V_{GT} = 0.5\,V$ for $L = 0.5$, 1, 2 and $5\,\mu m$. $V_{GT} = 0.5\,V$ was identified to cause significant EEI broadening of the EED tail for the $0.2\,\mu m$ device in figure 4.19.

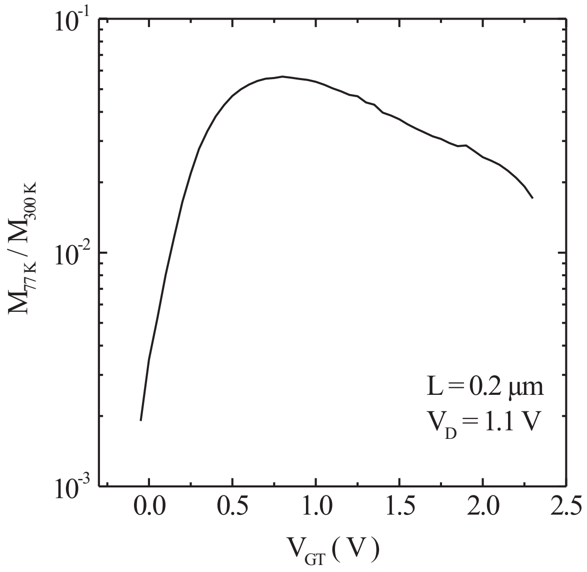


Figure 4.23: Gate voltage dependence of $M_{77\ K}/M_{300\ K}$ when only the tail of EED contribute to impact ionization.

results in the previous paragraph. For example, for $L = 0.16\ \mu m$, the difference between minimum V_D for impact ionization (V_{Dmin}) at 300 and 77 K was 0.15 V whereas for the 5 μm device, it was 0.35 V. If only the increase in the impact ionization threshold as the temperature is lowered was the reason for the difference between the V_{Dmin}, it should have remained independent of L. V_{Gpeak} for the lowest V_D for the 5 μm is also below V_T. 5 μm device also did not show sub bandgap impact ionization at 77 K.

4.2.8 Gate Voltage Dependence of Electron-Electron Interaction Tail

Rauch et al. [59] reported that, for $qV_D < \Delta W_C$ interface degradation increased with increasing V_G. This was explained based on the assumption that EEI increases with increasing V_G. However, we have already seen in figure 4.21 that $E_{LATpeak}$ decreases with increasing V_G. In the previous section we saw that reduction in $E_{LATpeak}$ as L was increased, resulted in weakening of EEI tail. Does the EEI tail weakens due to V_G increase? Also, we have seen that for identical V_{GT}, $E_{LATpeak}$ is higher at 77 K, for large V_{GT} values, figure 4.21. Should we expect a stronger EEI tail at 77 K than at 300 K?

Figure 4.23 shows $M_{77\ K}/M_{300\ K}$ vs V_{GT} for $V_D = 1.1\ V$. For this value of V_D, only the tail of the EED contributes to impact ionization. The population of the tail is highly sensitive to temperature at low V_{GT} due to the fact that it is predominantly a thermal tail. However, as V_{GT} increases, the tail is now determined by EEI and the temperature sensitivity decreases, consequently $M_{77\ K}/M_{300\ K}$ increases. If the population of the tail of EED monotonously increased with V_G, as speculated by Rauch et al. [59], $M_{77\ K}/M_{300\ K}$ should have remained flat for high values of V_{GT}. Contrary to this expectation, $M_{77\ K}/M_{300\ K}$ decreases for $V_{GT} > 0.8\ V$.

Let us assume that EEI induced EED tail weakens as V_{GT} is driven beyond a certain range. However the lower bound of the tail is set by lattice temperature. At 300 K, as V_{GT} is driven too high, the tail reaches the lower bound at lower V_{GT} than it would at 77 K. That means, beyond a certain V_{GT}, even though the tail have reached the lower bound at 300 K, it continue to weaken at 77 K. $M_{77\ K}/M_{300\ K}$ ought to decrease as V_{GT} is driven too high. This proves that the contribution of EEI induced tail can not keep on increasing as V_G is increased.

4.3 Conclusions

In this chapter, we have presented a comprehensive experimental investigation of the impact ionization phenomenon in n-channel MOSFETs for drain voltages near the impact ionization threshold voltage. Novel experimental results obtained by employing highly sensitive direct current measurements, many of which are first time in the literature, were presented.

We have observed an anomalous double-peaked substrate current versus gate voltage characteristics at 77 K. An anomalous increase in the gate voltage at which the substrate current peaks, was also observed at 300 and 77 K. By investigating the channel length dependence we have established that both the observations are linked and are manifestations of the same physical phenomena.

A clear experimental verification was provided for the nature of the tail of the electron energy distribution predicted by Monte-Carlo simulation groups. An anomalous bell shaped quantum yield versus gate voltage characteristics was observed for drain voltage below the bandgap voltage providing clear signatures for the thermal tail and the short range electron-electron interaction broadening of the tail. Nonlinear nature of the logarithm of the quantum yield versus gate voltage characteristics would mean that presently used exponential reliability prediction techniques would collapse at such low drain voltages.

A method is evolved to compare the relative strength of the thermal tail and the EEI tail by using the ratio of quantum yield at 77 K to that at 300 K. We have deduced that the tail beyond qV_D will play an important role in deciding the substrate current for V_D below 1.6 V for our 0.2 μm device.

We have also proposed a role for the inversion layer quantization in the electron energy distribution. The distribution may shift to higher energies due to the difference between the lowest energy level above the conduction band edge and the additional band bending required for identical inversion charge.

Two peaks in the substrate current vs gate voltage characteristics was shown to be due to the presence of various energy gain mechanisms which have differing gate voltage dependence. The abnormal V_{Gpeak} reversal was correlated to the presence of electron-electron interaction induced tail.

An interpretation of the channel length dependence of the substrate current versus gate voltage characteristics was provided by analyzing the peak lateral electric field obtained using 2-dimensional drift-diffusion simulations. For identical positive gate overdrive, the longer device has a lower peak lateral field and consequently a more dominant role for the tail. It was established that the EEI broadening of the tail weakens as the channel length is increased and this was related to the reduction in peak lateral field.

It was found that EEI contribution to impact ionization reduces as the gate voltage is driven too high. This is due to the reduction of the peak lateral field as the gate voltage is increased.

These results reaffirm the importance of the peak lateral field as the deciding factor as far as the low voltage reliability issues are concerned. We expect that structures that reduce the peak lateral field will have improved low voltage reliability.

The valuable experimental information on the nature of the tail of the electron energy distribution presented here may be of significant importance to understand the physics of soft programming reliability of flash memory cells and hot-carrier reliability of future MOSFETs with high relative permittivity dielectrics. The hot-carrier reliability is not a major concern in modern logic and DRAM devices with SiO_2 as the gate dielectric due to the scaling of operating voltages much below the $Si - SiO_2$ barrier. Reduced silicon to dielectric barrier in the case of high relative permittivity dielectrics would mean higher electron injection into the gate dielectric than into SiO_2 even at very low voltages. This may be an important reliability issue for such devices.

Chapter 5

Impact Ionization in Laterally Asymmetrical n-channel MOSFETs

As the channel length (L) of n-channel MOSFETs is scaled down to deep submicron dimensions, significant non stationary transport can be present in the devices. The device performance can be improved by designing structures that facilitate non stationary transport. The impact of velocity overshoot on device performance can be improved if the electrons see an accelerating field right at the source end of the channel [97, 98].

An accelerating field at the source can be achieved by a graded doping profile along the channel direction with the peak at the source junction. Such structures were designed and fabricated both in lateral and vertical transistors [49, 99, 100, 101]. The lateral devices are called "Laterally Asymmetrical Channel (LAC)" MOSFETs. Such devices are reported to have superior current drives [49, 81, 102] and hot-carrier reliability [81, 103] in comparison to CONventional (CON) devices.

In this chapter, impact ionization in LAC MOSFETs fabricated by Cheng [81] at the University of California Los Angeles, is experimentally investigated. Investigations were carried out by measuring the substrate current (I_{SUB}) at 300 and 77 K in devices of $L = 0.2$ to $5\,\mu m$. Measurements were done in both forward and reverse modes of operation of the devices. I_{SUB} vs gate voltage (V_G) characteristics with three distinct peaks were measured for the forward mode of operation. The peaks show differing L and temperature dependencies. Only one peak was found in I_{SUB} vs V_G data for the reverse mode of operation. Two dimensional drift-diffusion simulations were carried out to find possible explanations for the abnormal I_{SUB} characteristics. It was found that the lateral electric field (E_{LAT}) distribution has two peaks, one at the source end of the channel and the other at the drain end of the channel, for the forward mode of operation. The first and the third peaks in I_{SUB} are related to the peaks in E_{LAT}. For the reverse mode of operation, simulation results show only one peak in E_{LAT}. The results are analyzed and suggest that the second peak is due to electron-electron interactions (EEI). The roles of short and long range interactions are pointed out. For the forward mode of operation, the source electrons are directly injected into a high field region. For this reason, quantitative treatment of the data presented using Monte-Carlo tools incorporating appropriate models may provide insight into the nature of EED in the source. It is reported that long-range interactions may significantly modify

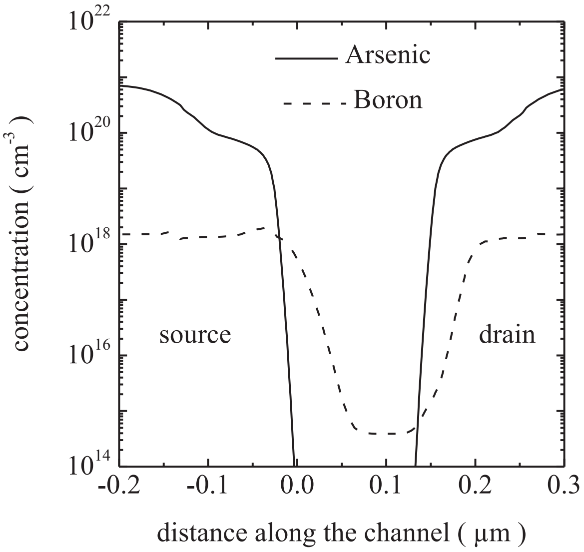


Figure 5.1: Simulated doping profile of a LAC device of drawn channel length $0.2\,\mu m$. The profile shown is for a depth of 1 nm from the interface. Tilted implant does not result in over-compensation of source extension. Source-drain configuration shown is for the forward mode of operation. Reverse mode of operation is obtained by exchanging the role of these regions.

the EED in the source [74].

This chapter is organized as follows. Device fabrication and structure are presented in section 5.1. Transfer and output characteristics of the devices are presented in section 5.2. Sections 5.3 to 5.5 detail the experimental I_{SUB} data for the devices in both forward and reverse modes of operation. These results are compared with that of conventional devices in section 5.6. In section 5.7, experimental results are analyzed based on 2-D simulation results. Conclusions are presented in section 5.8.

5.1 Device Structure

LAC process flow is slightly different from that of CONventional (CON) n-channel MOSFETs discussed in chapters 3 and 4. Process flows for the LAC and CON are given in Appendix A. Critical process steps are illustrated and compared. The important difference is that, for LAC devices threshold adjust implant is done after gate structuring, whereas in CON devices it is done before forming the gate oxide. In CON devices, the implant is done at zero tilt angle to get minimum gate-source and gate-drain overlap and the wafer is rotated 360^o to avoid shadowing effects [104]. In LAC devices, the threshold implant is done only from one side, which eventually becomes the source in the forward mode, and it is tilted, the tilt angle being a device design parameter. LAC devices can be thought of as a single source halo structure. For the devices used in this study, gate oxide has a nominal thickness of 3.6 nm and the threshold implant had a tilt angle of 10^o. No anti-punch-through implants were done so that a sharp LAC profile is obtained.

Simulated doping profiles along the channel direction and 1 nm from the $Si-SiO_2$ interface for LAC device of channel length $0.2\,\mu m$ are shown in figure 5.1. Boron concentration has a peak of approximately $10^{18}cm^{-3}$ at the source junction and it falls to the nominal substrate doping level, which is about $10^{15}cm^{-3}$ in the present case, in about 80 nm. The source and drain as per the device design are marked. When the device is operated with source and drain taken as shown, the operation mode is called forward mode and when the source and drain are exchanged it is called reverse mode. The tilted angle implant does not over-compensate the source extension doping. This ensures sufficient gate-source overlap for proper operation of the devices.

5.2 Terminal Characteristics

Since LAC devices are inherently asymmetric, measurements were performed in both modes described in the previous section.

Measured drain current (I_D) vs V_G at 300 and 77 K for devices of $L = 0.2$ and $2\,\mu m$ for the forward mode of operation are shown in figures 5.2a and 5.3a respectively. $2\,\mu m$ devices show excellent characteristics. $0.2\,\mu m$ devices show Drain Induced Barrier Lowering (DIBL) and punch-through effects for prematurely high drain voltages (V_D). This is because, anti-punch-through implant was avoided in the present device structures. Figures 5.2b and 5.3b show I_D vs V_D characteristics for the same devices.

Measured I_D vs V_D characteristics of $0.5\,\mu m$ devices operated in the reverse mode are compared with those operated in the forward mode in figure 5.4. The characteristics in the reverse mode does not show good saturation. This is because, in the reverse mode of operation the highest barrier for electron flow is at the drain junction which is directly controlled by V_D. However, when V_D is small, the current drive is higher for the forward mode of operation. For example, for $V_{GT} = 2.5\,V$ at 300 K, the drive is higher for the forward mode. At 77 K, partial freeze-out enhances the non saturating behavior. For the reverse mode of operation, investigations were conducted on devices with $L = 0.5\,\mu m$ and above, due to the poor characteristics.

5.3 I_{SUB} vs V_G in the Forward Mode

I_{SUB} vs V_G characteristics were measured for both forward and reverse modes of operation. In this section, the results of investigations in the forward mode are presented.

I_{SUB} was measured at 300 and 77 K for devices with $L = 0.2$ to $5\,\mu m$ for V_D upto 3 V. V_G was swept from well below threshold voltage (V_T) upto 3 V. The voltages are restricted to 3 V so that the measurements do not cause any degradation in the device characteristics. I_{SUB} vs V_G data obtained for $L = 5$, 2, 1, 0.5, 0.35 and $0.2\,\mu m$ are shown in figures 5.5, 5.6, 5.8, 5.9 5.10 and 5.11 respectively. In all the figures, **'(a)'** part shows the data at 300 K and **'(b)'** part shows the data at 77 K. V_T measured for $V_D = 0.05\,V$ is subtracted from V_G. The horizontal and vertical axes scales are identical in all the figures. V_D for which the data are shown are given in the figure captions. All the devices except the one with $L = 0.35\,\mu m$, had channel width of $20\,\mu m$. The $0.35\,\mu m$ devices had a width of $10\,\mu m$. All the data discussed are reproducible.

Figure 5.5a shows I_{SUB} vs V_G data for $5\,\mu m$ device at 300 K. Bell shaped curves with single peak are observed. Figure 5.5b shows the data at 77 K. A second peak is

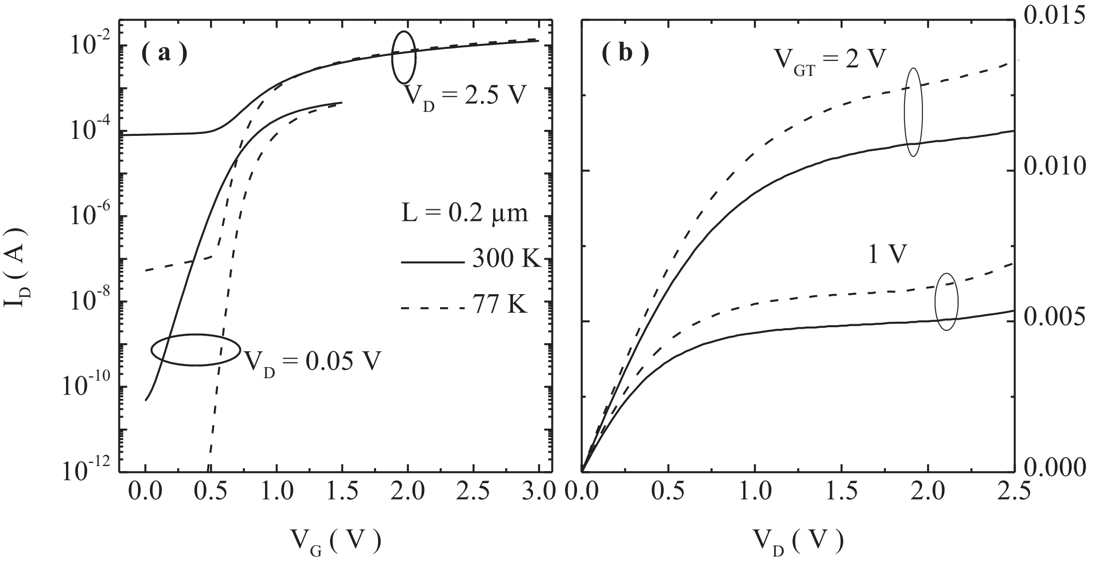


Figure 5.2: Measured terminal characteristics of devices of $0.2\,\mu m$ channel length at 300 and 77 K for forward mode of operation. The devices had a width of $10\,\mu m$. (a) shows the transfer characteristics and (b) shows the output characteristics.

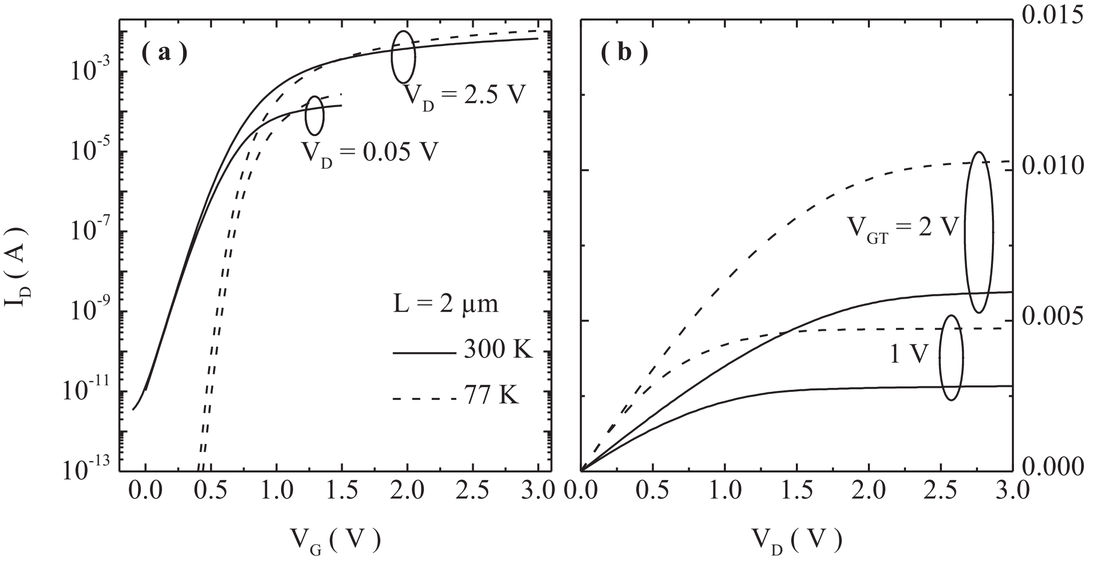


Figure 5.3: Measured terminal characteristics of devices of $2\,\mu m$ channel length at 300 and 77 K for forward mode of operation. The devices had a width of $10\,\mu m$. (a) shows the transfer characteristics and (b) shows the output characteristics.

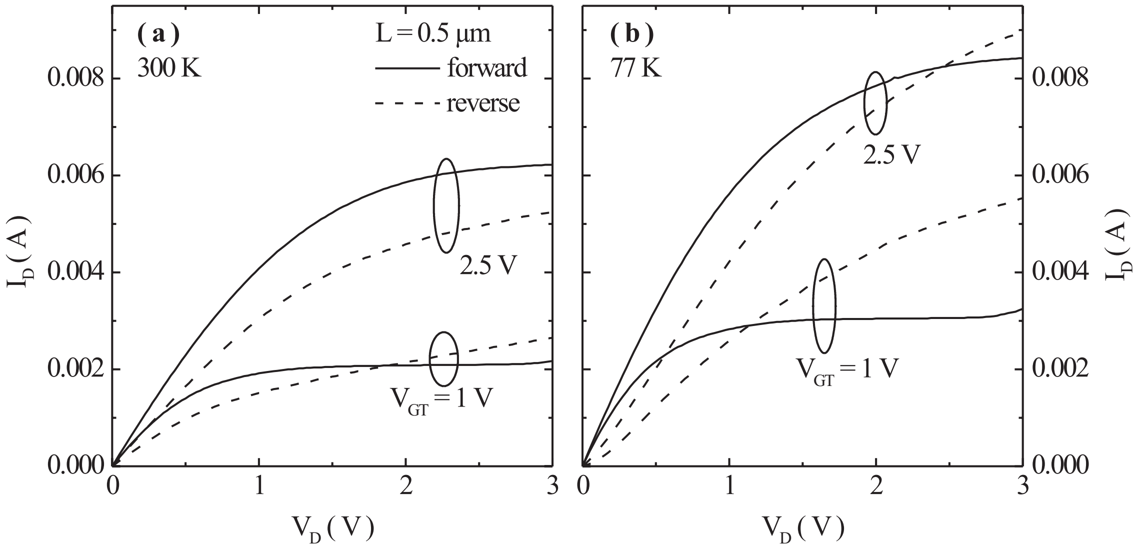


Figure 5.4: Output characteristics of LAC devices of channel length $0.5\,\mu m$ measured in forward and reverse modes of operation at (a) 300 K (b) 77 K. The devices had width of $10\,\mu m$.

observed in this case. For identical V_D, both the I_{SUB} peaks at 77 K are smaller than the only peak observed at 300 K. The second peak is less distinguishable as the V_D is raised and completely vanishes for very high values.

In the following discussion I_{SUB} values at the peaks are denoted by $I_{SUBpeak}$ and the corresponding V_G values by V_{Gpeak}.

Figure 5.6a shows I_{SUB} vs V_G data for a $2\,\mu m$ device at 300 K. Bell shaped curves with a single peak are observed. Figure 5.6b shows the data at 77 K. In addition to the second peak, a third peak is also observed in this case. For 1.3 V, the lowest V_D for which the characteristics are shown, only a single bell is observed. $V_{Gpeak} - V_T$ corresponding to this is 0.83 V. The first and second peaks make an appearance for $V_D \geq 2\,V$. $V_{Gpeak} - V_T$ corresponding to the first peak is -0.146 V. As V_D is increased, $I_{SUBpeak}$ for the first peak increases more rapidly than for the third peak. The third peak is much stronger than the second one. Whereas the first peak is suppressed as the temperature is reduced, the second and third peaks appear only at 77 K.

We digress to clearly identify and name the three peaks. Figure 5.7 shows I_D vs V_G plots for a $2\,\mu m$ device at 77 K for $V_D = 2.05, 2.1$ and $2.15\,V$. Three peaks can be clearly identified. All the peaks increase with increasing V_D and the curves do not cross-over for any V_D. The peaks are named as they appear as V_G is increased. In cases where all the three peaks are not visible, those visible are identified according to the corresponding $V_{Gpeak} - V_T$ values. For example, in figures 5.5a and 5.6a only one peak is visible for all the V_D values. The corresponding $V_{Gpeak} - V_T$ values fall in the range of $V_{Gpeak} - V_T$ for the first peak at 77 K (refer figures 5.5b and 5.6b) and hence are identified as the first peaks. V_{Gpeak} trends are analyzed later and justify such a scheme.

Figure 5.8 shows I_{SUB} vs V_G data for a $1\,\mu m$ device at 300 and 77 K. At 300 K, apart from the easily identifiable first peak, a measurable current is flowing for gate overdrive (V_{GT}) $> 1\,V$. It is emphasized that this is not due to gate oxide leakage

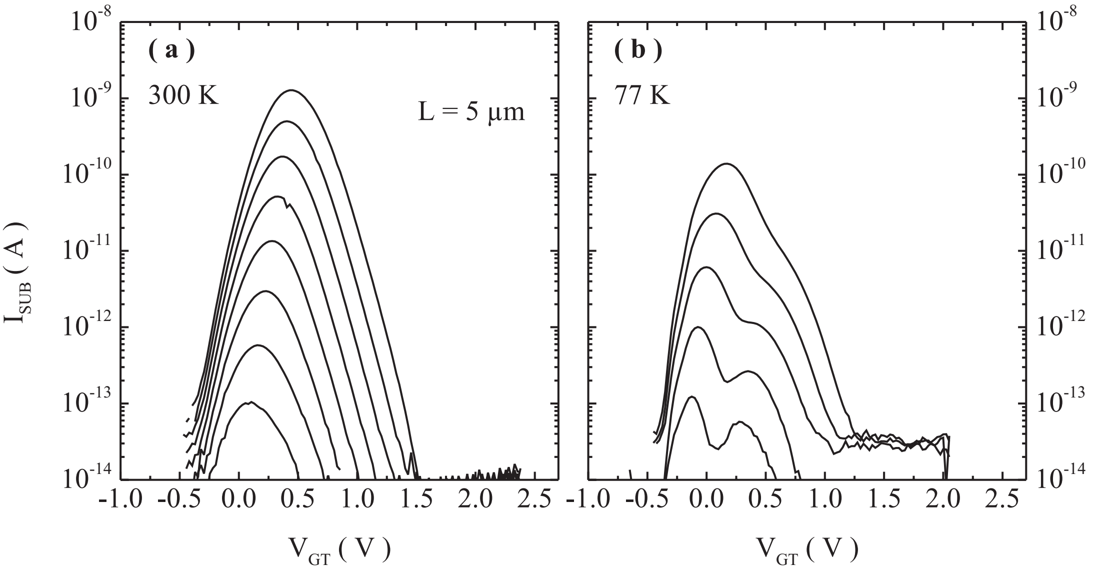


Figure 5.5: I_{SUB} vs V_G characteristics of a LAC device of $L = 5\,\mu m$, (a) at 300 K for $V_D = 1.8$ to $2.5\,V$ with $\Delta V_D = 0.1\,V$, and (b) at 77 K for $V_D = 2.1$ to $2.5\,V$ with $\Delta V_D = 0.1\,V$.

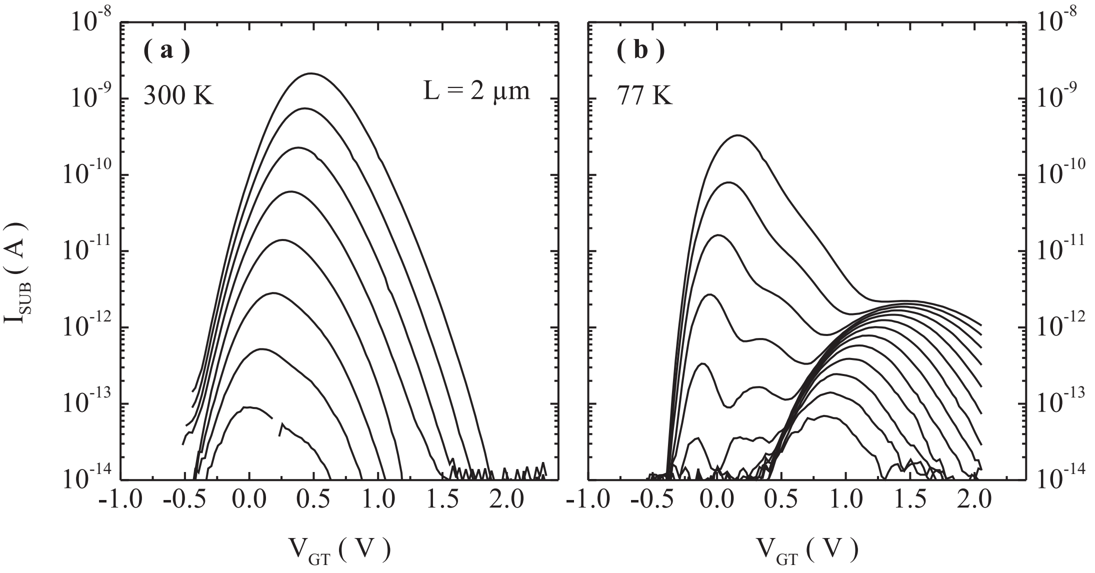


Figure 5.6: I_{SUB} vs V_G characteristics of a LAC device of $L = 2\,\mu m$, (a) at 300 K for $V_D = 1.8$ to $2.5\,V$ with $\Delta V_D = 0.1\,V$, and (b) at 77 K for $V_D = 1.3$ to $2.5\,V$ with $\Delta V_D = 0.1\,V$.

or drain junction leakage. Gate leakage would have been more visible in the case of the longer channel devices due to larger gate area (all the devices considered till now had a width of 20 μm). Drain junction leakage should be visible for $V_G \ll V_T$ as well. A feeble bell shape is visible for large V_{GT}. For 1.8 V, the lowest V_D shown, the top of the bell is more flatter than was observed for the longer devices. This point will be elaborated upon later. Figure 5.8b shows the data at 77 K. The second and third peaks are observed. For 1.1 V, the lowest V_D for which the characteristics are shown, only a single bell is observed. $V_{Gpeak} - V_T$ corresponding to this is 0.745 V. The first and second peaks make an appearance for $V_D \geq 1.9\,V$.

Figure 5.9 shows I_{SUB} vs V_G data for a 0.5 μm device at 300 and 77 K. Two peaks are observed at 300 K. Only the third peak is observable for $V_D < 1.6\,V$. At 77 K, all the three peaks are observed. Only the third peak is observed for $V_D < 1.9\,V$. The first and third peaks have opposite temperature dependencies. Whereas the first peak is suppressed as the temperature is reduced, the third peak is enhanced.

Figure 5.10 shows I_{SUB} vs V_G data for a 0.35 μm device at 300 and 77 K. Only two peaks are observed both at 300 and 77 K. No distinguishable second peak is observed at 77 K. Only the third peak is observed for $V_D < 1.6\,V$ both at 300 and 77 K. For $V_D \geq 1.6\,V$ at 300 K, the first peak is clearly distinguishable, whereas at 77 K, a bump is observed on the rising part of the curve. The bump evolves to a distinguishable peak for $V_D \geq 1.8\,V$.

Figure 5.11 shows I_{SUB} vs V_G data for a 0.2 μm device at 300 and 77 K. At both temperatures, only two peaks are observed. Only the third peak is observed for $V_D < 1\,V$ and $V_D < 1.1\,V$ at 300 and 77 K respectively. For $V_D \geq 1\,V$ and $V_D \geq 1.1\,V$ at 300 and 77 K respectively, a bump is observed in the I_{SUB} vs V_G at low V_G which gradually grows to a peak as the V_D is increased. No distinguishable second peak is observed in the plots.

I_{SUB} vs V_G data presented so far has painted a fairly complex picture, with new features appearing for each L. However, the changes are gradual and systematic as L is varied. In the following, data extracted from I_{SUB} vs V_G plots seen in this section are presented to reassert that the features evolve systematically with L.

Figure 5.12 shows I_{SUB} vs V_G data for $V_D = 1.8\,V$ at 300 K and for $V_D = 2\,V$ at 77 K for a device of $L = 1\,\mu m$. The data is a selection from figure 5.8. The minimum V_D for noise free data was the criterion of selection at 300 K. V_D at 77 K was chosen so that the peaks have I_{SUB} comparable to those at 300 K. We have shown only that part of the data which shows the first two peaks. The curve at 300 K looks more like a trapezoid than a bell for $-0.4\,V < V_{GT} < 0.75\,V$. If we refer back to figure 5.8a, it is seen that the trapezoid evolves to a bell as the V_D is increased. A replica of this case is also seen for the 2 μm device, figure 5.8a, but less distinct than for the 1 μm device. In figure 5.12, the data at 77 K show two peaks for comparable range of V_{GT} given before. As V_D is increased, the second peak diminishes in comparison to the first peak and eventually disappears for very large V_D values, figure 5.8b.

These observations suggest that the two distinguishable first and second bells observed at 77 K smoothly merge into a shape with a single peak at 300 K. More supportive evidence to this will be presented in the following sections.

Since only a maximum of two peaks are observed at 300 K, and since it seems that the first and second peaks observed at 77 K merge at 300 K, in the analysis that follows, we consider the first and second peaks together and the third peak separately.

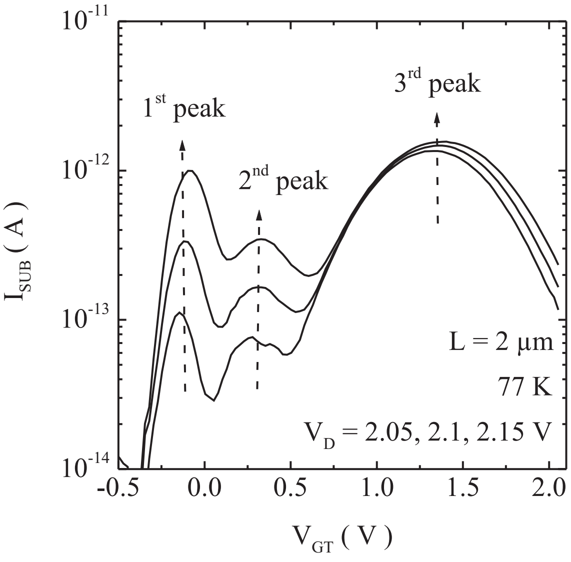


Figure 5.7: I_{SUB} vs V_G for device with $L = 2\,\mu m$ at 77 K. Three peaks are identified and named. All the peaks increase with increasing V_D.

Figure 5.13 shows L dependence of the minimum V_D (V_{Dmin}) at which the third peak and the first and second peaks combined are observed. For $L \leq 0.35\,\mu m$, only a bump is visible on the rising part of the I_{SUB} vs V_G plots at the lowest V_D. For this reason no V_{Dmin} were evaluated for the first and second peaks for this range of L. The bandgap voltages at 300 and 77 K are also shown in the figure. As we have already seen, at 300 K, the third peak was clearly observed for $L \leq 1\,\mu m$ whereas at 77 K, it was observed for $L \leq 2\,\mu m$. The third peak was observed for sub bandgap V_D for $L \leq 1\,\mu m$ at 300 and 77 K. V_{Dmin} for the third peak for the $2\,\mu m$ device at 77 K is slightly above the bandgap voltage. For $L \geq 0.35\,\mu m$, $V_{Dmin}(77K) < V_{Dmin}(300K)$. This trend is reversed for the smaller devices. On the other hand, for the first and second peaks combined, V_{Dmin} is greater than the bandgap voltage both at 300 and 77 K. In contrast to the trend for the third peak, $V_{Dmin}(77K) > V_{Dmin}(300K)$ in this case.

5.3.1 V_{Gpeak} vs V_D Plots

In the case of CON devices, V_{Gpeak} vs V_D plots had provided useful insights into the physical mechanisms. In this section, a similar analysis is made for the LAC devices. The first and second peaks are considered together. This is because the second peak is observed only at 77 K for $L = 0.5, 1,$ 2 and 5 μm and for a very limited range of V_D. In cases where the second peak is clearly visible, that peak which has the higher I_{SUB} was selected. Such a selection also makes comparisons with the CON devices easier.

Figures 5.14, 5.15 and 5.16 show V_{Gpeak} vs V_D data for devices of $L = 5$, 1, 0.5, 0.35, 0.25 and 0.2 μm at 300 and 77 K. V_{Gpeak} corresponding to the third peak and the first and second peak combined are shown. V_T measured for $V_D = 0.05\,V$ was subtracted from V_{Gpeak}. $V_{Gpeak} = V_T$ line is shown in all the plots for guidance.

For the $5\,\mu m$ device, figure 5.14a, $V_{Gpeak} - V_T$ varies nearly linear with V_D at both

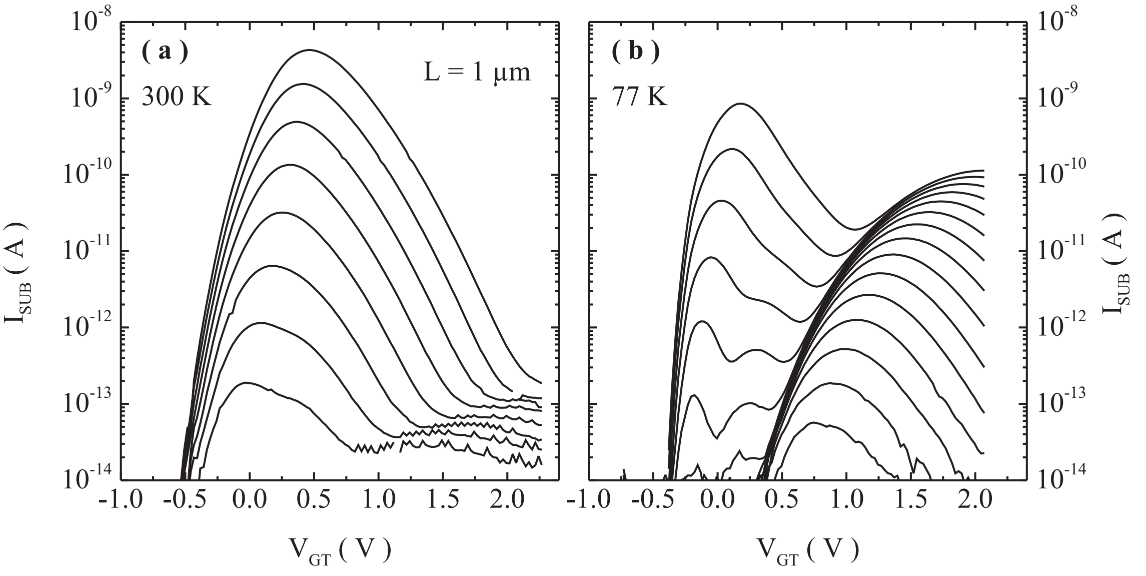


Figure 5.8: I_{SUB} vs V_G characteristics of a LAC device with $L = 1\,\mu m$, (a) at 300 K for $V_D = 1.8$ to $2.5\,V$ with $\Delta V_D = 0.1\,V$, and (b) at 77 K for $V_D = 1.1$ to $2.5\,V$ with $\Delta V_D = 0.1\,V$.

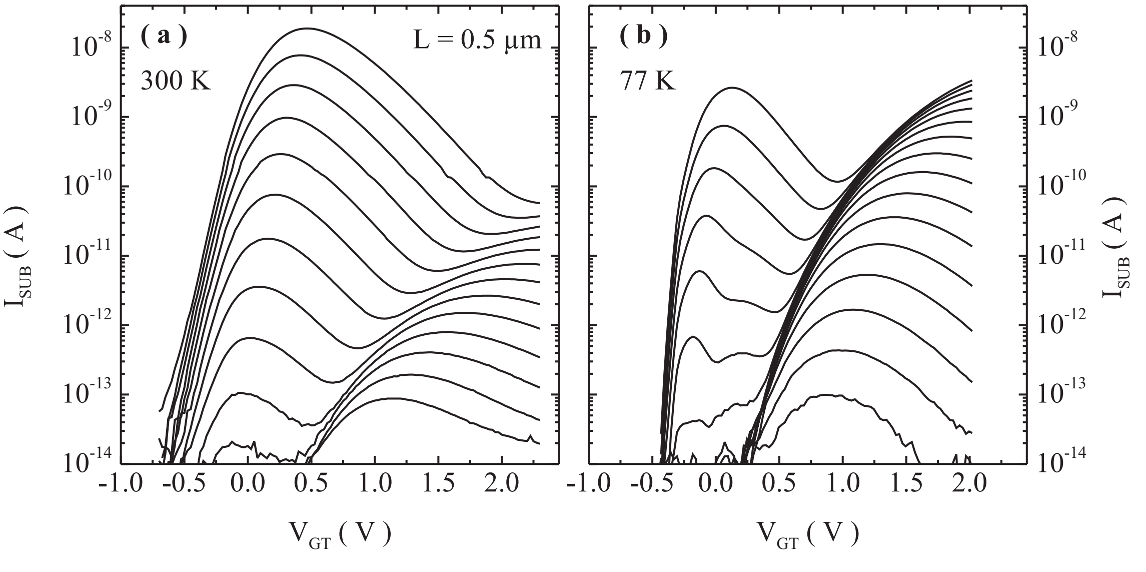


Figure 5.9: I_{SUB} vs V_G characteristics of a LAC device of $L = 0.5\,\mu m$, (a) at 300 K for $V_D = 1.3$ to $2.5\,V$ with $\Delta V_D = 0.1\,V$. Multiple peaks for $V_D \geq 1.5\,V$; (b) at 77 K for $V_D = 1$ to $2.5\,V$ with $\Delta V_D = 0.1\,V$.

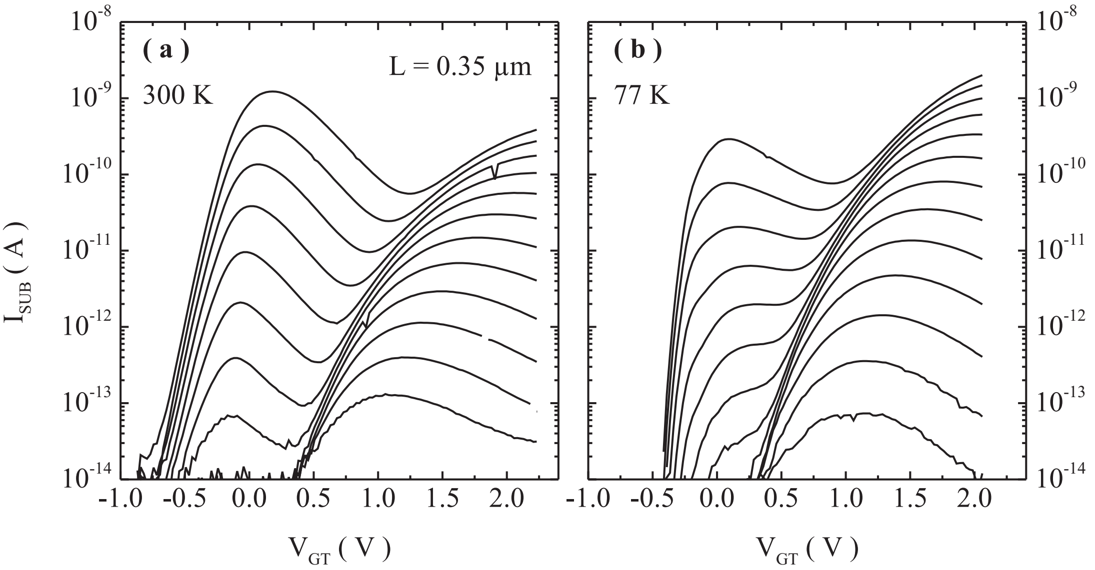


Figure 5.10: I_{SUB} vs V_G characteristics of a LAC device of $L = 0.35\,\mu m$, (a) at 300 K for $V_D = 1.1$ to $2.2\,V$ with $\Delta V_D = 0.1\,V$, and (b) at 77 K for $V_D = 1$ to $2.2\,V$ with $\Delta V_D = 0.1\,V$.

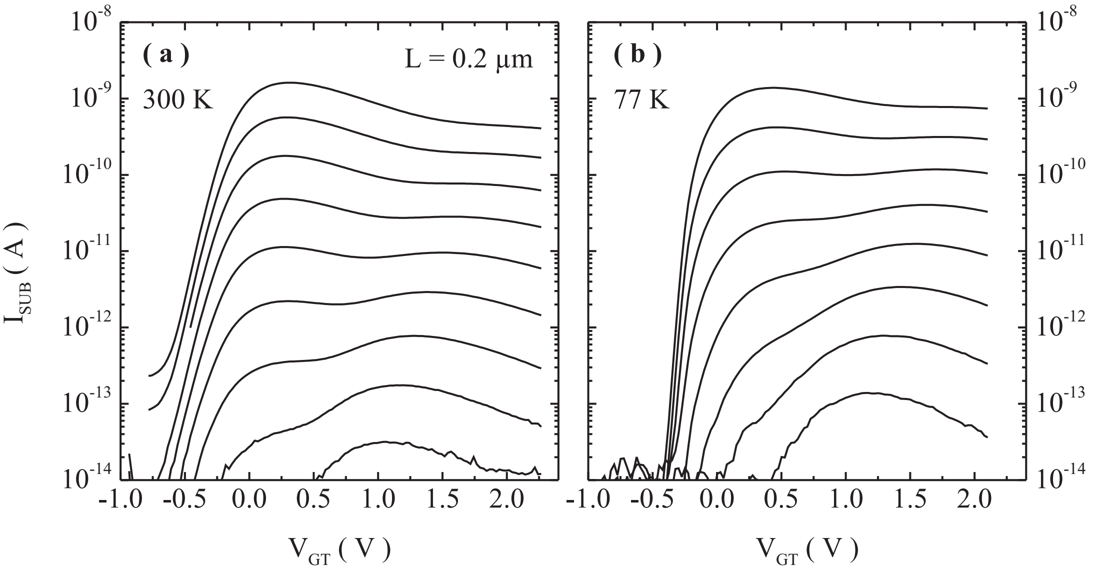


Figure 5.11: I_{SUB} vs V_G characteristics of a LAC device with $L = 0.2\,\mu m$, (a) at 300 K for $V_D = 0.9$ to $1.6\,V$ with $\Delta V_D = 0.1\,V$, and (b) at 77 K for $V_D = 1$ to $1.6\,V$ with $\Delta V_D = 0.1\,V$.

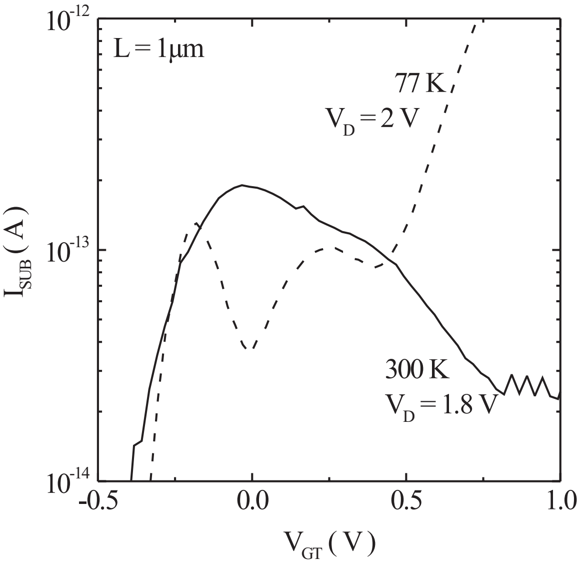


Figure 5.12: Comparison of the I_{SUB} vs V_G for a $1\ \mu m$ device at 300 and 77 K. V_D was chosen so that the first bells have comparable currents. A careful comparison suggests that the bell corresponding to the first peak at 300 K is a merger of two bells.

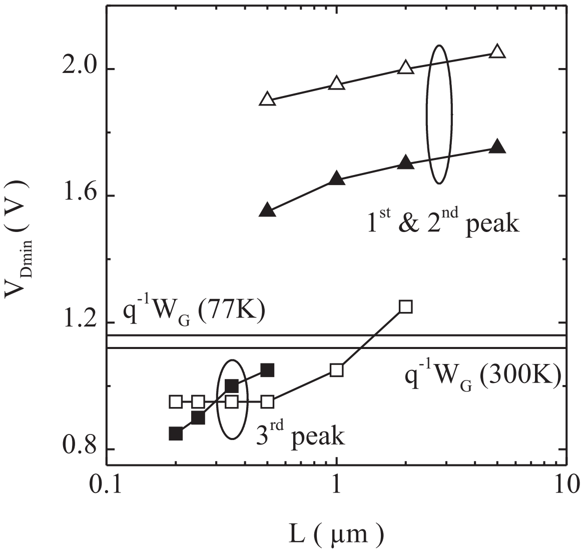


Figure 5.13: The minimum V_D for which the third peak and the first and second peaks are observed as a function of L at 300 and 77 K. The filled symbols are data at 300 K and the open symbols at 77 K. The bandgap voltages at 300 and 77 K are also shown.

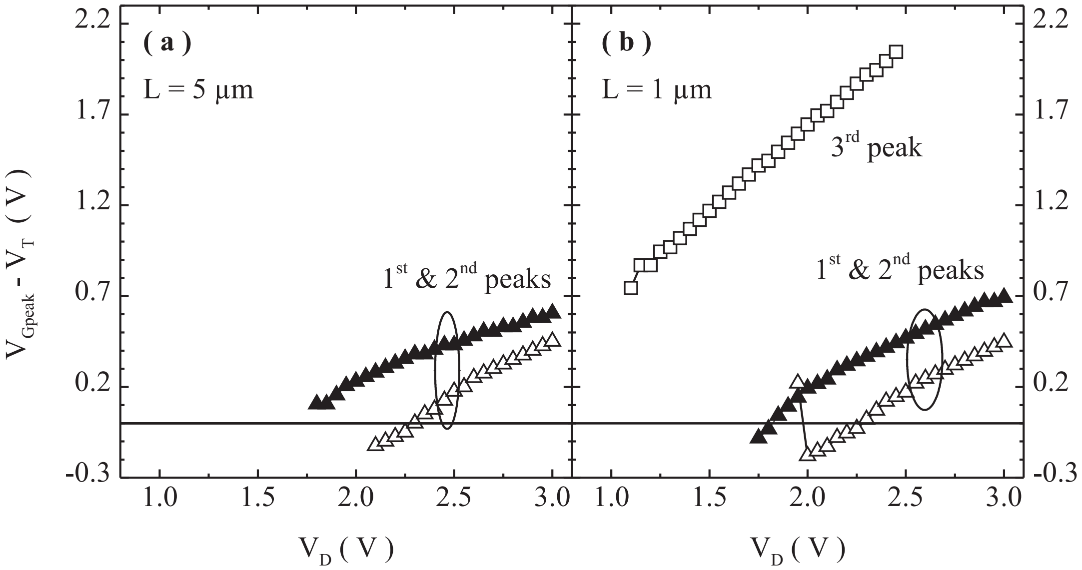


Figure 5.14: V_{Gpeak} vs V_D for devices of L equal to (a) $5\,\mu m$ and (b) $1\,\mu m$. Filled symbols are for data at 300 K and open symbols for that at 77 K.

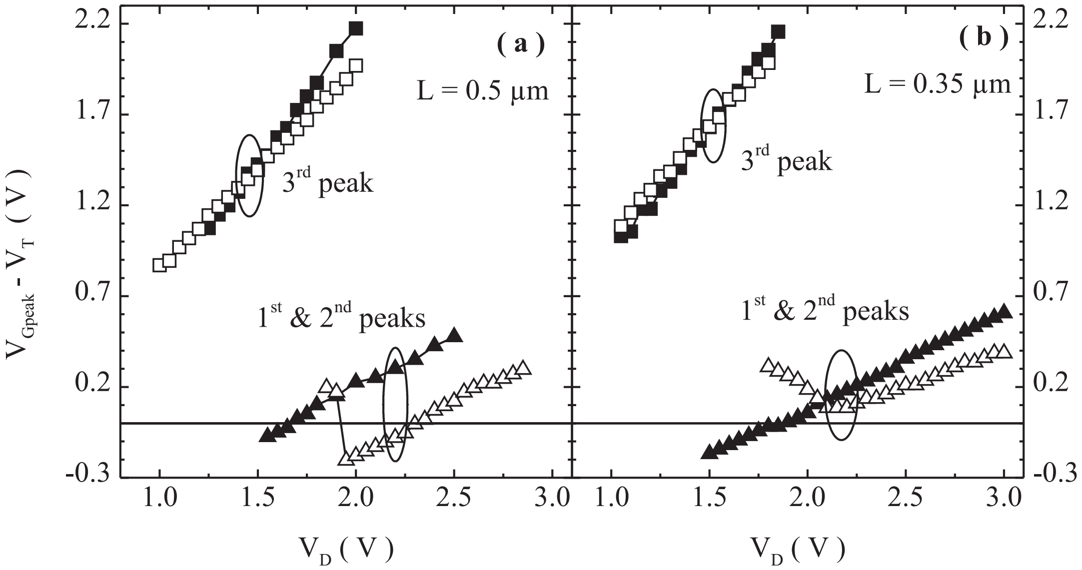


Figure 5.15: V_{Gpeak} vs V_D for devices of L equal to (a) $0.5\,\mu m$ and (b) $0.35\,\mu m$. Filled symbols are for data at 300 K and open symbols for that at 77 K.

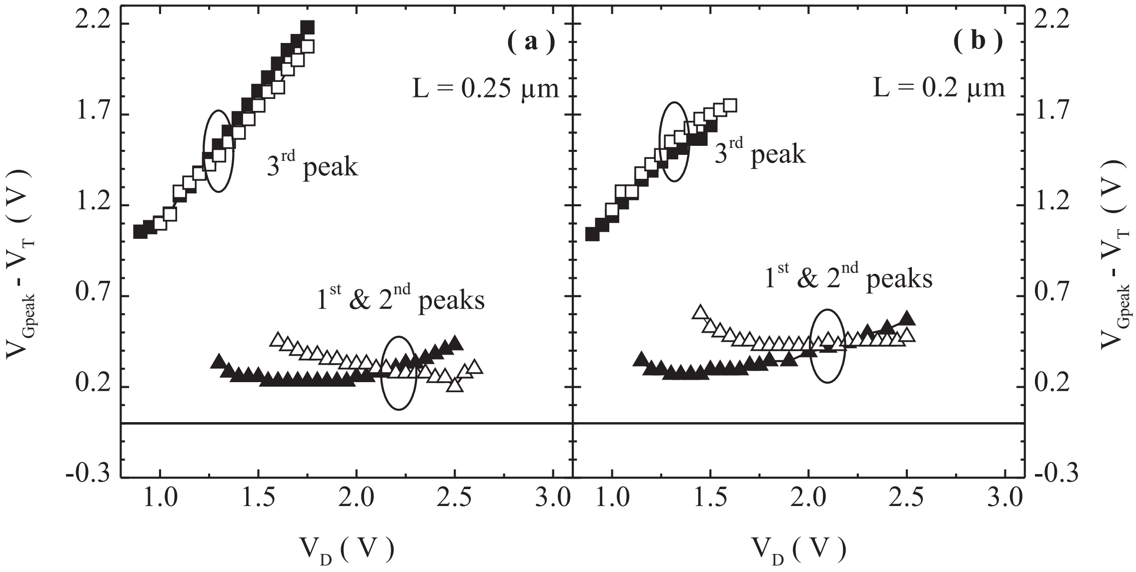


Figure 5.16: V_{Gpeak} vs V_D for devices of L (a) $0.25\,\mu m$ and (b) $0.2\,\mu m$. Filled symbols are for data at 300 K and open symbols for that at 77 K.

300 and 77 K. Of the first and second peaks, the first peak dominates for all V_D values. $V_{Gpeak} - V_T$ values at 77 K are consistently smaller than that at 300 K. For $V_D < 2.35\,V$, V_{Gpeak} is less than V_T at 77 K.

For the 1 μm device, figure 5.14b, the third peak is visible at 77 K. Corresponding V_{Gpeak} shows a linear dependence on V_D. V_{Gpeak} corresponding to the first and second peaks also show a nearly linear dependence on V_D at 300 K. For $V_D < 1.85\,V$, V_{Gpeak} is less than V_T. At 77 K, the V_{Gpeak} corresponding to the first and second peaks show linear dependence on V_D except for the lowest V_D (= 1.95 V) in which case a reversal in the trend is observed. This is due to the dominance of the second peak over the first one for this particular V_D. For $1.95\,V < V_D < 2.35\,V$, $V_{Gpeak} < V_T$.

For the 0.5 μm device, figure 5.15a, the third peak is visible both at 300 and 77 K. Corresponding $V_{Gpeak} - V_T$ data show linear dependence on V_D and does not show any significant temperature dependence. V_{Gpeak} data corresponding to the first and second peaks show different trends. The data at 300 K again show a linear behavior and for $V_D < 1.7\,V$, $V_{Gpeak} < V_T$. The data at 77 K show similar trends as for the 1 μm device. For $V_D < 1.95\,V$, the second peak dominate over the first one.

Figure 5.15b shows the data for $0.35\,\mu m$ devices. $V_{Gpeak} - V_T$ corresponding to the third peak varies linearly with V_D at both the temperatures and does not show any markable temperature dependence. For the first and second peaks combined, $V_{Gpeak} - V_T$ vs V_D is linear at 300 K. At 77 K, V_{Gpeak} decreases for V_D down to 2.2 V. It again increases as the V_D is reduced below 2.05 V. Unlike in the case of the 1 and $0.5\,\mu m$ devices, the reversal is gradual and smooth. We would like to note that I_{SUB} vs V_G plots for the $0.35\,\mu m$ devices, figure 5.10, did not show any clear second peak.

The evolution of the behavior of V_{Gpeak}, corresponding to the first and second peaks combined, at 77 K with L suggest that the two peaks merge to a single peak smoothly as L is reduced. The reversal in the V_{Gpeak} is due to the dominance of the second peak.

Figure 5.16a shows the data for 0.25 devices. The third peak retains the same trend as the longer devices and shows no distinguishable temperature dependence. On the other hand, the first and second peaks combined show V_{Gpeak} reversal even at 300 K. The reversal is gradual and smooth. At 77 K, $V_{Gpeak} - V_T$ values are higher than the corresponding data at 300 K, for V_D below the reversal point.

Figure 5.16b shows the data for 0.2 μm devices. The trends are similar to that of the 0.25 μm devices.

The data for the 0.25 and 0.2 μm devices attest to the presence and dominance of the second peak for low V_D even at 300 K. The second peak is enhanced at 77 K.

5.3.2 I_{SUB}/I_D vs V_D Plots

Analysis of quantum yield ($M = I_{SUB}/I_D$) provides important information regarding the energy gain and redistribution mechanisms and their relative strength. In chapter 4, it was shown that the comparison of M in subthreshold and above threshold regimes can be used to assess the relative strengths of the thermal and EEI broadened tails.

For the CON devices we analyzed M for a given V_{GT} and also using V_{GT} as a parameter. V_{GT} condition, to the first approximation, corresponds to equal inversion layer charge density. In the case of LAC devices, a fixed V_{GT} is a difficult condition to use for all values of L. The highest V_G was limited by the requirement that the devices are not degraded during the measurements. The difficulty associated with the choice of V_{GT} can be appreciated by referring to I_{SUB} vs V_G data for the 0.5 μm devices, 5.9a. The third peak is observed for $V_{GT} > 0.5\,V$. We can not use any choice of $V_{GT} > 0.5V$, as a representative of the third bell for the whole range of V_D because beyond certain V_D, the first and second bells combined dominate over the third for this range of V_{GT}. The problem is particularly severe in shorter devices. The best choice in these premises is the bias point corresponding to $I_{SUBpeak}$ which is well defined and is associated with a known peak.

Figure 5.17 shows M corresponding to the third peak and, the first and second peaks combined at 300 and 77 K for devices of $L = 5$ and 1 μm. M corresponding to the first and second peaks combined is consistently lower at 77 K than at 300 K. No cross-over is observed in this case for V_D upto 3 V. In the case of the 1 μm device at 77 K and the lowest V_D, M falls abruptly. For this V_D, the second peak dominates over the first one. Even though the second peak is marginally higher than the first one, the corresponding I_D is much higher for V_G corresponding to the second one and hence the abrupt fall. Except for this point, M is higher for the 1 μm device than for the 5 μm device at both the temperatures. For the 1 μm device, the third peak is visible at 77 K and the corresponding M values are lower than that for the first and second peaks combined.

Figure 5.18 shows the data for the 0.5 and 0.35 μm devices. For both L, the third peak was observed at 300 and 77 K. For the first and second peaks combined, M at 77 K is consistently lower than at 300 K. The effect of the increasing dominance of the second peak over the first is also evident at 77 K. No crossover is observed. For the third peak, M at 77 K is higher than at 300 K. The difference comes down as L is reduced. Even though no crossover is observed, the data extrapolated to lower V_D than shown, tend to cross-over. These extrapolated crossover voltages tend to decrease

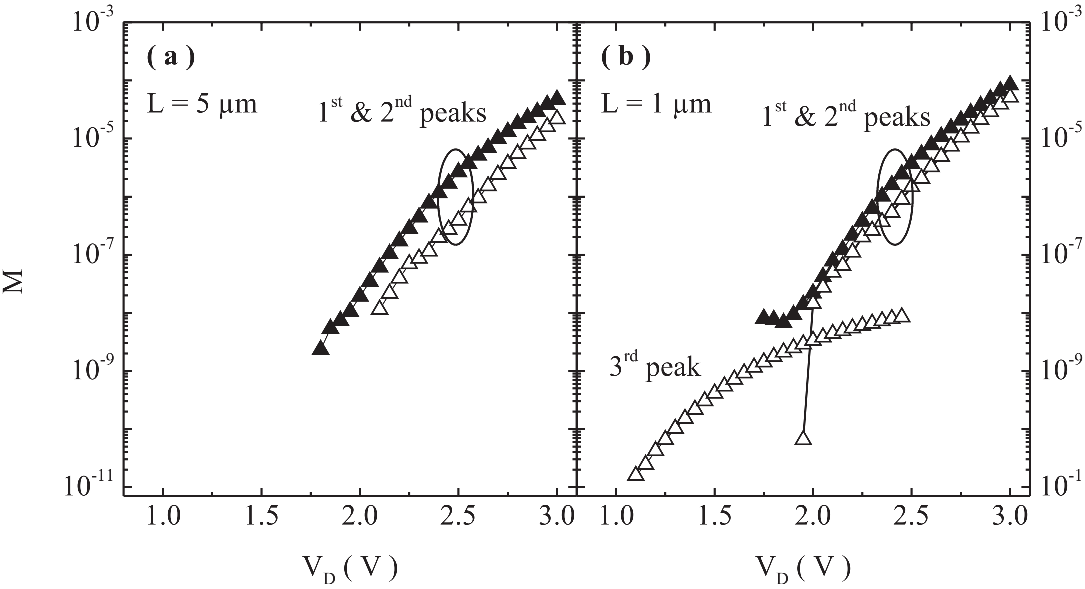


Figure 5.17: M vs V_D for devices of L equal to (a) $5\,\mu m$ and (b) $1\,\mu m$. M shown correspond to the peaks in I_{SUB} vs V_G. Filled symbols are for data at 300 K and open symbols for that at 77 K.

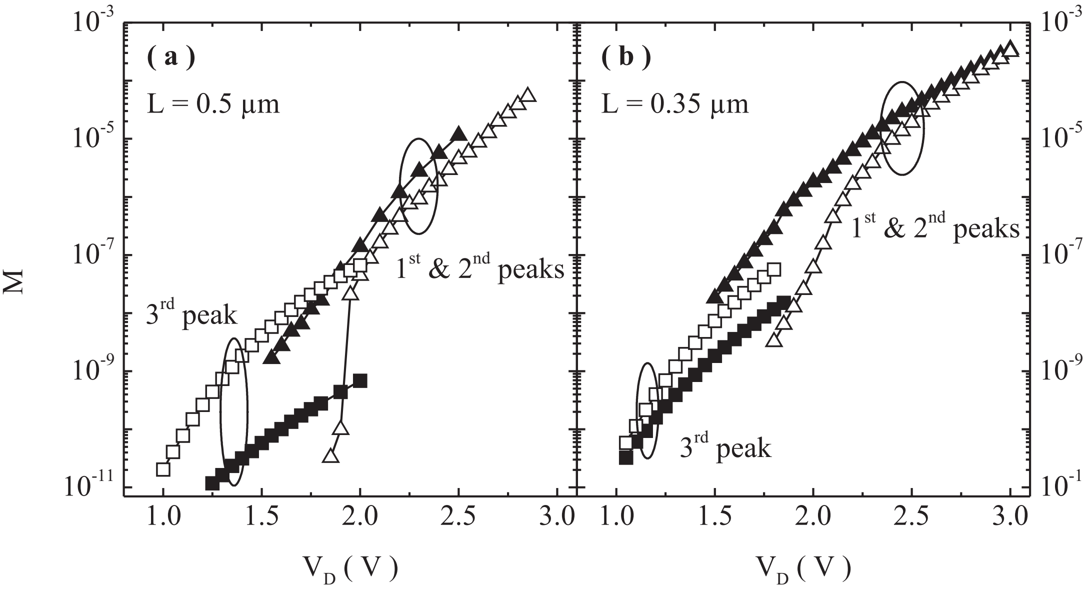


Figure 5.18: M vs V_D for devices of L equal to (a) $0.5\,\mu m$ and (b) $0.35\,\mu m$. M shown correspond to the peaks in I_{SUB} vs V_G. Filled symbols are for data at 300 K and open symbols for that at 77 K.

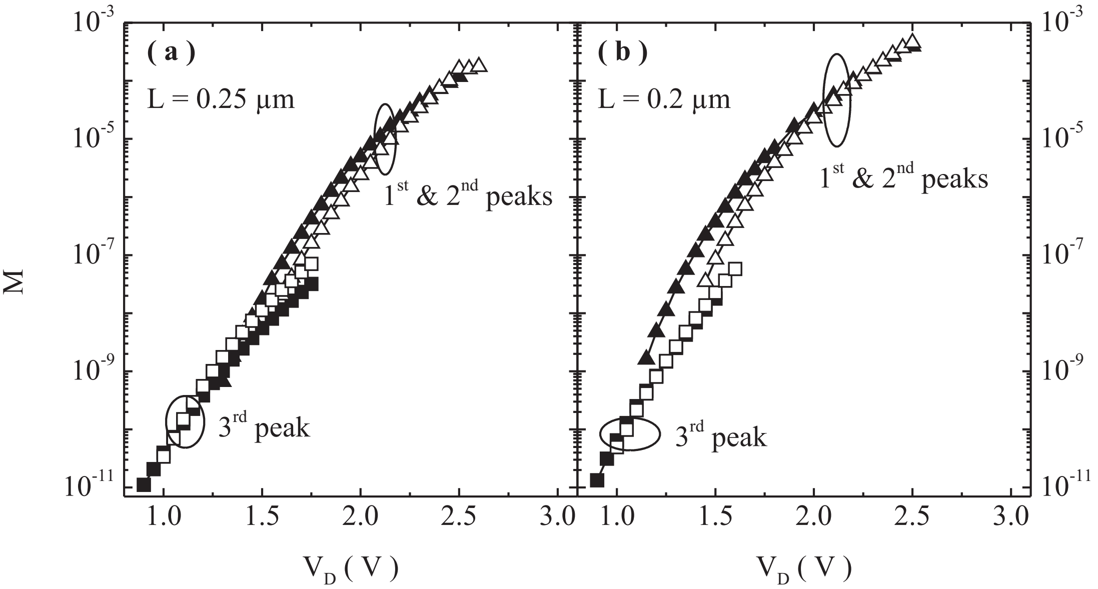


Figure 5.19: M vs V_D for devices of L equal to (a) $0.25\,\mu m$ and (b) $0.2\,\mu m$. M shown correspond to the peaks in I_{SUB} vs V_G. Filled symbols are for data at 300 K and open symbols for that at 77 K.

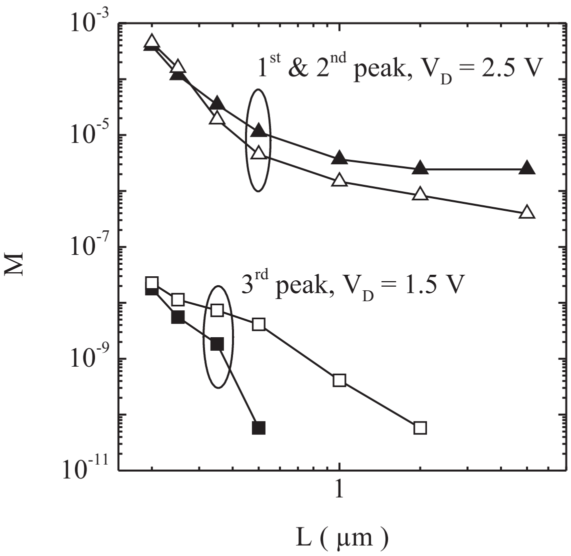


Figure 5.20: L dependence of M. The solid symbols show the data at 300 K and open symbols at 77 K.

as L is increased.

Figure 5.19 shows the data for the 0.25 and 0.2 μm devices. Cross-over is observed for the third peak and, the first and second peaks combined, for both L. There is an overall decrease in the differences between M at 300 and 77 K as L is reduced.

L dependence of M data is summarized in figure 5.20. M for a V_D of 2.5 V is chosen for the first and second peaks combined. In fact, only the first peak is captured at such a high V_D and this avoids the drastic changes in M that appears as the second peak become the dominant one. The third peak is represented by its value at $V_D = 1.5\,V$. We will only make comparison between the behavior at 300 and 77 K. The differences in V_D chosen is not a deterrent to that. M decreases as L increases. Down to $L = 0.25\,\mu m$, M corresponding to the third peak showed a negative temperature dependence whereas the first and second peaks combined showed a positive temperature dependence. M corresponding to the third peak is more sensitive to temperature than the first and second peaks. In the extreme case of the 2 μm device, the third peak makes an appearance only at 77 K.

5.3.3 Cross-over Voltage

Cross-over voltage (V_{XOVER}) extracted from figures 5.19a and b are shown in figure 5.21. V_{XOVER} for the first and second peaks combined is more than 2 V and increases with L. The range falls in the typical range of V_{XOVER} reported in the literature, table 2.1, and also found for our CON devices, chapter 3. L dependence is also identical to that of CON devices.

V_{XOVER} corresponding to the third peak are smaller than 1.25 V and decreases as L is increased. It was also mentioned previously that M vs V_D extrapolated for the third peak would cross-over for 0.35 and 0.5 μm devices, figure 5.18, and the extrapolated V_{XOVER} also show a negative L dependence.

5.4 I_{SUB} vs V_G in the Reverse Mode

In this section, I_{SUB} vs V_G characteristics of the LAC devices operated in the reverse mode are presented. For this mode, channel doping peaks right at the drain junction.

Performance of the devices in the reverse mode is severely degraded in certain aspects. DIBL is higher and punch-through voltage is lower in the reverse mode [81]. This is because the highest barrier to electron flow is at the drain side due to the high channel doping near the drain. When this region is depleted, the device can be easily turned on because the source barrier is low due to the low doping at the source junction. Another fall out of the heavy drain side doping is the early breakdown of the device. These issues become more severe as L is reduced. We would limit our investigations to $L \geq 0.5\,\mu m$ for these reasons. For the devices and configurations considered in chapter 4 and in this chapter so far, all the relevant features of I_{SUB} vs V_G plots were revealed for this range of L. It turns out that the case is not different for the reverse mode of operation.

Figure 5.22 shows I_{SUB} vs V_G plots for 0.5 μm devices at 300 and 77 K. Unlike in the forward mode, we observe only one peak at 300 and 77 K in this case. I_{SUB} for identical V_D is lower at 77 K than at 300 K. Impact ionization is observed for

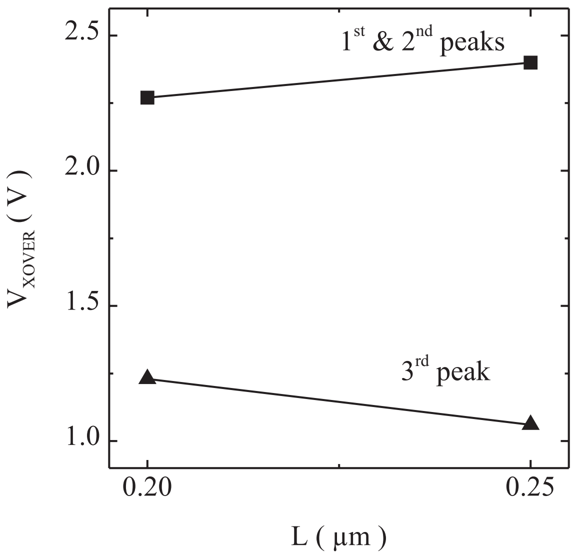


Figure 5.21: V_{XOVER} for the first and the third peaks as a function of L. V_{XOVER} shows opposite L dependence for the two cases.

$V_D < 0.8\,V$. This value is less than for CON devices of identical L , figure 4.2, and LAC operated in forward mode, figure 5.13.

The peak I_{SUB} condition was investigated as a function of V_D. Figure 5.23 shows $V_{Gpeak} - V_T$ vs V_D for LAC devices of $L = 0.5$ and $1\ \mu m$. As V_D is reduced, V_{Gpeak} also decreases and then shows a turn around for the lowest V_D values. The turn around is more pronounced for the shorter device and also at 77 K than at 300 K. These features are very similar to the behavior of V_{Gpeak} corresponding to the first and second peaks combined for operation in the forward mode. V_{Gpeak} values also have comparable range. Though we do not see any distinct second peak, the turn around in V_{Gpeak} is indication of the fact that the same physical mechanism that is responsible for the second peak in the forward mode, is at play in the reverse mode as well. No third peak was observed for devices of either L.

M corresponding to $I_{SUBpeak}$ as a function of V_D for the 0.5 and $1\ \mu m$ devices are shown in figure 5.24. M at 77 K is consistently lower for the V_D range investigated. No cross-over is observed.

5.5 Summary of Experimental Results

The results presented so far can be summarized as follows.
For the LAC devices operated in the forward mode :

1. Three peaks were identified in I_{SUB} vs V_G plots.

2. The third peak was observed for $L \leq 2\ \mu m$. For $L = 1$ and $2\ \mu m$, it was distinctly observed only at 77 K.

3. The second peak was observed at 77 K and distinctly visible for $L \geq 0.5\ \mu m$. At

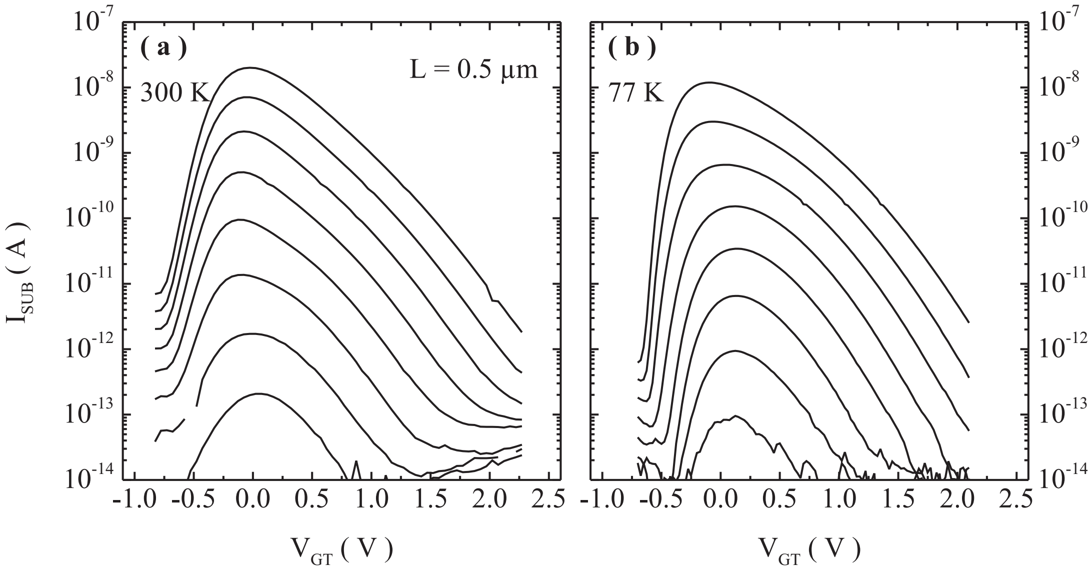


Figure 5.22: I_{SUB} vs V_G characteristics of a LAC device of $L = 0.5\,\mu m$ operated in the reverse mode, (a) at 300 K and (b) at 77 K. $V_D = 0.8$ to $1.5\,V$ in $0.1\,V$ steps.

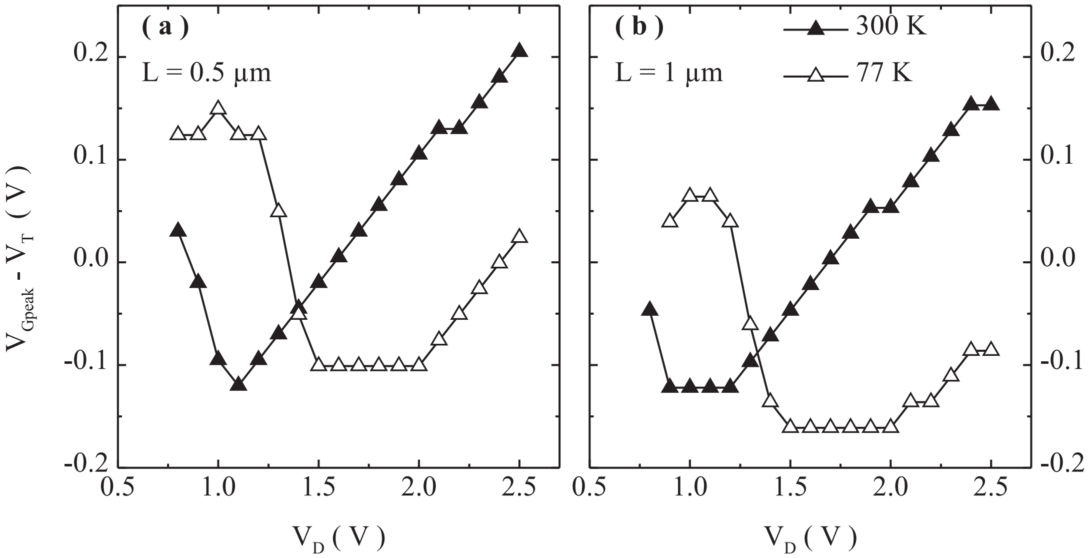


Figure 5.23: $V_{Gpeak} - V_T$ vs V_D for LAC devices of L (a) $0.5\ \mu m$ and (b) $1\ \mu m$. The devices were operated in the reverse mode.

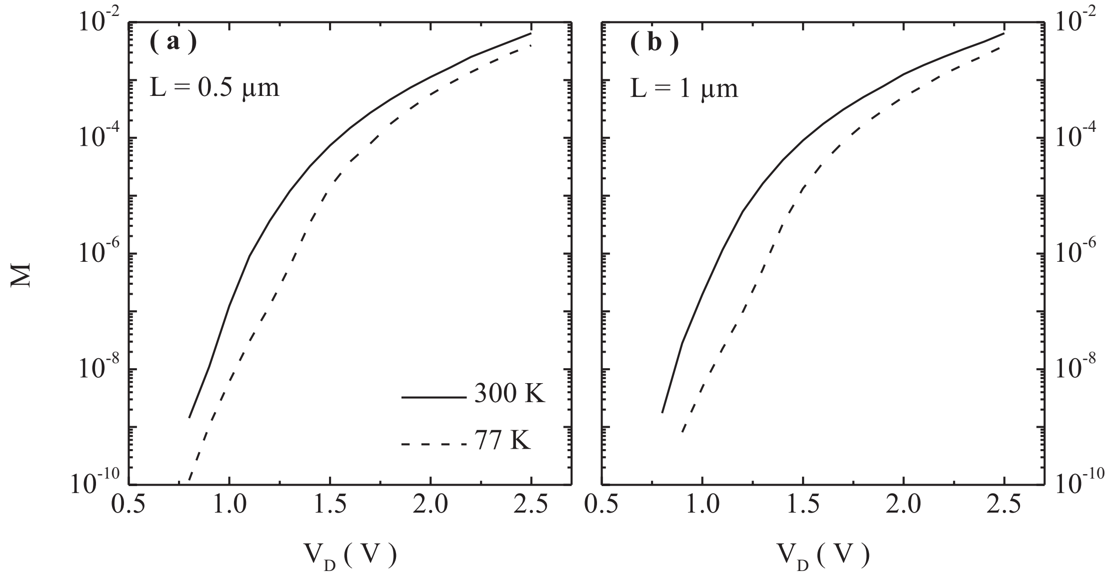


Figure 5.24: M vs V_D characteristics of LAC devices of L (a) $0.5\,\mu m$ and (b) $1\,\mu m$ operated in the reverse mode. M was evaluated for $I_{SUBpeak}$. M is consistently lower at 77 K.

300 K, the first bell was much broader and for very low V_D, it resembled more of a trapezoid than a bell for $L = 1$ and $2\,\mu m$.

4. For $L \leq 1\,\mu m$, at 77 K, V_{Gpeak} corresponding to the first and second peaks decreased as V_D was decreased and then increased again in the low V_D regime. For the 1 and $0.5\,\mu m$ devices this turn around was rather abrupt, which could be identified with the dominance of the second peak. For smaller devices the turn around was smooth and gradual. Such a turn around was observed for 0.25 and $0.2\,\mu m$ devices even at 300 K.

5. V_{Gpeak} vs V_D data for the third peak showed a monotonous behavior.

6. For $L \geq 0.35\,\mu m$, $I_{SUBpeak}$ for the first and second bells combined showed a positive temperature dependence, whereas the third peak showed a negative temperature dependence.

7. For $L = 0.25$ and $0.2\,\mu m$, cross-over was observed for both the third peak and the first and second peaks combined. In the first case $V_{XOVER} \sim 1.2\,V$ and showed a negative L dependence, whereas in the second case, $V_{XOVER} \sim 2.2\,V$ and showed a positive L dependence.

For the LAC devices operated in the reverse mode :

1. Only a single peak was observed both at 300 and 77 K.

2. V_{Gpeak} vs V_D showed a reversal for low V_D values.

3. M showed a positive temperature dependence.

5.6 Comparison with Conventional Devices

LAC devices operated in the forward mode have higher drive current than CON devices [81, 102, 103]. Comparison of I_{SUB} vs V_G data of conventional and LAC devices is worthwhile. First we would compare the shapes of I_{SUB} vs V_G plots. Comparison of features like V_{Gpeak} are then made.

Figure 5.25 shows a comparison of I_{SUB} vs V_{GT} data for CON device with that of LAC devices operated in the forward mode. The device length is 0.2 μm. In the case of conventional devices, even for the extended range of V_G, only one peak is observed both at 300 and 77 K. For identical V_D and for the V_{GT} range corresponding to the first bell of LAC, I_{SUB} is significantly lower than that of the conventional devices. However, as V_{GT} is increased, the third peak appears in the plots for LAC whereas I_{SUB} for CON devices continue to fall and finally I_{SUB} for LAC exceeds that of CON. V_{GT} at which I_{SUB} for LAC exceeds that of CON, increases with V_D.

Figure 5.26 compares the data for $L = 0.5\,\mu m$. For this L also, CON devices have only one peak in the I_{SUB} vs V_G plots. As was the case for the shorter devices, I_{SUB} for LAC exceeds that of CON for a certain value of V_{GT}. Crossing points are highlighted by circles in the plots.

Comparison of CON, and LAC devices operated in the forward mode, can be summarized as :

1. Whereas LAC operated in the forward mode has three peaks in the I_{SUB} vs V_G data, the conventional devices have only two (refer figures 5.12 and 4.6).
2. First two peaks of LAC show identical L and temperature dependencies as the two peaks of CON. The V_{GT} range are also similar. Specifically,
    (a) The minimum V_D for which the two peaks could be measured was higher for LAC than CON.
    (b) The second peak is much more pronounced at 77 K for both structures.
    (c) The second peak is much more pronounced and distinct in the case of LAC than CON.
    (d) For $L \leq 1\,\mu m$, and for the lowest V_D values, the second peak dominated at 77 K. As a consequence, V_{Gpeak} vs V_D data shows a non monotonous behavior. The turn around in V_{Gpeak} became smooth as L was decreased as a consequence of the merging of the two peaks. The non monotonous V_{Gpeak} vs V_D was observed even at 300 K for $L \leq 0.25\,\mu m$.
    (e) For LAC devices of $L = 0.25$ and $0.2\,\mu m$, a cross-over was observed in M vs V_D plots and the corresponding V_{XOVER} values were in the range of the V_{XOVER} values obtained in the case of CON devices in chapter 3. V_{XOVER} in both cases increased with increasing channel length.
3. Quantum yield corresponding to the third peak showed negative temperature dependence for $L \geq 0.35\,\mu m$. For $L = 0.25$ and $0.2\,\mu m$, a cross-over was observed. V_{XOVER} values were much smaller than that for the other case and decreased with increasing L.

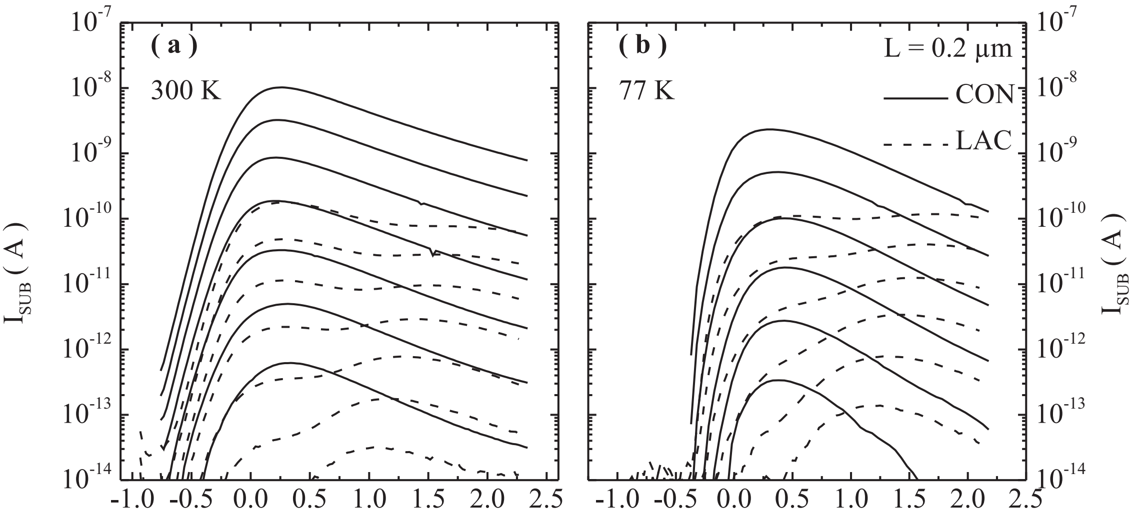


Figure 5.25: Comparison of I_{SUB} vs V_G data of CON and LAC devices of $L = 0.2\,\mu m$: (a) at 300 K, $V_D = 0.9$ to $1.5V$ and (b) at 77 K, $V_D = 1$ to $1.5V$. $\Delta V_D = 0.1V$. The LAC device was operated in the forward mode.

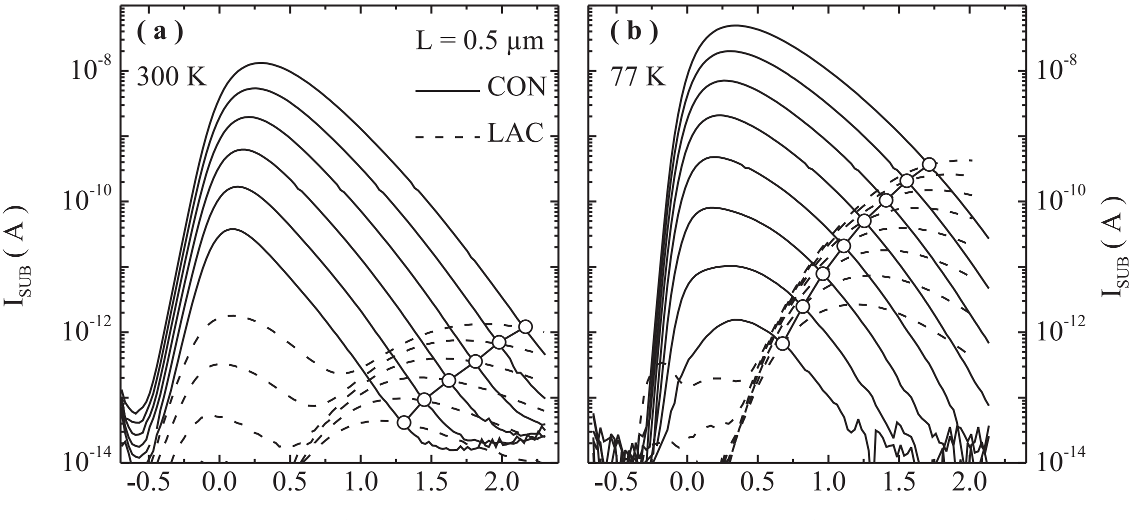


Figure 5.26: Comparison of I_{SUB} vs V_G data of CON and LAC devices of $L = 0.5\,\mu m$: (a) at 300 K, $V_D = 1.3$ to $1.8V$ in $0.1V$ steps, and (b) at 77 K, $V_D = 1.3$ to $2V$ in $0.1V$ steps. The LAC device was operated in the forward mode. The circles represent the points of intersection of the plots for the CON and LAC for identical V_D. For V_{GT} to the right of the intersections, the I_{SUB} for LAC is larger.

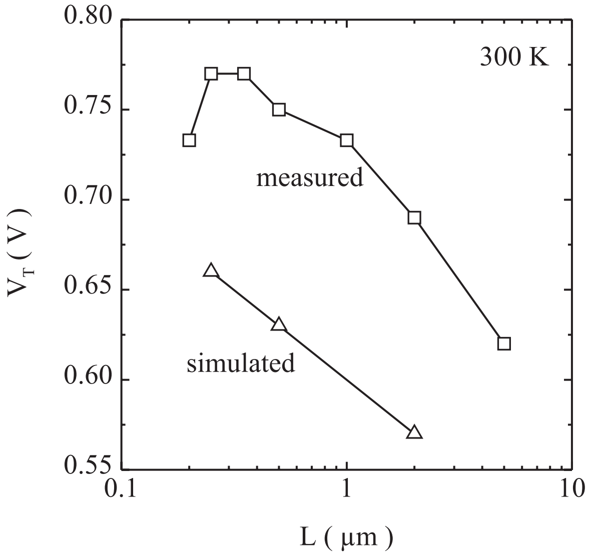


Figure 5.27: The measured and simulated V_T for the LAC devices operated in the forward mode at 300 K. The simulated values are ($\sim$) 0.12 V below measured. This margin was because the simulations do not include inversion layer quantization effects.

Comparison of CON, and LAC devices operated in the reverse mode, can be summarized as :

1. LAC operated in the reverse mode shows only one distinct peak.
2. V_{Gpeak} vs V_D shows non monotonous behavior at 300 and 77 K. This is more pronounced at 77 K. This observation is similar to that for CON. This suggests that the physical mechanisms responsible for the first and second peaks in the CON and LAC operated in forward mode are playing an important role in this case as well.

The comparisons suggest that identical physical mechanisms are responsible for the first and second peaks or their signatures in the case of CON, and LAC operated in both forward and reverse modes.

5.7 Analysis

In this section, experimental results presented in the previous sections are analyzed based on two dimensional drift-diffusion simulation data.

5.7.1 Simulations

Two dimensional drift-diffusion simulations were performed on LAC device structures using ATLAS [105]. Device structures were obtained by simulating the process flow using ATHENA [106]. Simulations were done to obtain qualitative ideas about the physical processes responsible for the anomalous I_{SUB} vs V_G characteristics. Default models of ATLAS and ATHENA were used. Even though we have not attempted to

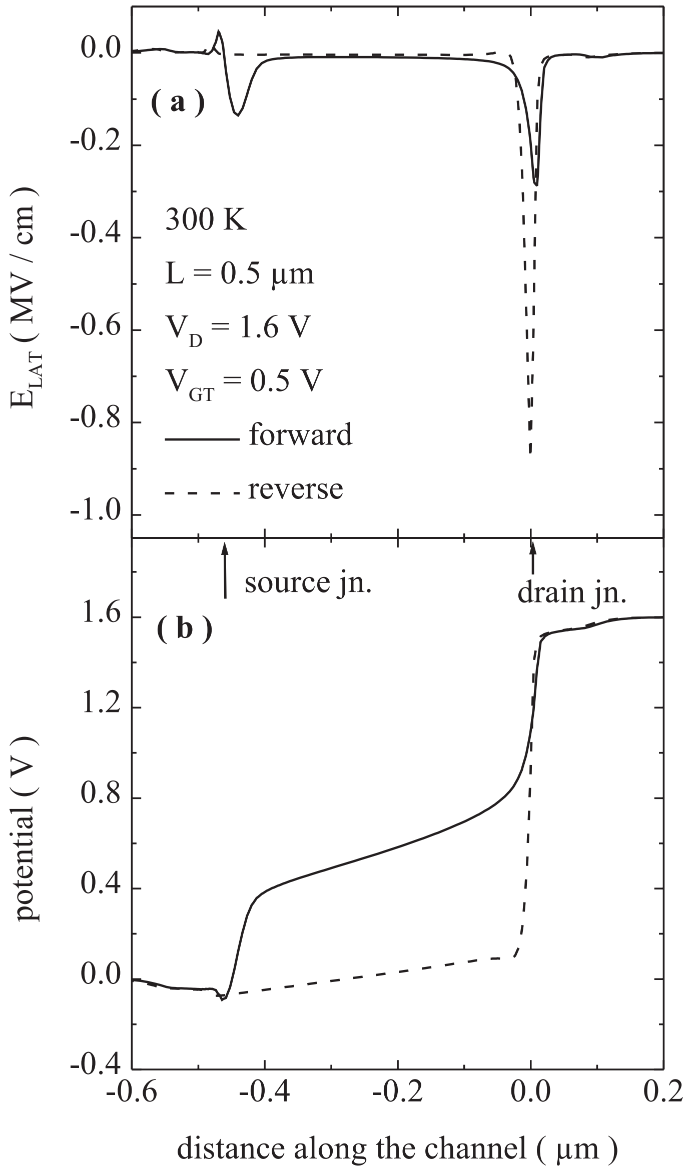


Figure 5.28: Simulated E_{LAT}, (a), and potential, (b), along the channel of a $0.5\,\mu m$ LAC device in the forward and reverse modes of operation. The profiles shown are for a cutline 1 nm below the interface. Drain junction is taken as the reference.

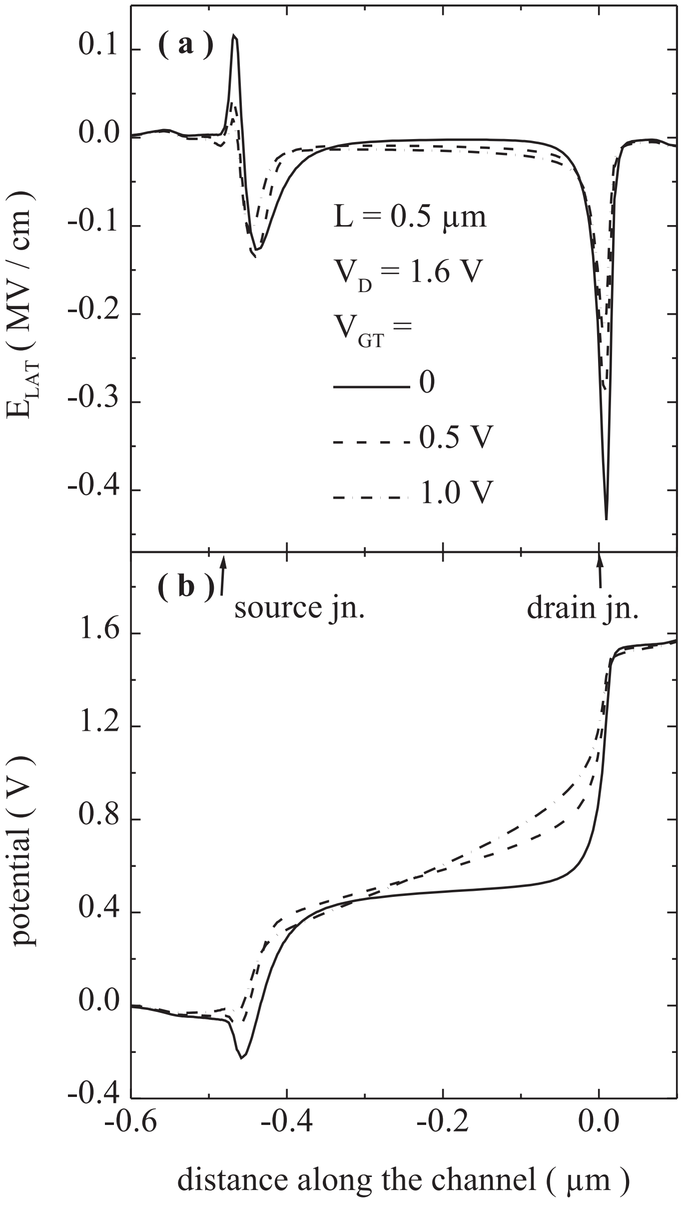


Figure 5.29: Simulated E_{LAT}, (a), and potential, (b), along the channel of a $0.5\,\mu m$ LAC device in the forward mode for various V_{GT}. The profiles shown are for a cutline 1 nm below the interface. Drain junction is taken as the reference.

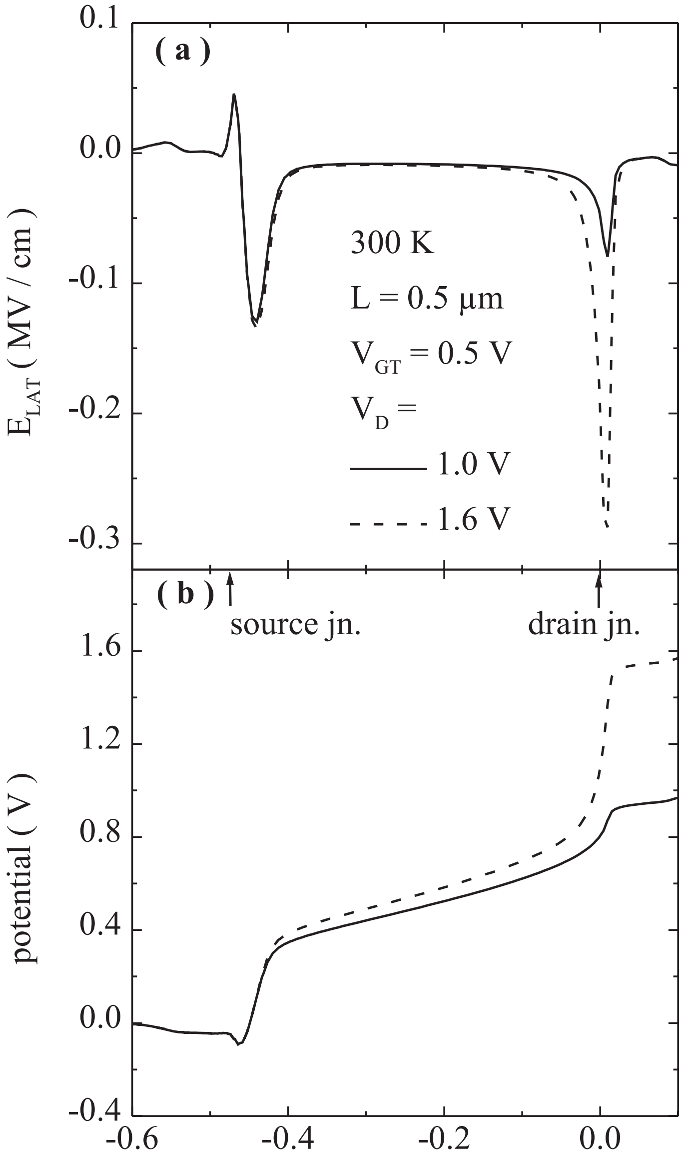


Figure 5.30: Simulated E_{LAT}, (a), and potential, (b), along the channel of a $0.5\,\mu m$ LAC device in the forward mode for various V_D. The profiles shown are for a cutline 1 nm below the interface. Drain junction is taken as the reference.

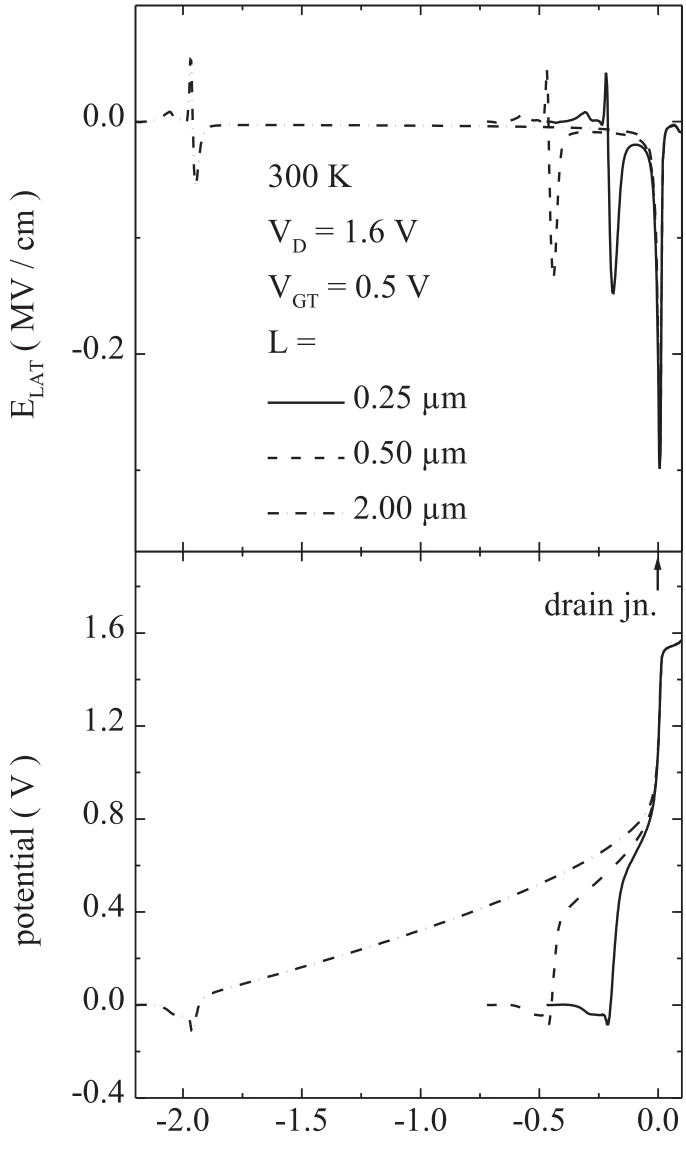


Figure 5.31: L dependence of E_{LAT}, (a), and potential, (b), for LAC devices in the forward mode. The profiles shown are for a cutline 1 nm below the interface. Drain junction is taken as the reference.

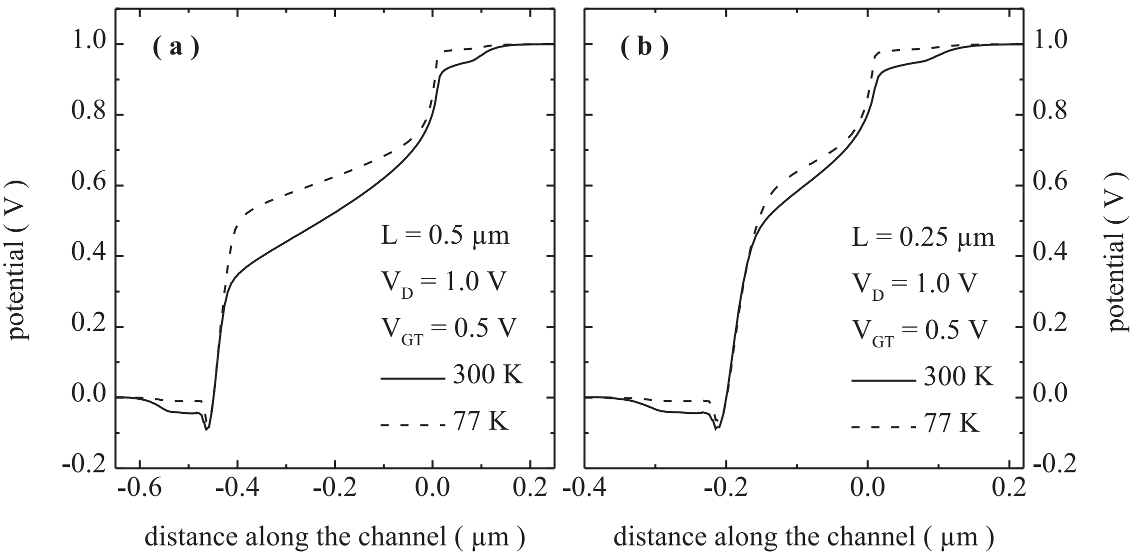


Figure 5.32: Temperature Dependence of the potential profile for (a) $0.5\,\mu m$ and (b) $0.25\,\mu m$ LAC devices in the forward mode. The profiles shown are for a cutline 1 nm below the interface. Drain junction is taken as the reference.

tune the models to reproduce the measurement results, the models employed reproduce the trends in I_D accurately [81]. The measured and simulated V_T are shown in figure 5.27 for the forward mode of operation. Simulated V_T were matched to ($\sim$) 0.12 V below the measured values. Such a margin was allowed since the simulations we employed does not include inversion layer quantization effects. One dimensional consistent Poisson-Schrödinger simulations for CON devices had shown a 0.1 V increase in V_T due to surface quantization. For LAC devices it is difficult to assess the effect, due to the two dimensional doping profile. We expect the effect to be more due to the higher channel doping on the source side and hence the slightly higher V_T off-set than obtained for CON devices.

When the device was biased as shown in figure 5.1, the operation mode is called forward mode. When the biasing is reversed to make the heavily doped N+ region close to the peak channel doping positively biased, the operation mode is called reverse. In the reverse mode the N+ region near the heavily doped channel region is drain and the other N+ region is source.

Figure 5.28 shows E_{LAT} and the potential along the channel of a $0.5\,\mu m$ LAC device simulated both in the forward and reverse modes. Drain junction is taken as the reference for the distance along the channel. Field and potential were taken along a cutline 1 nm below the interface. When the device is operated in the reverse mode, there is only one high field region near the drain. Almost all the applied potential falls in this high field region. When the device is operated in the forward mode, there are two high field regions, one near the drain and the other in the heavily doped channel region. Applied V_D is divided between these two regions. Correspondingly the potential drop across either high field region is much less than V_D.

The field and potential distributions along the channel for the reverse mode of operation are identical to the case of the CON devices in that only one peak is observed in either case. Since the experimental data obtained for the reverse mode of operation also show similar trends as the CON devices, it can be concluded that the explanations of the observed data would be identical. For the same reason, only the simulation data for the reverse mode are analyzed in detail.

The two peaked field distribution for the forward mode of operation is similar to the case of source side non-overlap structures [87, 88], even though the process simulations in our case does not show any non-overlap. The non-overlap structures have significantly higher parasitic resistance, causing a degradation of current drive. Suppose that the tilted implant causes a non-overlap on the source side for the source-drain configuration shown in figure 5.1. There will be a parasitic series resistance associated with the non-overlap region which will degrade the device performance. In the reverse mode of operation, the non-overlap region will be on the drain side and will be depleted when a V_D is applied. Consequently, the source non-overlap structure is expected to have a higher current drive when operated in the reverse mode [88]. This is not the case for our devices, refer figure 5.4. B. Cheng [81] also reported that similar LAC devices, operated in the reverse mode has lower current drive compared to forward mode of operation. These results support the simulation result that the tilted implant does not produce a non-overlapping structure. The device simulation results suggest that two peaked field distributions are possible even in structures that do not suffer from non-overlapping.

Figure 5.29 shows E_{LAT} and the potential along the channel of a $0.5\,\mu m$ LAC device simulated in the forward mode for $V_D = 1.6\,V$ for $V_{GT} = 0$, 0.5 and $1\,V$. As V_{GT} is increased, the peak lateral electric field ($E_{LATpeak}$) near the drain junction decreases consistently. However, $E_{LATpeak}$ near the source does not decrease significantly as V_{GT} is increased from 0 to $0.5\,V$. This is also reflected in the potential distribution. When V_{GT} is increased to $1\,V$, the source side peak decreases. It may also be noted that the potential drop in the channel regions excluding the high field regions increases with increasing V_{GT}.

V_D dependence of the relative magnitudes of $E_{LATpeak}$ in the two high field regions were investigated. Figure 5.30 shows E_{LAT} and the potential along the channel of a $0.5\,\mu m$ LAC device simulated in the forward mode for $V_{GT} = 0.5\,V$ and $V_D = 1$ and $1.6\,V$. Whereas the potential drop in the high field region near the drain is significantly increased, that near the source side is only marginally increased. For $V_D = 1\,V$, the drop in the source side high field region is significantly higher than that in the drain side high field region.

L dependence of the two peak field regions are shown in figure 5.31. V_D was kept constant at $1.6\,V$ and V_{GT} at 0.5 V. The drain junction is taken as the reference and hence, in the figure, the high field region near the drain overlaps for all the devices. The right most peak in E_{LAT} corresponds to the drain side high field region and the other three peaks corresponds to the source side high field region for the three values of L. The field and potential distributions near the drain junction are nearly independent of L. On the contrary, potential drop near the source end decreases as L is increased. As can be appreciated from the figure, this is because, longer the channel larger the potential drop in the channel region excluding the two high field regions.

Temperature dependence was investigated for devices of $L = 0.5$ and $0.25\,\mu m$ for $V_D = 1\,V$ and $V_{GT} = 0.5\,V$. The results are shown in figure 5.32. Potential drop in the high field regions increases with decreasing temperature. Reduced phonon scattering result in lower channel resistance and the potential drop in the channel region excluding the high field regions decrease with decreasing temperature. This result in a higher drop in the source side high field region. For the 0.5 μm device the source side potential drop has a higher temperature sensitivity than that for the 0.25 μm device.

5.7.2 Interpretation of I_{SUB} vs V_G Data for the Forward Mode of Operation

The experimental data obtained for the forward mode of operation of the devices are interpreted. Since the reverse mode of operation resembles the CON devices as far as the field distribution is considered, this case is not analyzed in great detail.

5.7.2.1 The First and Second Peaks

The first and second peaks combined can be associated with the high field region near the drain. This can be deduced from the following observations :

1. They are observed for CON and LAC devices operated in the reverse mode. Even though in the case of short channel devices the second peak was not distinctly visible, its signature, reversal in V_{Gpeak} vs V_D in the low V_D regime, have shown identical trends. Simulations have shown that there is only one high field region, which is near the drain junction, in the case of the conventional devices and the LAC operated in reverse mode, figure 5.30.

2. The first and second peaks combined, for LAC in forward mode, show a higher sensitivity to V_D than the third peak, figure 5.18. Simulated $E_{LATpeak}$ and potential drop in the high field region near the drain is more sensitive to variations in V_D than those in the source side high field region.

3. V_{Gpeak} vs V_D corresponding to the first and second peaks combined, for LAC in forward mode, showed identical trends as the same kind of plots for the other two cases.

The above arguments further support the energy gain and redistribution picture presented in figure 4.17. The electrons heated in the high field region near the drain also interact with similar other electrons and gain or lose energy. Such short-range interactions result in the broadening of the EED tail. Since EEI becomes stronger as the electron density is increased, I_{SUB} vs V_G can have two peaks. At 300 K, since the thermal tail of the EED can be quite significant, the transition from the thermal tail to EEI broadened tail is less distinct than at 77 K.

It should be emphasized here that the experimental and simulation results do not suggest that the second peak in I_{SUB} vs V_G is associated with a high field region in the device that is different from the one which causes the first peak.

L dependence of V_{XOVER} corresponding to the first and second peaks combined, which is identical to that of CON devices, further support the conclusion that these peaks are caused by high field region at the drain side of the channel.

Since we have shown that the first and second peaks in I_{SUB} vs V_G for all the cases studied so far are due to the same reasons, and the trends in V_{Gpeak} and the channel dependence are identical in all the cases, the physical mechanisms and their dependence on applied biases are identical. Since these points were discussed in detail in chapter 4, only the significant features and differences are discussed here.

A significant difference between the three cases of impact ionization discussed in the previous and present chapter are the relative visibility of the second peak. The visibility of the second peak increases in the order : LAC in reverse mode, conventional and then LAC in forward mode. On the other hand the channel doping concentration near the drain junction decreases in the same order. Field heating is higher when the doping is higher. This is because the depletion region is shorter for an applied voltage. This argument is supported by the fact that the peak I_{SUB} corresponding to the first and second peaks combined, increases in the order : LAC in the forward mode, conventional and then LAC in the reverse mode. However the ionized impurity scattering also increases with increased doping. Ionized impurity scattering even though an elastic scattering process, may indirectly enhance the other scattering mechanisms by randomizing the electron trajectories. This can enhance the short-range EEI and electron-phonon interactions.

Quantifying the impact of the indirect role of the ionized scattering on the EED at the device level is difficult because the process is accurately captured only when the simulation grid size is comparable to the lattice constant. Memory requirements of such a simulation will be tremendous. However such modeling approaches may be successful in ultra-small devices.

Improved visibility of the second peak at 77 K may be due to a greatly suppressed thermal tail. Transition from the field heated plus thermal tail dominated impact ionization, to the field heated plus EEI broadened tail dominated impact ionization, is expected to be smoother at 300 K due to the broader thermal tail.

We had also seen in the case of the conventional devices that, the visibility of the second peak may be correlated to the evolution of $E_{LATpeak}$ with V_G. This was one of the reasons for the dominance of the second peak in shorter devices at very low V_D for the conventional structure. However, a qualitative comparison between the three device structures is difficult from a peak lateral field perspective because of the differences in doping profiles.

5.7.2.2 The Third Peak

The third peak observed in the case of the forward mode of operation of LAC devices present difficult challenges to interpretation. In the present section we would try to relate some of the experimental observations qualitatively with the simulation results.

The third peak can be correlated to the high field region near the source end. This is supported by the following observations.

1. The third peak was observed only for $L \leq 2\mu$. Also $I_{SUBpeak}$ is strongly dependent on L. Simulation results have shown that the potential drop in the source side high field region decreases with increasing L, figure 5.31.

2. The third peak increases with decreasing temperature for $L \geq 0.35\mu$. We have seen in figure 5.32 that the potential drop in the source side high field region

enhances significantly with reduction in temperature. This is because of the reduced potential drop in the channel region excluding the two high field regions. However, as L decreases, potential drop in the source side high field region is not significantly enhanced as the temperature is reduced, figure 5.32.

3. V_{Gpeak} corresponding to the third peak is much higher than that corresponding to the first and second peaks. Potential drop in the source side high field region is less sensitive to V_G variations than that in the drain side high field region.

4. The first peak I_{SUB} is much more sensitive to V_D than the third peak I_{SUB}. For large V_D the first peak completely dominates I_{SUB} vs V_G curves. Simulation results show that the potential drop in the source side high field region is less sensitive to V_D than that in the drain side high field region.

The experimental observations and the simulation results correlate qualitatively. However, the simulation results also show that for LAC operated in forward mode, $E_{LATpeak}$ of either high regions is decreasing with increasing V_G. Then why should there be separate peaks in I_{SUB} vs V_G for each high field region? We had seen in the case of CON devices that the first peak is the optimization point of the number of electrons potentially available to cause impact ionization which increases with V_G and the field heating which decreases with V_G. In the case of LAC operated in the forward mode, there are two electric field peaks. The peak field near the drain decreases much more rapidly with V_G than the peak field near the source, figure 5.29. So the optimization point of the drain side field and the electron density can be different from the optimization point of the source side field and the electron density leading to separate peaks in I_{SUB} vs V_G for the two high field regions.

Negative temperature dependence of the third peak may partly be explained by the positive temperature dependence of the potential drop in the source side high field region. The EEI may also be playing a greater role in deciding the shape of the EED in the high field region near the source.

Negative L dependence of V_{XOVER} can be explained as follows. For conventional devices we had seen that the positive L dependence of V_{XOVER} is caused by decreasing field heating as L is increased. However, in the case of the source side high field region in LAC devices operated in the forward mode, potential drop in the high field region increases as the temperature is reduced. Due to this fact the effect of the increased impact ionization threshold has an impact on I_{SUB} for much lower V_D than for the conventional case. This pushes V_{XOVER} low. The enhancement in potential drop was also higher for the longer devices resulting in a negative L dependence.

The high field region near the source is caused by the presence of the doping gradient. A careful look at the simulation data presented for LAC in forward mode shows that the peak of the electric field near the source side is not exactly at the source junction. E_{LAT} at the source junction is very low. The inversion layer quantization at this point will have a significant impact on the energy distribution. We had seen in the previous chapter that the inversion layer quantization cause an off-set in the EED. Electrons with such an EED is directly injected into a high field region. Consequently the role of the inversion layer quantization may be more significant in the present case.

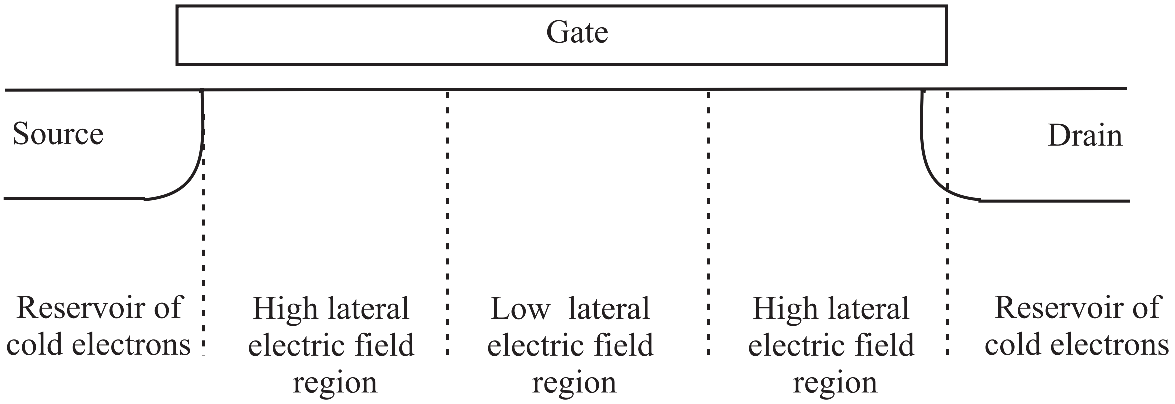


Figure 5.33: Schematic showing different regions of field heating and energy redistribution mechanisms in a LAC device operated in the forward mode. For a detailed discussion refer to the accompanying text.

5.7.2.3 Differences between Electron Heating Near the Source and Near the Drain

The differences between the carrier heating in the high field regions near the source and drain can be appreciated with reference to figure 5.33. The figure divides the LAC MOSFET operated in the forward mode into five regions. The source and drain are heavily doped with donor type of impurities and are reservoirs of cold electrons. There are two different high field regions, one near the source junction and another near the drain junction. These two regions are separated by a low E_{LAT} region.

Electron concentration in the low field region can be very high. This is because the concentration is proportional to V_{GT} which is higher in this region due to the low local V_T. Note that the low field region has an extremely low doping ($\sim 10^{15}\, cm^{-3}$). High inversion layer concentration can enhance short-range electron-electron interactions in this region. Since the doping is also lower in this region, EEI are expected to be more efficient.

Electron heating in the drain side high field region is similar to that in a conventional structure with just one high field region. Electrons are heated by field and the EED tail may be broadened by energy redistribution through short-range EEI.

Carrier heating in the high field region near the source can be described as follows. Cold electrons are injected from the source into the high field region. Electrons are heated by the high field. Short-range interactions in the high field region and the low field region following it, may play an important role in deciding the shape and population of the high energy part of EED. Monte-Carlo simulation results published have indicated that the impact ionization need not occur in the high field region itself for low potential drop in the high field region. For example, in a conventional MOSFET, the impact ionization occurs mostly in the drain, rather than in the pinch-off region, for low V_D. If this can be extended to field heating near the source junction, the impact ionization occurs mostly not in the high field region. The enhanced EEI in the low field region may significantly broaden the EED.

Since the carriers from the source are directly injected into a high field region, the resulting EED can be significantly influenced by the source carrier distribution. As

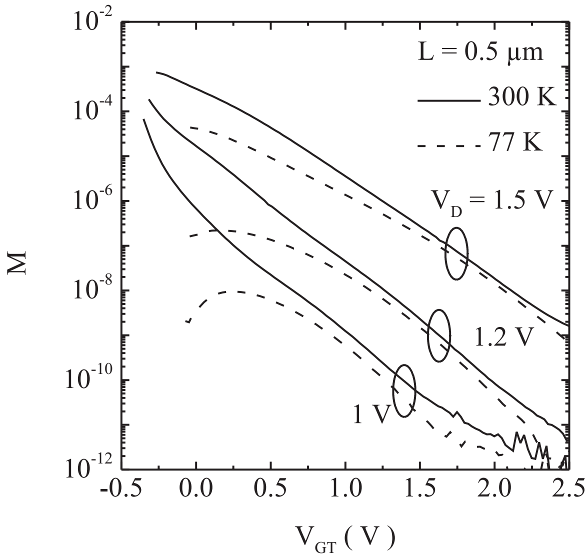


Figure 5.34: Measured quantum yield at 300 and 77 K for an LAC device of L $0.5\,\mu m$ operated in the reverse mode.

discussed in chapter 2, MC simulations of Fischetti and Laux [74, 75] have predicted significant modifications of the average energy of the electron gas and departure from Maxwell-Boltzmann Distribution due to long-range EEI in the source.

For very short devices, the broad EED emerging from the source side high field region may not be completely thermalized in the “low field region”.

The LAC device operated in the forward mode may be the kind of structure in which the predictions of Fischetti and Laux may be verified. Fischetti and Laux also speculated that the long-range interactions will be a physical mechanisms which seriously degrade the performance of ultra-short channel devices. However the verification of these predictions need not wait for sub-100nm technologies to mature. The speculations in the present section, when further explored using Monte-Carlo tools with appropriate physical models may provide important insights into the extent to which the long-range interactions can influence electron transport.

5.7.3 Further Support for the Verification of the EED Tail

The nature of the high energy tail of electron energy distribution near the drain junction was verified in chapter 4 for devices with a single high field region near the drain. The nature of the tail, especially the thermal tail and EEI broadening of the tail were verified from the general result that, in the absence of an energy gain or redistribution mechanism that has a positive dependence on V_G, the population of EED beyond W_G decreases as V_G is increased. We provide further support for this by investigating the evolution of M with V_G at 300 and 77 K.

The LAC devices when operated in the reverse mode resembles the situation of the CON device in that there is only one high field region. Therefore the nature of the EED tail can be expected to be similar to the case of the CON devices. This is indeed the case is shown in figure 5.34.

Figure 5.34 shows the evolution of M with V_G at 300 and 77 K for a LAC device of $L = 0.5\,\mu m$ operated in the reverse mode. The data are shown for $V_D = 1$, 1.2 and $1.5\,V$. At 300 K, M decreases monotonously for all V_D values. However for $V_D = 1\,V$, $qV_D < W_G$, M shows an initial increase, a peak and then a decrease as the V_G is increased. As the V_D is increased, this non monotonous behavior gradually disappears. This observation is exactly the same as that for the CON devices, figure 4.9, and confirm the conclusions we derived on the nature of the EED tail in chapter 4.

For LAC operated in the forward mode, the nature of the EED tails corresponding to either high field regions is difficult to speculate due to the complexity of the field distributions and the nature of the secondary energy gain and redistribution mechanisms.

5.8 Conclusions

Impact ionization in laterally asymmetrical channel (LAC) MOSFETs were investigated in both forward and reverse modes of operation at 300 and 77 K for channel lengths from 0.2 to $5\,\mu m$.

In the forward mode, three distinct peaks were observed in the I_{SUB} vs V_G characteristics. The first peak was observed for all devices at both the temperatures. The second peak was observed only at 77 K. The second peak was found to dominate and merge with the first one for $L \leq 0.35\,\mu m$, resulting in a turn around in V_{Gpeak} vs V_D, where V_{Gpeak} is the gate voltage at which the substrate current peaks. The third peak was observed for $L \leq 2\,\mu m$. For $0.35\,\mu m \leq L \leq 2\,\mu m$, it showed a negative temperature dependence and was observed for $qV_D < W_G$, where W_G is the bandgap of silicon.

Cross-over was observed in I_{SUB}/I_D vs V_D for the first and third peaks for $L = 0.25$ and $0.2\,\mu m$. Cross-over voltage corresponding to the first peak showed a positive channel length dependence and that corresponding to the third peak showed a negative channel length dependence.

In the reverse mode, only one peak was observed in I_{SUB} vs V_G characteristics. However, a turn around in V_{Gpeak} vs V_D was observed.

These results were compared with those obtained for the conventional devices presented in chapter 4. The first and second peaks for the forward mode and the turn around for the reverse mode of operation compared well with similar results for the conventional devices.

For certain channel lengths, I_{SUB} for LAC operated in the forward mode was greater than that for the conventional devices for low V_D and large V_G values. This result suggest that the LAC device need not be better than conventional in terms of hot-carrier effects under real operating bias conditions.

Two dimensional drift-diffusion simulations showed the presence of two peaks in the lateral electric field profiles, one near the source junction and another near the drain junction. The gate and drain bias and temperature dependencies of the two electric fields were compared with that of the first and third peaks in I_{SUB} vs V_G. It was established that the first and the third peaks are caused by the high field regions near the drain and source respectively.

However, the second peak could not be associated with any specific high field region.

By comparing the results of the conventional devices and the LAC devices operated in the forward and reverse modes we have shown that the second peak is associated with strong short-range electron-electron interactions in the drain side high field region.

Differences in the roles of long-range interactions on electron transport in the two high field regions for the forward mode of operation are speculated. Electrons are directly injected into the source side high field region from the source. This may result in a significant enhancement of the tail of the electron energy distribution (EED) in the high field region if the source EED has higher average energy and broader tails due to long-range interactions. The LAC devices operated in the forward mode is highly suited to investigate the role of long-range interactions on electron energy distribution and transport.

Since the electrons are injected over the source junction barrier into a high field region, the role of inversion layer quantization presented in the previous chapter on EED in the source side high field region may be higher than speculated for conventional devices discussed in chapter 4.

Analysis presented in this chapter were based on electric field and potential profiles obtained from two dimensional drift-diffusion simulations. However a complete physical picture may only be obtained using a Monte-Carlo simulator which include appropriate models for quantization effects and short and long-range electron-electron interactions.

Chapter 6

Low Voltage Hot-Electron Device Reliability

In previous chapters we had presented experimental data that provided useful information on electron energy distributions (EED) in deep-sub-micron devices. Specifically we established experimental signatures for secondary energy gain and redistribution mechanisms and their influence on the tail of the distribution. We have also seen the influence of channel length scaling and gate voltage variations on short-range electron-electron interactions (SREEI). In the present chapter we will illustrate impact of low supply voltage hot-carriers in the tail of EED on device operation in vertical n-channel floating body MOSFETs and hot-carrier degradation in lateral n-channel MOSFETs.

Section 6.1 presents experimental data on floating body effects in 0.06 and 0.12 μm channel length (L) vertical MOSFETs for sub bandgap drain voltage (V_D). Direct current measurements were also employed to explore gate current (I_G) for V_D below the $Si - SiO_2$ barrier height.

In section 6.2, sub bandgap impact ionization and sub-barrier hot-carrier degradation in lateral devices with gate oxide thicknesses (t_{OX}) of 3 and 5 nm are presented. These devices were fabricated at Infineon AG, Germany.

6.1 Hot-Carrier Effects in Vertical MOSFETs

In this section we illustrate floating body effects for qV_D below W_G and I_G for qV_D below the $Si - SiO_2$ barrier height in vertical MOSFETs fabricated using molecular beam epitaxy (MBE).

6.1.1 Device Structure

Structure of the devices used in the present study is shown in figure 6.1a. It is similar to the surrounding gate transistor presented by Takato et al. [107]. Channel region of the transistors studied in the present case are formed by MBE. L can be controlled independent of lithography and arbitrary doping profiles along the channel with nanometer scale spatial resolution can be obtained. Another advantage of this structure is that the doping profile along the channel can be obtained using secondary ion mass spectroscopy (SIMS). These factors make the structure very attractive as a test device for research.

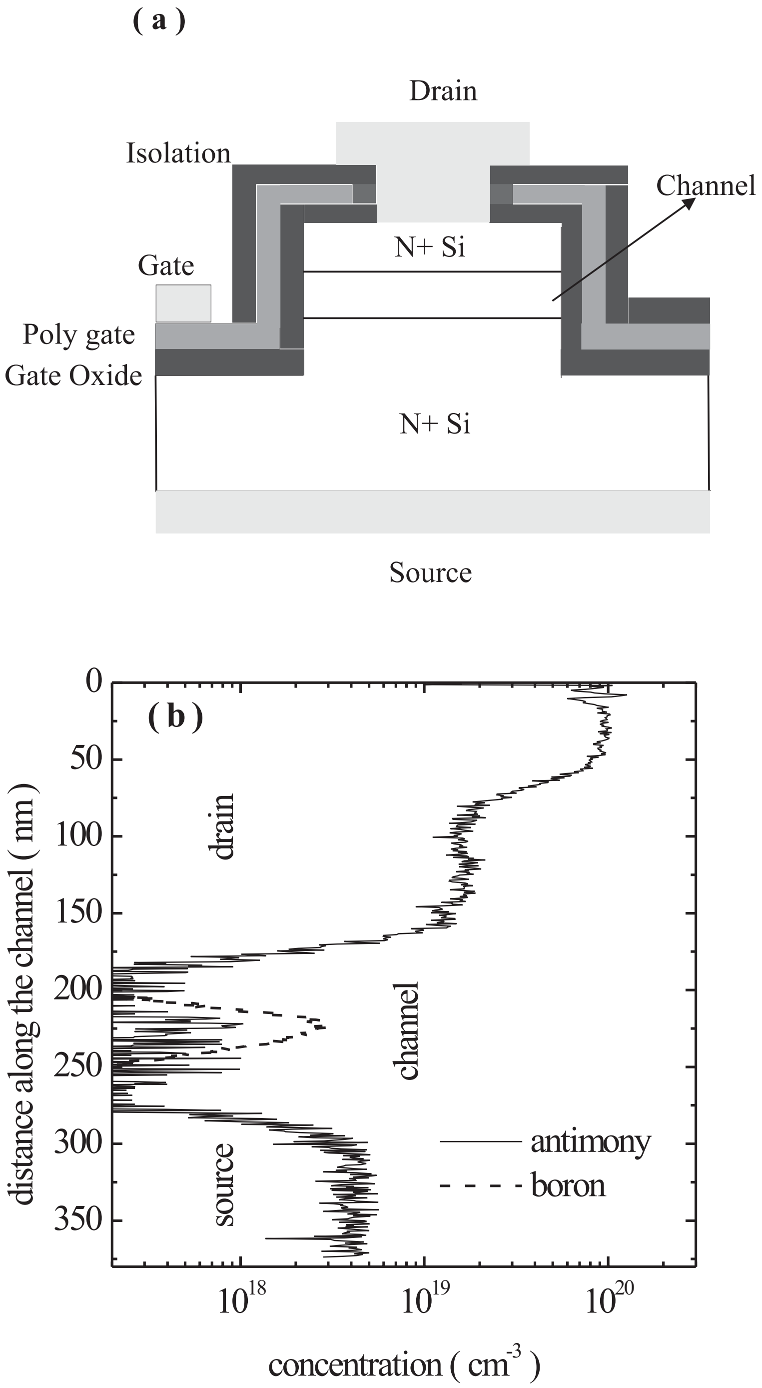


Figure 6.1: (a) Schematic of the structure of the vertical MOSFET used in the present study. Not to scale. (b) The doping profile along the vertical direction obtained using SIMS of a device of $L = 0.12\,\mu m$.

Device fabrication procedure is briefly outlined in the following. Details can be found in [100, 108]. On an N^+ doped $< 100 >$ silicon substrate, silicon layers were grown using MBE. N^+ source layer - undoped silicon layer - heavily boron doped silicon layer with a typical thickness of 5 nm - undoped silicon layer - N^+ drain layer were grown in that order. Then mesas of various dimensions were etched using reactive ion etching (RIE). Low temperature thermal oxides were formed to make the gate dielectric layer. This was followed by poly-silicon deposition and structuring. The gate was isolated using a deposited silicon nitride. Contact holes were then etched to define the gate and drain contacts. Silicon dioxide was removed from the back side of the wafer. The back side was then metalized and used as the source contact. The devices have no body contact and hence they belong to the class of devices called floating body MOSFETs. Process flow for the devices and manufacturability data can be found in Appendix B.

We investigate devices of $L = 0.12$ and $0.06\,\mu m$ in this section. Gate oxide thickness was determined to be 15 nm from transition electron micrograms (TEM) [108]. SIMS profiles for a device of $L = 0.12\,\mu m$ are shown in figure 6.1b. In this particular case, boron profile resembles a Gaussian with the peak near the center of the channel. Performance advantages of such structures in comparison to conventional structures can be found in [108]. The structure provides an opportunity to precisely define the doping profile along the channel and performance optimization. Hot-carrier reliability issues of these devices were explored in [103]. Devices with doping profiles similar to that shown in figure 6.1b are reported to be more robust to hot-carrier damage than conventional devices. Device optimization issues were explored in [109].

6.1.2 Impact Ionization

In this subsection, impact ionization and some of its implications for device operation are illustrated. Since the devices do not have a body contact, impact generated substrate current (I_{SUB}) can not be measured. Instead we would look for signatures of impact ionization in device characteristics.

Figures 6.2 and 6.3 show the output characteristics of devices of $L = 0.12$ and $0.06\,\mu m$ respectively. The characteristics show poor saturation. This may be due to inadequate scaling of the gate oxide. For the $0.12\,\mu m$ device for a gate voltage (V_G) of 3 V, the device is broken down for $V_D = 2.8\,V$. Also a kink is observed for $V_D \sim 1\,V$. The kink is less obvious for larger V_G. For the $0.06\,\mu m$ device, the device has broken down for $V_D > 2.5\,V$ and a kink is observed for $V_D \sim 1\,V$. In this case it is more apparent and is clearly seen for all the V_G shown.

Break down and punch-through can be differentiated by the nature of current-voltage (IV) curves. Punch-through IV is distinguished by transport through a space charge region and is smoother than breakdown IV, which is more abrupt and limited by series resistance.

The kink effect is a consequence of impact ionization [110]. In floating body devices, the holes generated by impact ionization flow towards the source because that is the lowest energy location for them. At any moment, there are a significant number of holes in the body which causes a positive body potential. This reduces the source-channel barrier. Which in turn increases the channel current flow and number of holes generated in impact ionization. This positive feed back is the cause for the kink in

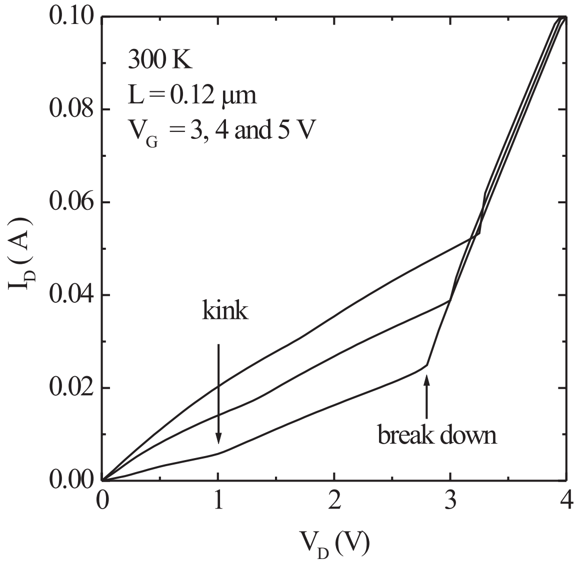


Figure 6.2: I_D vs V_D characteristics of a device of $L = 0.12\,\mu m$. Kink effect is observed for V_D as low as $1\,V$.

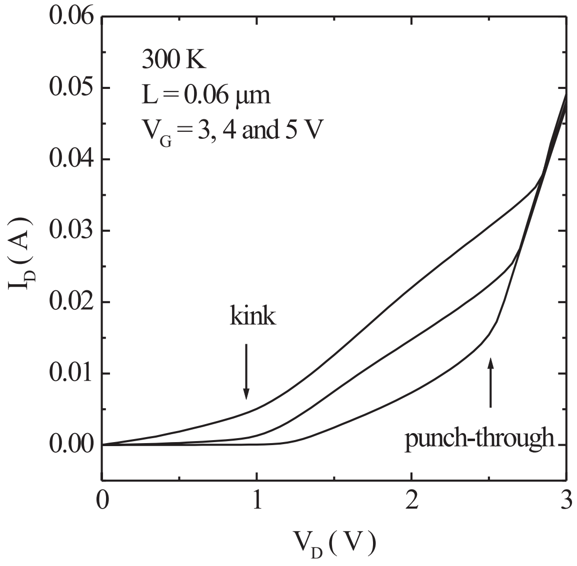


Figure 6.3: I_D vs V_D characteristics of a device of $L = 0.06\,\mu m$. Kink effect is observed for V_D as low as $1\,V$.

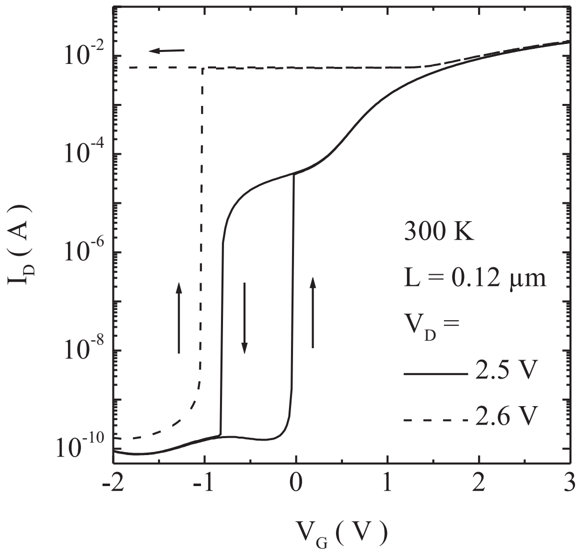


Figure 6.4: Hysteresis observed in the transfer characteristics of devices of $L = 0.12\,\mu m$.

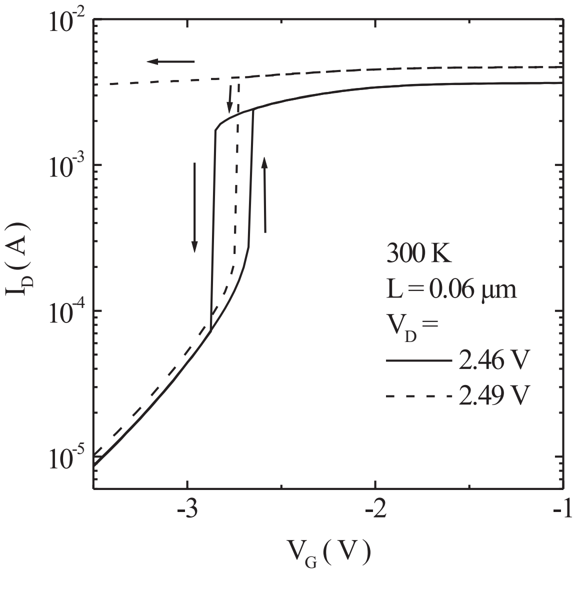


Figure 6.5: Hysteresis observed in the transfer characteristics of devices of $L = 0.06\,\mu m$.

the output characteristics of the devices. The impact of kink effect on performance depends on circuit. In analog circuits, kink effect is undesirable because it makes the device characteristics highly nonlinear. In digital circuits, the kink effect improves the current drive.

The point of interest to us is that the kink is observed for sub bandgap V_D. According to the international technology roadmap for semiconductors, operating voltage of devices with $L = 0.05\,\mu m$ is 0.9 to 1.2 V. This means that sub bandgap kink effect is an important device operational issue for floating body devices belonging to advanced generations.

As V_D is increased further, impact generated holes increase in number. The body potential can be sufficiently high to forward bias the source-body junction, which turns on the parasitic source-body-drain bipolar transistor. This leads to hysteresis in the transfer characteristics of the devices. This situation is illustrated in figures 6.4 and 6.5 for the 0.12 and 0.06 μm devices respectively. V_G was swept from very low values to high values. During the sweep, the drain current (I_D) increases abruptly, marking the turning on of the source-body diode. When V_G is swept in the reverse direction, the device does not turn off at the same V_G at which it turned on during the forward sweep. As V_D is increased further, the turn off voltage of the device becomes highly negative. In a circuit, this has serious implications for the transient handling capabilities of the floating body devices. For example, an output driver in an integrated circuit, which drives an inductive load, may have to handle $2 \times V_D$ during switching.

6.1.3 Gate Current

The interface of MOS devices can be damaged by hot-carriers having energy more than 3 eV [4, 79]. Since the $Si - SiO_2$ barrier is 3.1 eV, such high energy carriers may cause a gate current if the field distributions are favorable. The matching values of the degradation threshold and barrier height make I_G a suitable monitor for hot-carrier degradation.

Figures 6.6 and 6.7 show the results of direct I_G measurements on vertical devices of $L = 0.12$ and $0.06\,\mu m$ respectively. The bell shaped curves are signature of I_G caused by hot-electron injection [10]. For the $0.12\,\mu m$ device, we observe I_G for V_D down to 2.5 V. For the $0.06\,\mu m$ device, I_G is observed even for a V_D of 2.2 V. Both values are much smaller than the barrier height.

6.1.4 Summary

In this section we have illustrated floating body effects in vertical MOSFETs for sub bandgap V_D. We have also seen significant I_G for sub barrier V_D. These results point to the importance of understanding the hot-carrier physics at low voltages.

6.2 Sub-Barrier Hot-Carrier Degradation in Lateral nMOSFET

Hot-Carrier degradation in deep-sub-micron lateral n-channel MOSFETs with gate oxide thicknesses of 3 and 5 nm for V_D nominally below the $Si - SiO_2$ barrier height is

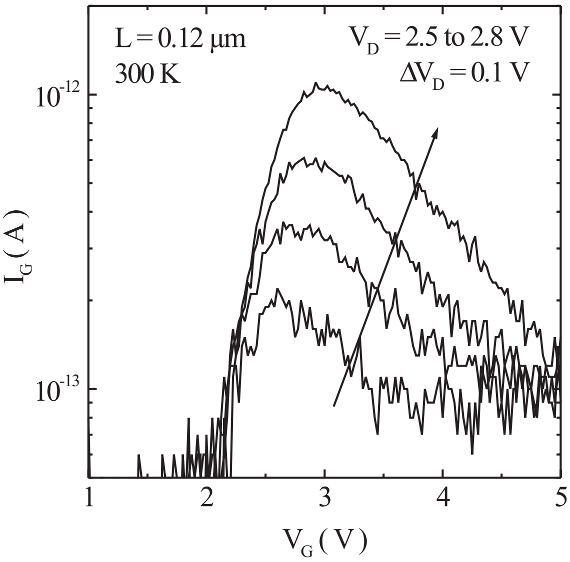


Figure 6.6: Directly measured I_G of vertical device of $L = 0.12\,\mu m$. Bell shaped curves are observed for sub barrier V_D.

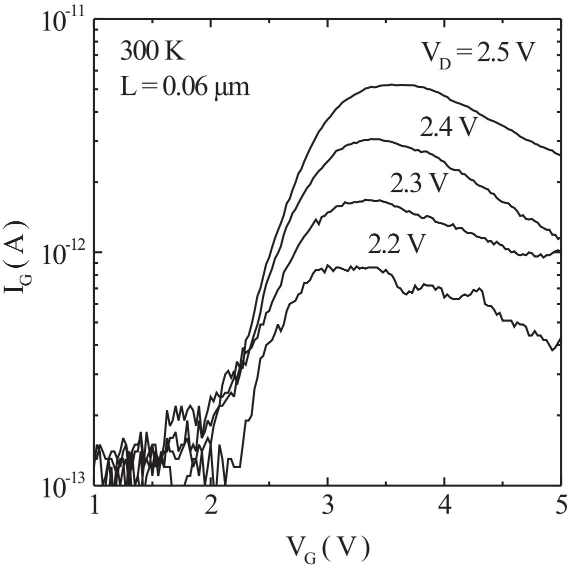


Figure 6.7: Directly measured I_G of vertical device of $L = 0.06\,\mu m$. Bell shaped curves are observed for sub barrier V_D.

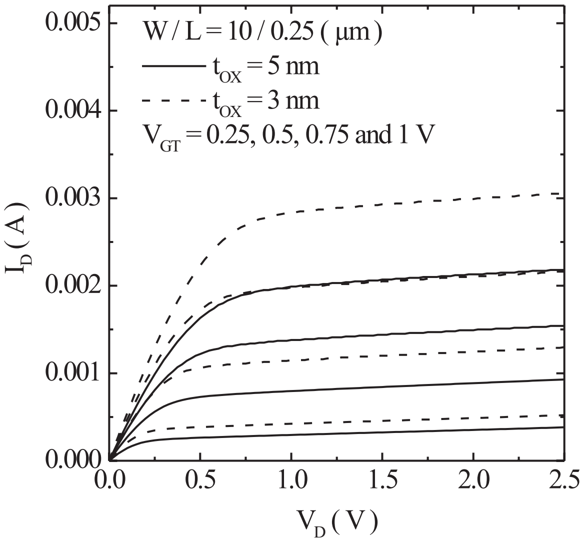


Figure 6.8: $I_D - V_D$ characteristics for $0.25\,\mu m$ channel length devices with t_{OX} of 5 and 3 nm used in this study for various $V_G - V_T$.

presented in this section. The worst case degradation bias condition was studied and was found to be different from those used in the literature.

6.2.1 Devices

In this study we use n-channel MOSFETs fabricated using an industry standard $0.25\,\mu m$ twin-well technology [111]. Gate oxides of thickness 5 and 3 nm were thermally grown at $800^o\,C$. The devices used in this study have a drawn channel length of $0.25\,\mu m$.

Output characteristics of the devices at 300 K are shown in figure 6.8. V_T of the devices were 0.24 and 0.37 V for gate oxide thickness of 3 and 5 nm respectively. The devices show excellent characteristics. Current drive increases with down scaling of the gate oxide as expected.

6.2.2 I_{SUB} vs V_G Characteristics

Substrate current (I_{SUB}) was measured as a function of gate voltage (V_G) for the devices for V_D ranging from 0.8 to 2.55V. Bell shaped $I_{SUB} - V_G$ plots for the $t_{OX} = 3\,nm$ case is shown in figure 6.9 for V_D down to 0.825 V. Similar data were also obtained for devices with 5 nm gate oxide. The issue of sub bandgap impact ionization was dealt with in detail in chapters 4 and 5.

V_G at which I_{SUB} peaks (V_{Gpeak}) is plotted in figure 6.10 as a function of V_D. $V_{Gpeak} - V_T$ is also plotted. V_{Gpeak} is found to decrease as t_{OX} is reduced. The reduction in V_{Gpeak} is proportional to the difference in threshold voltage (V_T). V_{Gpeak} vs V_D can be fitted with the following relation in the high V_D regime.

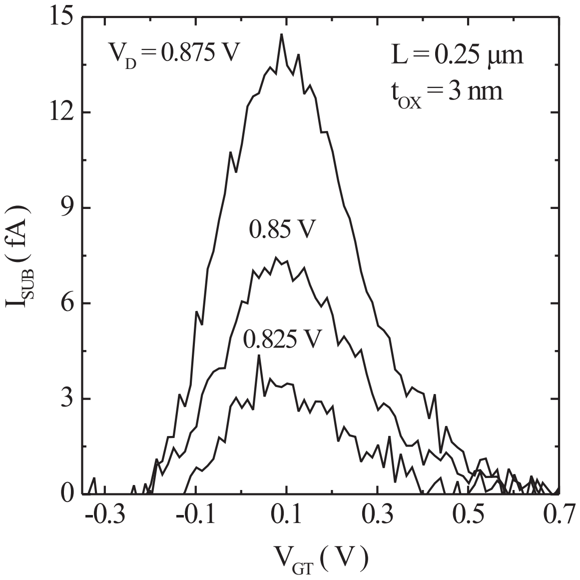


Figure 6.9: Bell shaped I_{SUB} vs V_G characteristic measured for V_D well below the bandgap voltage of silicon.

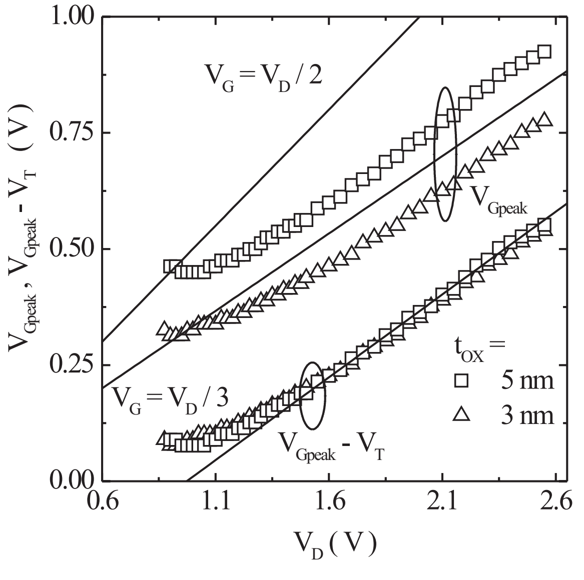


Figure 6.10: V_{Gpeak} as a function of V_D. As the t_{OX} is scaled down, the V_{Gpeak} also decreases, the reduction being proportional to the reduction in V_T. At low V_D, the V_{Gpeak} shows a non-linear behavior.

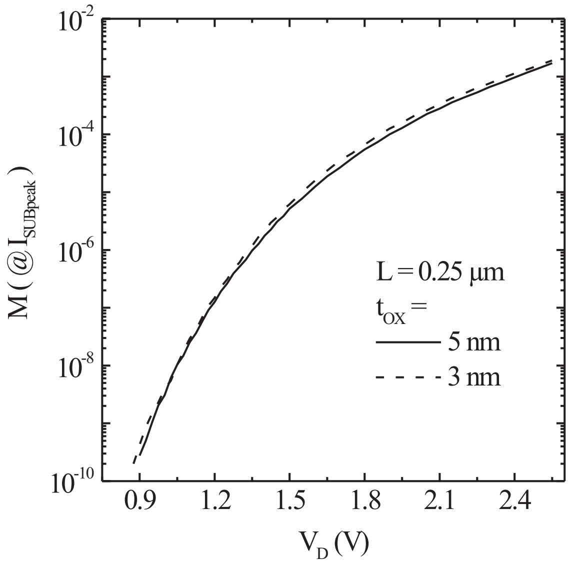


Figure 6.11: Measured quantum yield vs V_D corresponding to $I_{SUBpeak}$ bias condition.

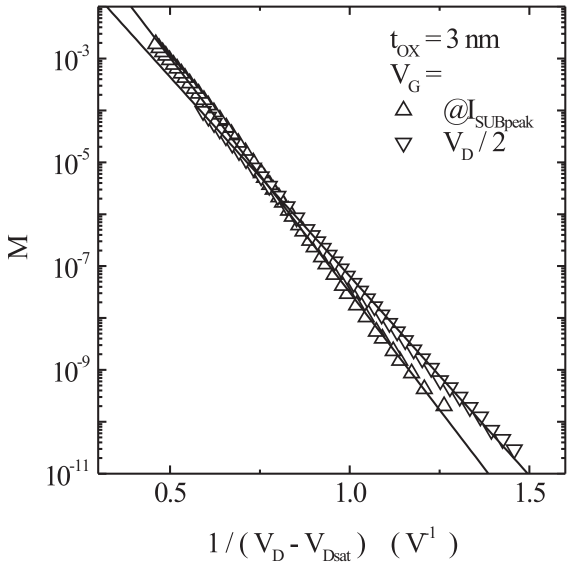


Figure 6.12: Lucky electron model fit of the measured M data at $I_{SUBpeak}$ bias and $V_G = V_D/2$ for a device with gate oxide thickness of 3 nm.

$$V_{Gpeak} = \frac{V_D - 1}{3} + V_T \tag{6.1}$$

The figure also shows $V_{Gpeak} = V_D/2$ and $V_{Gpeak} = V_D/3$ lines. For both the t_{OX} values, V_{Gpeak} is much smaller than $V_D/2$, the bias condition assumed as the worst case degradation condition in many hot-carrier reliability studies, for example [55, 79, 80, 85].

For very low V_D, V_{Gpeak} deviates from the linear behavior observed at high V_D. This is similar to the trends observed for devices studied in chapters 4 and 5 and strengthen the status of those observations as technology independent.

Figure 6.11 shows quantum yield (M) corresponding to the peak substrate current ($I_{SUBpeak}$) condition for the two oxide thicknesses. M for the 3 nm case is higher than for the 5 nm case. This is in contrast to the generally held view that I_{SUB} and hence M decreases with decreasing gate oxide thickness [112, 113].

It is reported that hot-carrier life time extrapolation schemes based on lucky electron model (LEM) [4] can be applied to predict reliability at sub-barrier voltages [79]. LEM predicts an exponential V_D dependence of both I_{SUB} and I_G.

$$\ln M \propto \frac{1}{V_D - V_{Dsat}} \tag{6.2}$$

where V_{Dsat} is the saturation drain voltage and is expressed in many forms in literature. We employ the form given in [4], which is

$$V_{Dsat} = \frac{V_{GT} \,.\, L \,.\, E_{sat}}{V_{GT} + L \,.\, E_{sat}} \tag{6.3}$$

where E_{sat} is the critical field for velocity saturation and is approximately 5×10^4 V/cm.

We have seen in chapter 4 that, even though the tail of the EED becomes important for $V_D < 1.6\,V$ for I_{SUB}, an exponential behavior is still shown by M vs V_D. This is consistent with the fact that mechanisms like EEI merely redistribute the energy gained from the field. The case is similar for gate injection. LEM predicts a maximum energy of qV_D for the electrons. Even though this is wrong, the energy of any electron in the tail has ultimately come from field heating.

Since the peak substrate bias condition deviates significantly from the widely used worst case degradation condition, $V_G = V_D/2$, it is of interest to know whether the data for both conditions can be fitted with LEM. Figure 6.12 shows the measured M plotted against the right hand side of equation 6.2. The symbols show the measured data and the lines show linear fits to the data. The data fit fairly well to the model for V_D down to $0.85\,V$ for both the bias conditions. This suggests that either bias conditions can be used for hot-carrier reliability prediction.

6.2.3 Hot-Carrier Stress Experiments

There are conflicting reports of the worst case degradation stress bias conditions, especially at low V_D. For example, Mahapatra et al. [60] have used $V_G = V_D/2$ as the

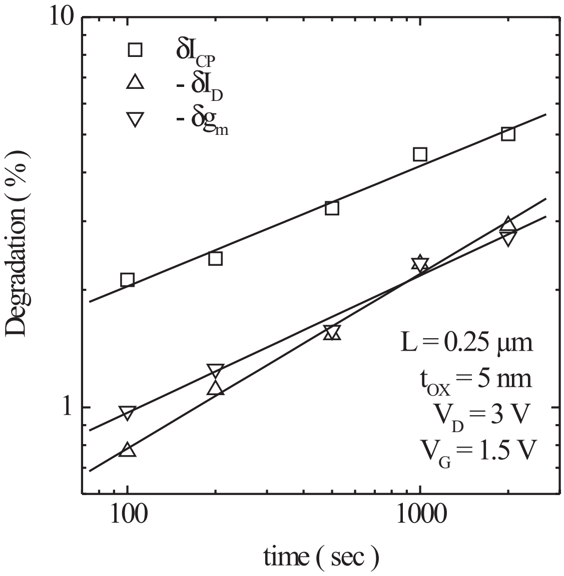


Figure 6.13: Interface degradation monitored using increase in charge pumping current and, degradation in I_D and transconductance for a stress V_D below the barrier height. I_D and transconductance degradations show identical temporal evolution as the charge pumping current.

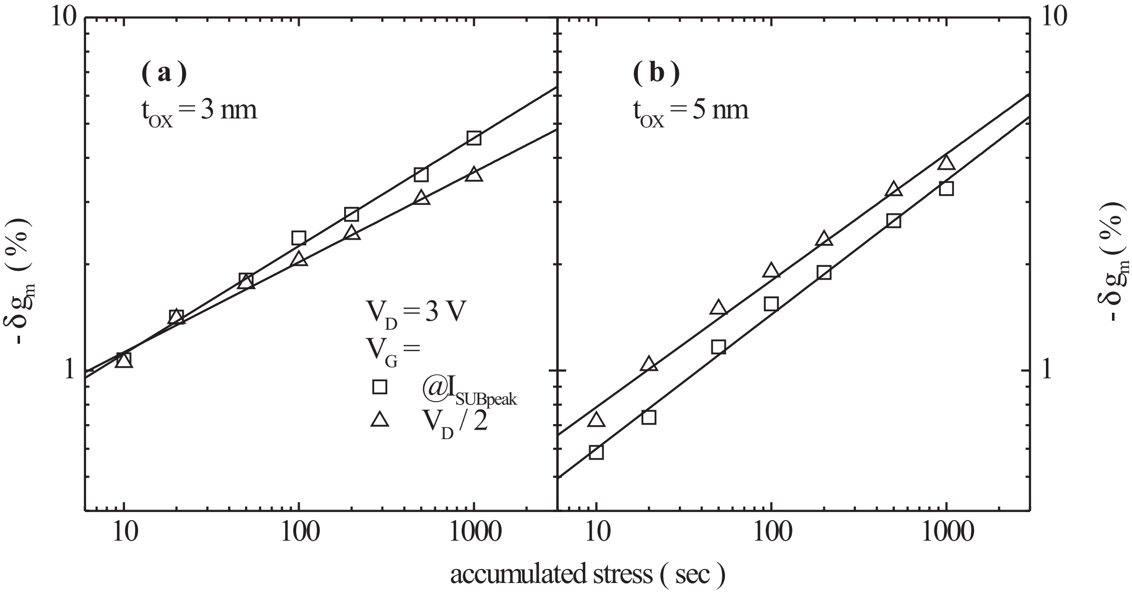


Figure 6.14: Temporal evolution of the degradation for various stress bias conditions. (a) for $t_{OX} = 3\,nm$ and (b) for $t_{OX} = 5\,nm$.

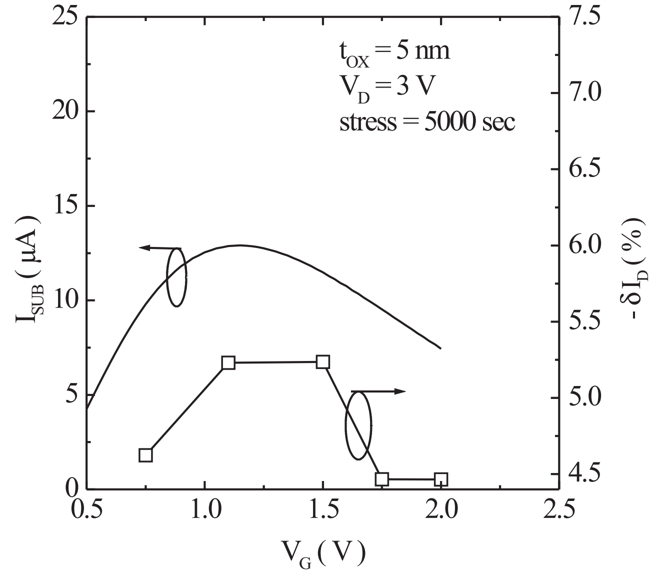


Figure 6.15: V_G dependence of I_D degradation for devices with 5 nm gate oxide. I_{SUB} is also shown for comparison.

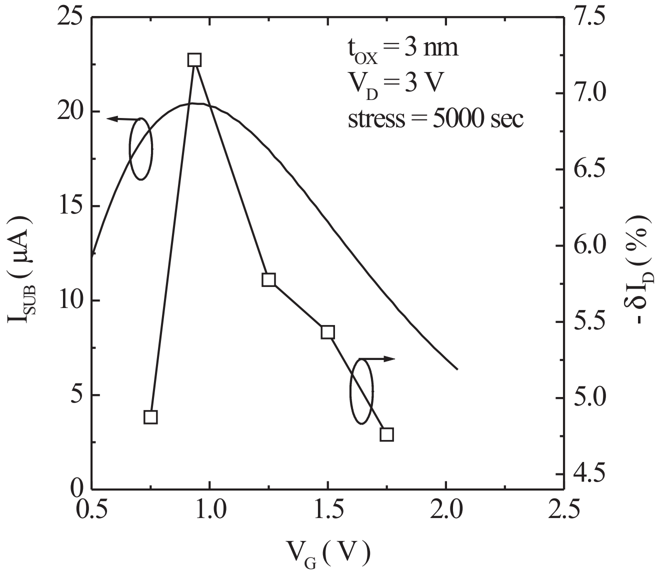


Figure 6.16: V_G dependence of I_D degradation for devices with 3 nm gate oxide. I_{SUB} is also shown for comparison.

worst case degradation bias for dielectrics of equivalent oxide thicknesses of 3.1 to 3.9 nm. Rauch et al. [59] reported that the degradation increases as the stress gate voltage was increased and attributed this to the presence of EEI. Since the devices are usually designed and tested for worst case conditions to ensure that hot-carrier degradation is not the limiting factor for device reliability, it is important to determine the worst case degradation condition itself.

The devices were stressed at $V_D = 3\,V$, which is nominally below the $Si - SO_2$ conduction band barrier. We observed significant device degradation. We also establish the worst case degradation condition for the devices investigated. Charge pumping current (I_{CP}), transconductance (g_m) and I_D are used as degradation monitors. Degradation is monitored by observing the percentage degradation in the parameter that is being monitored. If P is the parameter being monitored, percentage degradation is defined as

$$\delta P = \frac{P - P_v}{P_v} \times 100 \tag{6.4}$$

where, P_v is the value of the parameter for the virgin device. P can be I_{CP}, g_m or I_D.

Charge pumping technique [114, 115] is used to ensure that the degradation is indeed due to interface damage. A brief outline of the charge pumping technique to investigate interface states is given in appendix C. We have employed trapezoidal waveforms of frequency 1 MHz and rise and fall times of 250 nano seconds for charge pumping.

Figure 6.13 shows the temporal evolution of I_{CP} and degradation in g_m and I_D in the linear regime for a device with 5 nm gate oxide. The device was stressed at $V_D = 3\,V$ and $V_G = V_D/2$. An increase in I_{CP} is observed. Degradation in transconductance and I_D follows identical trends as I_{CP}. This ensures that the degradation is due to increase in the interface state density. There is significant degradation for sub-barrier V_D. Since we have established interface degradation as the cause, for further investigations we employ g_m and I_D as degradation monitors.

Figure 6.14 shows the temporal evolution of degradation of g_m for two bias conditions for devices with gate oxide thicknesses of 3 and 5 nm. The two bias conditions used were $I_{SUBpeak}$ and $V_G = V_D/2$. For the 3 nm case the peak substrate bias condition causes more damage than the other condition, whereas for the 5 nm case, the $V_G = V_D/2$ causes greater damage.

A more detailed V_G dependence study was conducted and the results are shown in figures 6.15 and 6.16 for the 5 and 3 nm cases respectively. The devices were stressed at $V_D = 3\,V$ for 5000 seconds at various V_G. The left vertical-axis shows I_{SUB} of the virgin device whereas the right vertical-axis shows the percentage degradation in I_D. The degradation plot roughly follows the I_{SUB} vs V_G plot. However the worst case degradation condition for the 5 nm case is $V_G = V_D/2$.

In summary, we have shown significant interface degradation for sub-barrier V_D. However the worst case degradation condition shows a gate oxide thickness dependence. The widely used $V_G = V_D/2$ stress condition does not reflect the peak I_{SUB} condition in all the cases and it is also not the worst case degradation condition for the devices with 3 nm gate oxide investigated. In contrast to the reports of Rauch et al. [59], degradation

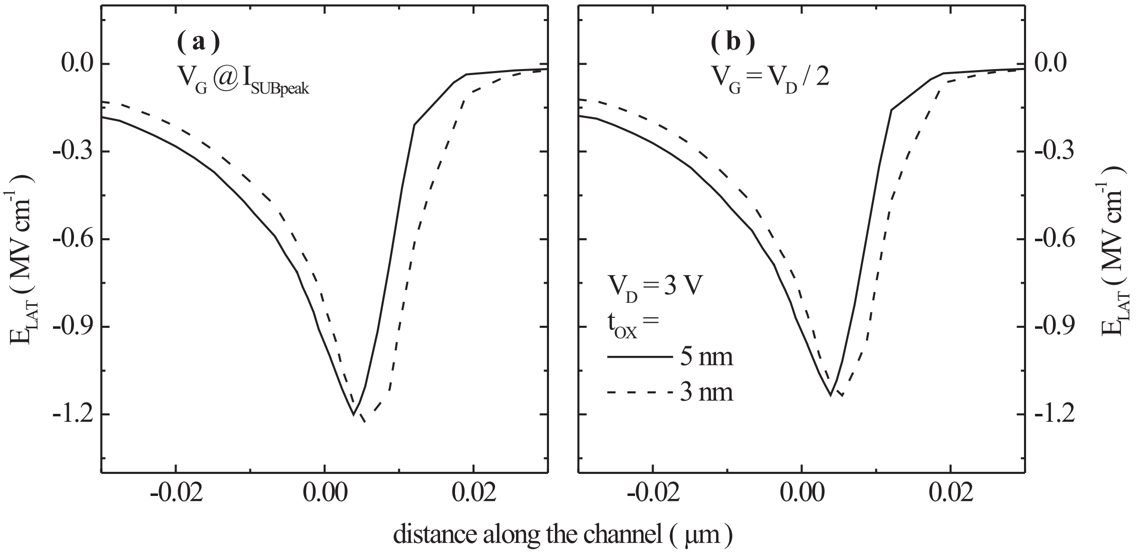


Figure 6.17: E_{LAT} distributions at the drain end of the channel for the stress bias conditions investigated.

does not increase as the gate voltage is raised. Even though EEI play an important role in populating the EED beyond qV_D, and hence important for the analysis of low voltage degradation, its impact can not increase indefinitely with increase in V_G as was amply demonstrated in chapter 4.

6.2.4 Simulations and Discussions

The variations in the worst case stress conditions were further investigated using two dimensional drift-diffusion simulations. MINIMOS 6 was employed for this purpose. The results are presented below.

Figure 6.17 shows the lateral electric field (E_{LAT}) distribution along the channel direction. The drain junction is taken as the reference. Simulations were done for $V_D = 3\,V$ and, $V_G = V_D/2$ and $V_G@I_{SUBpeak}$ bias conditions. Contrary to expectations we do not find any significant oxide thickness dependence of the peak lateral electric field ($E_{LATpeak}$). The field is marginally higher for the 3 nm case. The higher M observed for the 3 nm case may be due to two reasons : (i) the gate oxidation time for 3 nm is smaller than for the 5 nm case and hence the former result in sharper doping profiles (ii) electron-electron interactions (EEI) are stronger for the thinner oxide case due to the larger density of electrons in the inversion layer.

There seems to be a concensus in the literature that the interface damage is caused by energetic electrons destabilizing the chemical bonds at the interface [4, 55, 57, 79]. If the literature values for the minimum energy that an electron should have to cause damage, 3 to 3.5 eV, are true, the damage is caused by electrons in the tail of the EED for $V_D \leq 3\,V$. The damage is then more severe for structures and bias conditions for which the EEI are enhanced. Our results point out that E_{LAT} does not provide the correct information for comparing the effect of oxide thickness scaling on sub-barrier hot-carrier damage.

6.3 Conclusions

In this chapter we have presented results that illustrate the impact of hot-carrier effects on device characteristics and reliability for V_D smaller than the respective thresholds.

Floating body effects are exhibited by vertical nMOSFETs for $qV_D < W_G$. Significant I_G were also observed for V_D down to 2.2 V, much below the $Si - SiO_2$ barrier for electrons, which is 3.1 eV. These results stress the importance of investigating the physics of hot-carriers with energy beyond the applied bias.

We have also presented experimental results on sub bandgap impact ionization and sub barrier interface degradation in lateral devices fabricated using an industry process technology. I_{SUB} were measured for V_D down to 0.825 V. V_{Gpeak} vs V_D showed a nonlinear trend and further support the observations presented in chapters 4 and 5. The peak substrate bias condition is found to depend strongly on oxide thickness for the range from 3 to 5 nm. The 3 nm device showed a higher impact ionization M than the 5 nm device.

Significant hot-carrier degradation was observed for stress V_D marginally lower than the $Si - SiO_2$ barrier. We found that V_G dependence of degradation followed the I_{SUB} vs V_G curve for the devices with gate oxide thickness of 3 nm whereas for 5 nm gate oxide devices the peak degradation was for $V_G = V_D/2$. Two dimensional drift-diffusion simulations did not provide any explanations to this change. Since the tail of EED is responsible for the degradation for sub barrier V_D, ensemble Monte-Carlo simulations may be required to explain the observations. However, a blind choice of $V_G = V_D/2$ as the stress bias may not reflect the worst case degradation condition for oxide thickness range of 3 to 5 nm, and may overestimate the hot-carrier life time.

Chapter 7

Conclusions and Outlook

In this work we have presented a detailed experimental investigation of hot-carrier effects like impact ionization, gate injection and interface degradation near and below their respective threshold voltages. Investigations were carried out in n-channel, conventional (CON) and laterally asymmetrical channel (LAC) MOSFETs and vertical MOSFETs. Samples prepared in academic and industry fabrication facilities were used.

First we presented experimental findings on temperature dependence of impact ionization in conventional MOSFETs. Substrate current (I_{SUB}) was found to be independent of temperature for drain voltage (V_D) around 2 V. This V_D is known as the cross-over voltage (V_{XOVER}). For $V_D > V_{XOVER}$, I_{SUB} showed a negative temperature dependence and for $V_D < V_{XOVER}$, it showed a positive temperature dependence. We found that V_{XOVER} increases, with gate overdrive (V_{GT}) for a given channel length (L), and with channel length for a given V_{GT}. These results were interpreted assuming that the cross-over is caused by an increase in threshold energy for impact ionization, which is equal to bandgap energy (W_G) in the case of silicon. A graphical method of analysis was derived based on Monte-Carlo (MC) simulation results found in the literature. According to this model, cross-over happens when an enhancement of carrier heating due to reduced phonon scattering at low temperature is compensated by the suppression of impact ionization due to a higher W_G. V_{GT} and L dependencies of V_{XOVER} were found to be due to decreasing population of the electron distribution (EED) beyond W_G due to the reduction of effective temperature (T_E) of carriers. Since increasing V_{GT} and decreasing L result in reduction of field heating of the carriers, we could establish a qualitative relation between the peak lateral field, effective temperature and EED.

Next we investigated impact ionization in conventional devices of channel lengths from 0.16 to 5 μm for qV_D near and below W_G. Bell shaped I_{SUB} vs gate voltage (V_G) characteristics were measured for V_D of 0.65 V at 300 K and 0.8 V at 77 K. We observed an anomalous double peak in I_{SUB} vs V_G plots at 77 K. We also observed that V_G corresponding to the peak substrate current (V_{Gpeak}) showed an anomalous turn around. As V_D was reduced from high values, V_{Gpeak} first decreased and then increased again in the low V_D range. This turn around was observed both at 300 and 77 K and it was found to enhance with reduction in channel length and temperature. A detailed channel length dependence study proved that both the double peaked I_{SUB} vs V_G and the turn around in V_{Gpeak} are expressions of the same phenomenon.

A free electron drifting in a potential drop of V_D can gain a maximum energy of qV_D. In such a case there should not be any impact ionization for $qV_D < W_G$. However MC simulations have predicted that electron-phonon and electron-electron interactions might populate the EED beyond qV_D. A thorough analysis of the temperature dependence of I_{SUB} and the quantum yield ($M = I_{SUB}/I_D$) was performed to provide experimental proof for the presence of a lattice temperature dependent tail (LTDT) and its broadening due to short range electron-electron interactions (SREEI). The nature of the tail of EED was also verified. LTDT strongly support the presence of a thermal tail in the EED which result from electron-phonon interactions (EPI). Our data also suggest that SREEI, though depends on electron density, is not effective in populating the high energy tail of the EED for large V_G. This is because, the energy redistributed through SREEI is essentially gained from the field and the peak lateral field decreases with increasing V_G. Since the field is also decreasing with increasing V_G, SREEI was also found to be weaker for longer channel length devices.

Based on one-dimensional consistent Poisson-Schrödinger simulations of an MOS system that resemble the channel of the devices experimentally studied, we have proposed a role for inversion layer quantization in impact ionization at very low voltages. It is well known that the electrons entering the channel from the source have energy higher than the bottom of the conduction band in the source. This is because in MOSFETs, the drain current is limited by how much of carriers are supported in the inversion layer by the gate and not by source injection. This is reflected as a small barrier between source and the channel even in strong inversion. We have found that the inversion layer quantization increases this barrier by about 40 meV. This was found to increase with gate bias and can be a significant contribution to impact ionization for qV_D near and below W_G.

Impact ionization at low V_D was further investigated in n-channel LAC devices. These devices have a graded doping profile along the channel direction. Investigations were conducted for both directions of operation. In the forward mode, peak of the channel doping was at the source end of the channel and in the reverse mode, it was at the drain end. For the forward mode of operation we have observed two peaks in I_{SUB} vs V_G at 300 K and three peaks at 77 K. A detailed investigation of V_{Gpeak} vs V_D behavior indicated that the second peak observed at 77 K is hidden in the 300 K data as a reversal in V_{Gpeak}. For the reverse mode of operation, even though only one peak was observed, a reversal in V_{Gpeak} vs V_D was observed at 300 and 77 K.

Two-dimensional drift-diffusion analysis showed the presence of two peaks in lateral electric field distributions for the forward mode of operation. One peak near the drain junction and another near the source junction. Temperature, channel length and gate bias dependence of the peaks in E_{LAT} were compared with the trends exhibited by the first and third peaks in I_{SUB} vs V_G. We have established that the first peak in I_{SUB} vs V_G correspond to the high field region near drain and the second peak correspond to the high field region near source.

Comparison of V_{Gpeak} vs V_D data for CON and LAC operated in the forward and reverse modes of operation suggested that the second peak or its manifestations are due to SREEI in the drain side high field region.

Comparison of CON and LAC operated in the forward mode also showed that I_{SUB} in the later case exceeds that in the former for large V_G values. This suggest that, contrary to expectations, LAC may have poor hot-carrier reliability than CON for certain bias conditions.

For LAC operated in the forward mode, source electrons are injected directly into a high field region. In such a case, source EED can have a profound impact on the hot-carrier effects in the source side high field region. The data presented, when further investigated in combination with an MC simulator incorporating appropriate models, may be able to confirm the role of long-range electron-electron interactions (LREEI) on source EED predicted by some of the MC simulation groups.

We have also presented hot-carrier effects in vertical transistors at low voltages. Kink effects were observed for $qV_D < W_G$. Gate injection for $V_D = 2.2\,V$, which is much smaller than the $Si - SiO_2$ barrier, was also demonstrated.

We have measured significant interface degradation for $V_D = 3\,V$ in conventional devices with gate oxide thicknesses of 3 and 5 nm. It was found that the bias conditions for worst case degradation depends strongly on the thickness of the gate oxide. Even though SREEI may be playing a role in degradation at such low V_D, degradation was found not to increase indefinitely with increasing V_G as was reported by some groups. The earlier stated result, that SREEI is less efficient in populating the high energy tail of the EED for large V_G support this observation.

Interpretations presented in this thesis were qualitative in nature. More rigorous quantitative information can be obtained by numerically solving transport equations with appropriate models for SREEI, LREEI, EPI and inversion layer quantization. An obvious approach is using MC tools incorporating these models.

To conclude, hot-carrier effects will be present even in advanced CMOS technologies in which supply voltages are scaled below the threshold voltages for the related physical phenomena. An illustrative example is in order. For devices belonging to the 50 nm or lower channel length generations, supply voltage is about 0.6 V or higher. Significant ballistic transport can be present in such devices. That means, a significant number of the electrons have energy equal to 0.6 eV. If we account for SREEI, a first order interaction can lead to a significant number of electrons with energy equal to 1.2 eV or higher. Higher order interactions can lead to the presence of electrons with energy that are integral multiples of qV_D. In this scenario the advent of high relative permittivity dielectrics which have lower silicon to dielectric conduction band discontinuity, may have serious implications for hot-carrier effects in such futuristic devices.

Appendix A

Process Technology for CONventional and LAC MOSFETs

Process flow for the devices used in chapters 3, 4 and 5 are given below.

The process was done on p-type $< 100 >$ oriented wafers of resistivity $10-20\ \Omega cm$.

1. Pad oxide, dry O_2 at 950^oC, 25 nm + and nitride deposition NH_3+ DC sputtering at 785^oC, 100 nm
2. Active area definition, lithography + Nitride etch (RIE)
3. LOCOS isolation, wet oxidation
4. Threshold implant, lithography and ion implant **(CONventional devices)** BF_2^+
5. Gate oxidation, dry O_2 at $800^oC + N_2$ anneal at 800^oC, 3.6 nm thick oxide.
6. Poly deposition (LPCVD) $SiH_4 + H_2$ at 620^oC, 200 nm
7. Gate definition, e-beam lithography
8. Poly etch, $HBr + Cl_2$ (RIE)
9. Threshold implant, large angle tilt implant from source side **(asymmetric devices)** Boron, tilt angle, $\beta = 10^o$
10. S/D extension implant, As, 10 keV, $4 \times 10^{14} cm^{-2}$
11. LTO deposition, $SiH_4 + O_2$ at 400^oC, 100 nm
12. Oxide spacer, $CHF_3 + O_2$ plasma (RIE)
13. Deep S/D + poly implant As, 40 keV, $5 \times 10^{15} cm^{-2}$
14. S/D/gate anneal, RTA, 1020^oC, 15 seconds
15. Silicidation, Ti deposition + two step RTA anneal
16. Contact hole, 500 nm LTO deposition + lithography + LTO etch
17. Metalization, $0.5 \mu m$ Al + lithography + plasma etch

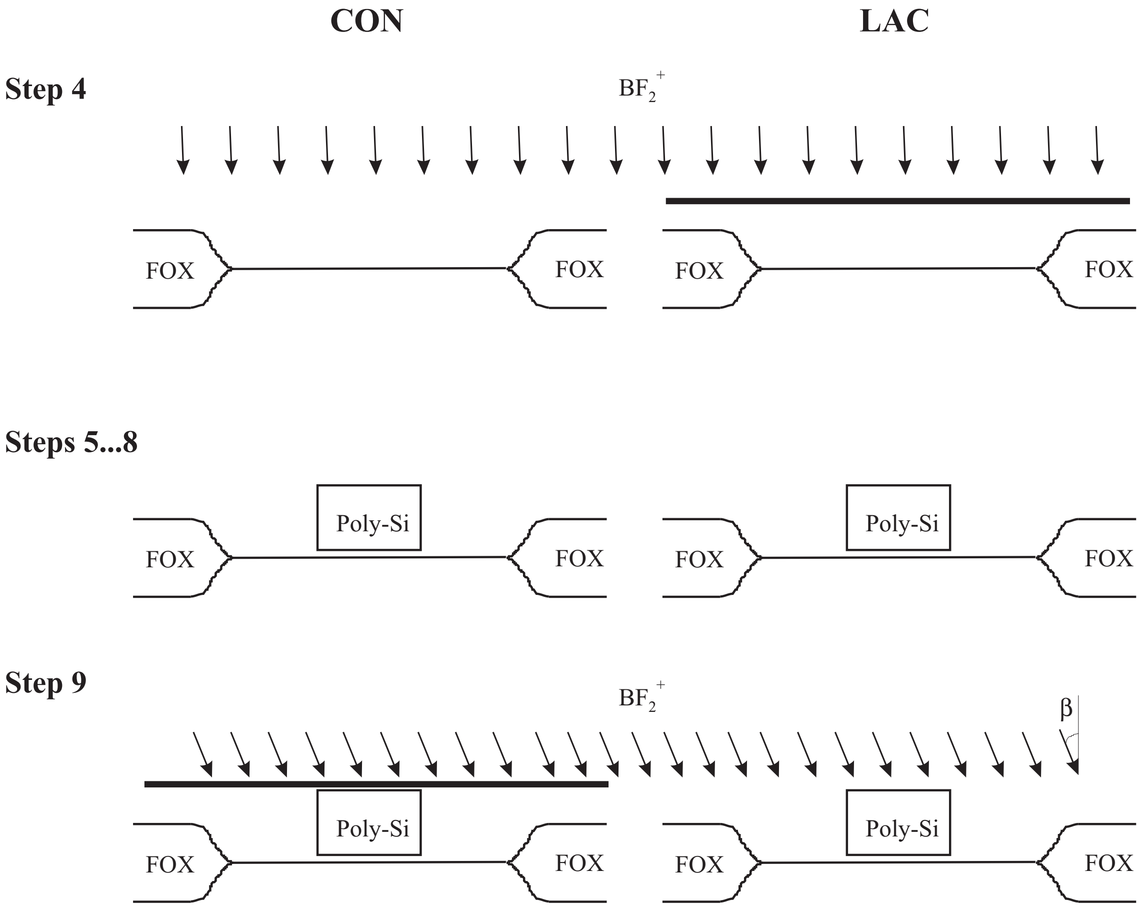


Figure A.1: Critical steps in the fabrication of CON and LAC devices. For LAC, the threshold adjust implant is done after poly gate definition at a tilt angle of β from the source side. For the devices used in the present study, $\beta = 10^o$.

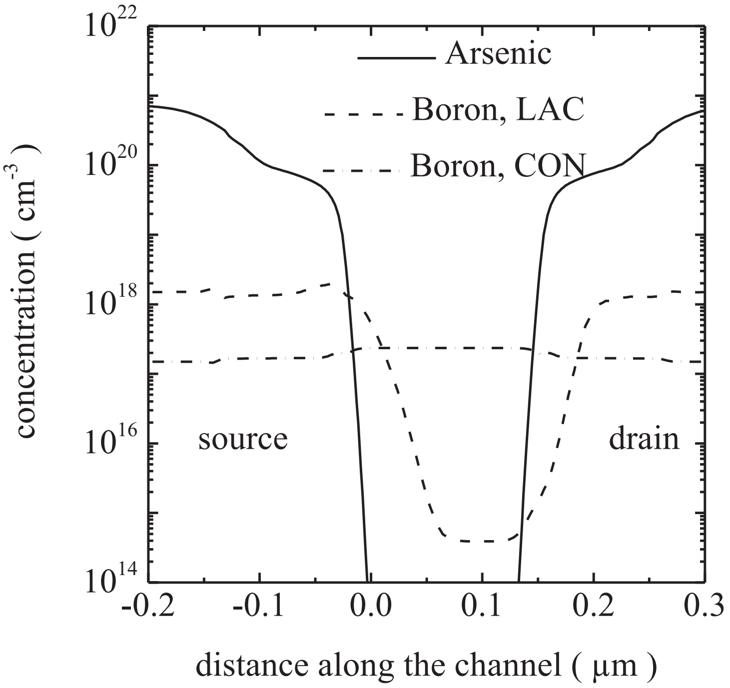


Figure A.2: Simulated doping profile along the channel direction, 1nm below the $Si - SiO_2$ interface for both LAC and CON devices.

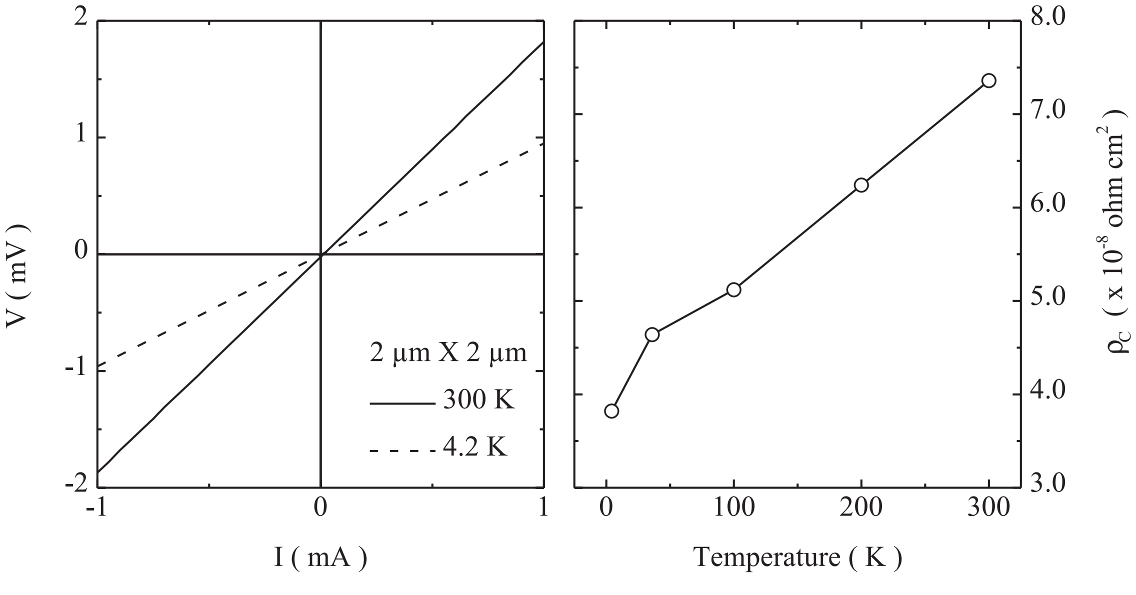


Figure A.3: Measured characteristics of source/drain Kelvin contact structures of area $2\,\mu m \times 2\,\mu m$. (a) IV characteristics (b) specific contact resistance versus temperature for temperature down to 4.2 K.

18. Forming gas anneal, $400^{o}C$

The above stated process flow is taken from [81]. The critical process steps that differentiate the two structures are illustrated in figure A.1.

The nominal oxide thickness for the devices used in chapters 4 and 5 was 3.6 nm. Simulated doping profiles along the channel direction of the two structures are compared in figure A.2.

Two step RTA silicidation process was employed to reduce the contact resistance. Voltage vs current characteristics of 4-terminal Kelvin contact structures of area $2\ \mu m \times 2\ \mu m$ for temperatures down to 4.2 K are shown in figure A.3. The characteristics show excellent linearity and hence low temperature characteristics of the MOSFETs reflect device physics. Extracted specific contact resistance vs temperature is also shown in the figure. The specific contact resistance decreases with temperature as expected for silicon-silicide contacts [116]. The specific contact resistance is below $10^{-7}\,\Omega\,cm^2$, the value specified in the International Technology Roadmap for Semiconductors 2000 update, for the 90 nm technology node [117].

Appendix B

Process Flow and Manufacturability of Vertical MOSFETs

1. Wafer cleaning : modified RCA cleaning
2. MBE growth of the source, channel and drain regions
3. Mesa etching using Reactive Ion Etching (RIE), SF_6
4. Gate oxidation, thermal oxide at $800^o\,C$
5. Poly silicon deposition, $1050^o\,C$, in-situ doped, 200 nm
6. Gate structuring, RIE, SF_6
7. Deposition of passivation layer, LPCVD Si_3N_4, $800^o\,C$, 150 nm
8. Contact hole etching, RIE, CF_4
9. Front side metalization, Titanium 30 nm + AlSi 300 nm
10. Back side etching and metalization

The process flow is cited from [118].

Manufacturability of the devices were investigated using threshold voltage (V_T) as a monitor. Since V_T depends on the oxide thickness, doping profile, parasitic source/drain contact resistances and channel length (for deep-sub-micron devices), variations in V_T reflect the variations in these parameters.

Distribution of the V_T over a 3 inch wafer is shown in figure B.1. The V_T distribution has a standard deviation (σ) of 5% of the mean. 3σ value is then 15%. This value is close to the industry requirement of about 12% for the sub-100 nm gate length technologies [117, 119] and is very good for a university process. Figure B.2 shows the chip-wise distribution of V_T on the same wafer.

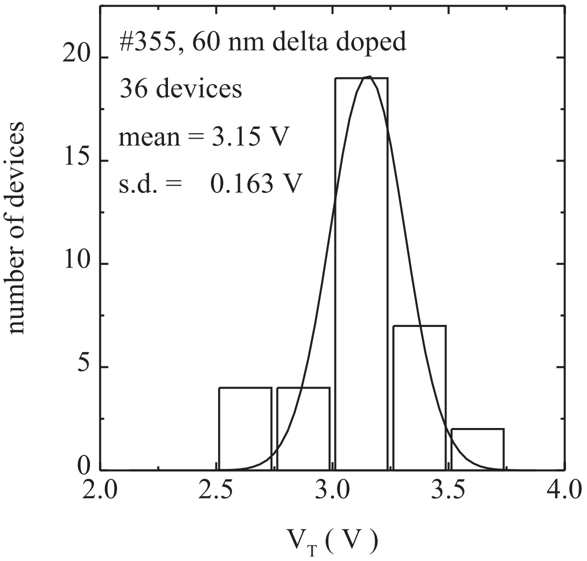


Figure B.1: Threshold voltage distribution over a 3 inch wafer.

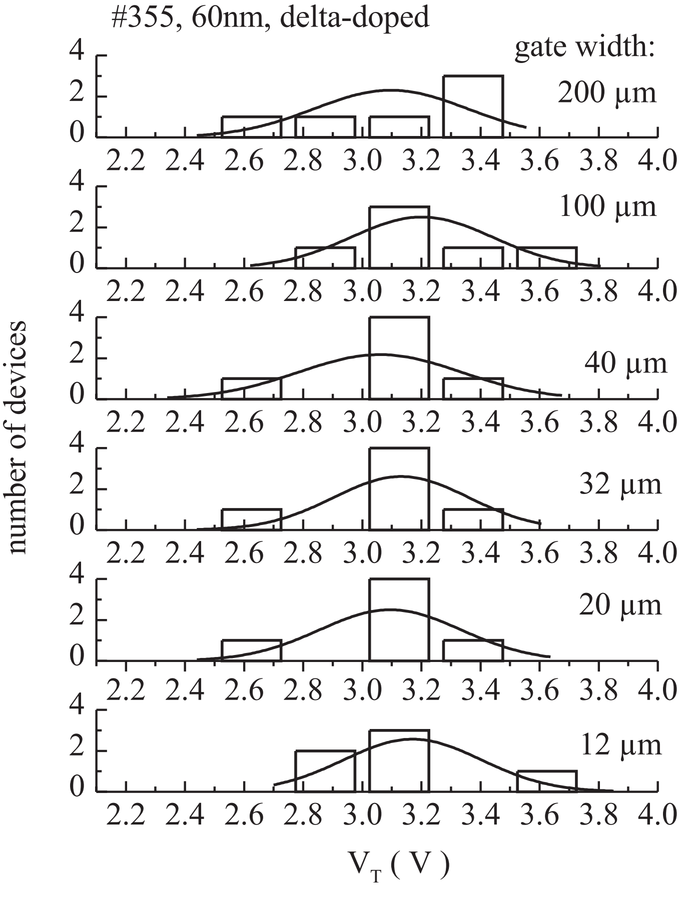


Figure B.2: Threshold voltage distribution on 6 different chips on a single wafer.

Appendix C

Schematics of Electrical Measurement Systems

Schematic of the setup used for sensitive substrate current measurements is shown in figure C.1. HP 4155 parameter analyzer controls and acquires data from Keithley 617 electrometer. Low level measurement sensitivity and accuracy depend, apart from the measuring instruments, on shielding, grounding and wiring [84]. A well shielded probe station was used for the measurements. Substrate terminal was connected to the electrometer using a low noise tri-axial cable.

Charge pumping is a standard technique to investigate interface states in MOSFETs and gated diodes [114, 115]. Schematic of the setup used in the present investigations is shown in figure C.2. The schematic shown is general except for the equipment used. Charge pumping current can be measured either at the substrate terminal or the source and drain terminals. Various modes and bias conditions can be achieved by programming the SMUs. When the source and drain are to be at the same potential, it is advisable to tie them to the same SMU. This is because, two SMUs can have nonzero off-set which leads to parasitic channel currents.

During charge pumping electrons are trapped in the interface states during the positive half of the pulse since the device is in inversion. In the next half of the cycle, the channel is driven to accumulation. The trapped electrons are emitted and recombine with holes from the substrate which leads to a positive substrate current. This charge pumping current is proportional to the interface state density.

In the measurements reported in chapter 6, we have used trapezoidal waveforms of frequency 1 MHz and rise and fall times of 250 nano seconds.

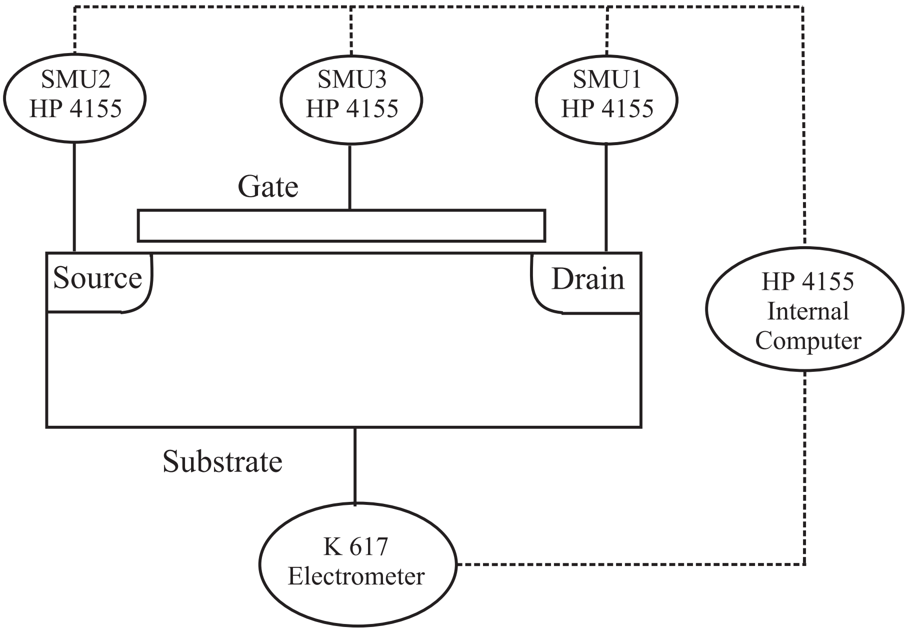


Figure C.1: Setup for measurement of substrate current with femto-ampere measurement resolution. All measurement cables (solid lines) are triax. Source-measure units (SMU) of HP 4155 Parameter Analyzer are configured as voltage source - current measure units.

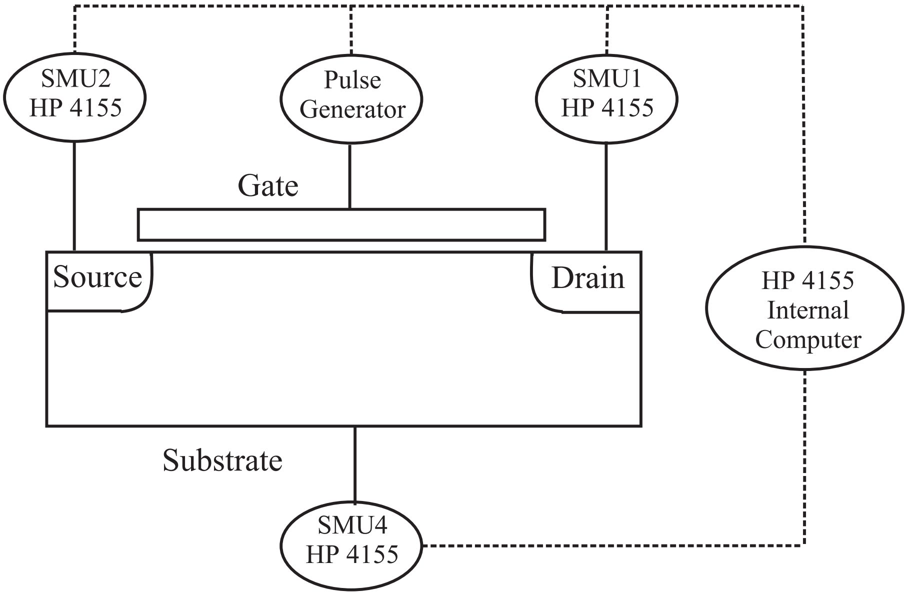


Figure C.2: Setup for charge pumping. Source-measure units (SMU) of HP 4155 Parameter Analyzer are configured as voltage source - current measure units. HP 33120A arbitrary waveform generator was used to generate trapezoidal pulses.

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2. **K. G. Anil**, S. Mahapatra, V. Ramgopal Rao and I. Eisele, "Comparison of Sub- Bandgap Impact Ionization in Deep-Sub-Micron Conventional and Lateral Asymmetrical Channel nMOSFETs", in *Proceedings of the International Conference on Solid State Devices and Materials (SSDM) 2000*, Sendai, Japan, 29-31 August 2000, pp. 60-61. *Japanese Journal of Applied Physics*, vol. 40, Part 1, No. 4B, pp. 2621-2626, April 2001.

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