Pulsed High Current Characterization of Highly Integrated Circuits and Systems

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Erklärung

Ich versichere an Eides statt, dass ich die der Fakultät für Elektrotechnik und Informationstechnik (EIT) der Universität der Bundeswehr München vorgelegte Dissertation mit dem Thema PULSED HIGH CURRENT CHARACTERIZATION OF HIGHLY INTEGRATED CIRCUITS AND SYSTEMS ohne fremde Hilfe erstellt, bei der Abfassung keine anderen als die im Schriftenverzeichnis angeführten Hilfsmittel benutzt und die wissenschaftlichen Leistungen eigenständig erbracht habe. Inhaltliche Bestandteile der Dissertation basieren teilweise auf meinen zuvor veröffentlichten Erstautorpublikationen (List of publications).

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Abstract

The Charged Device Model (CDM) describes the primary cause for Electrostatic Discharge (ESD) failures in manufacturing and automatic handling. The CDM test method is the standardized procedure used worldwide to characterize the susceptibility of a device to damage from ESD under CDM conditions. Prevailing trends in the semiconductor industry like technology scaling towards the deep sub-10-nm regime or the steady increase in data rates in high-speed IOs ($> 50\,\text{Gbps}$) have come at the expense of degraded ESD robustness, entailing new challenges in the field of ESD protection as well as in ESD testing. The resulting demand for improved CDM test precision steadily reveals the limitations of the CDM testing method, which is highly unreliable due to the air discharge. Because of the very poor repeatability of CDM testing, a contact-mode ESD test method called Capacitively Coupled Transmission-Line Pulsing (CC-TLP) was developed, starting two decades ago by Gieser and Wolf, when the risk of false CDM test results was still limited.

This thesis mainly deals with the question if CC-TLP is capable to complement or even replace the commonly used CDM testing method for product development and characterization of challenging package setups and very advanced high-speed technologies today and beyond. Like today's CDM testing, CC-TLP needs to reproduce exactly the failure locations and failure signatures of real world CDM events. Tested devices should fail at about the same peak stress current within the $\pm 20\%$ tolerance of the current CDM standard. This was already demonstrated in several correlation studies between CDM and CC-TLP on technologies up to 90 nm CMOS in the last decades. In view of issues of CDM correlating voltage failure thresholds between compliant CDM testers in many cases, this thesis studies the intrinsic stress factors relating the two test methods. It investigates in detail both test methods and their correlation on following, very advanced technologies, motivated by the fact that there was no simple correlation between the peak currents obtained.

A) A large Chip-on-Flex (COF) assembly with a highly chargeable foil substrate

B) A very small packaged Integrated Circuit (IC) designed in a 0.25 µm BCD technology

C) A 28 nm CMOS IC for network applications with ultra-high-speed (25 Gbps) interface

Challenging the limits of today's metrology and test setups, a characterization and significant improvement of the impulse setup enabled an accurate generation, controlling and monitoring of intrinsic stress parameters like the CC-TLP current rise time or slew rate. In order to reach a current rise time resolution in the single-digit ps-domain, post measurement embedding/de-embedding techniques were implemented. These were essential prerequisites for an exhaustive comparison of both test methods and revealed that the energy content of the pulses and cumulative stress effects (A) as well as the stress current slew rate (B,C) can have a direct influence on the failure threshold. Despite decades of application, there is still a significant lack of understanding about the influences of critical stress parameters beyond the peak current as well as the interaction of the tester and the Device under Test (DUT) including the package, particularly because the investigation of these parameters is not directly addressable by the poorly reproducible CDM test method. Thanks to the single-digit ps-resolution and precision of the highly reproducible CC-TLP test method, which additionally provides wafer-level capabilities and the possibility to control key parameters like the rise time or the pulse width of the stress, this thesis is one of the first to directly analyze the influence of critical stress factors on advanced semiconductor technologies at device and wafer level. Furthermore, this thesis contains not only CC-TLP investigations of CDM typical gate oxide ruptures but, for the first time, a pn-junction failure (A).

The thesis also presents an innovative method for scanning the surface potential across e.g. PCBs or flexible electronics (A), providing specific information for identifying root causes of the electrostatic stress. Circuit simulations support the experiments and provide a deep insight into the general correlation between CDM and CC-TLP with respect to the variation of specific test parameters. The outcome of this work is pushing forward the frontiers of today's ESD testing in the CDM domain and is expected to play a decisive role for future standardization of CDM and alternative stress test methods like CC-TLP.

Zusammenfassung

Das Charged Device Model (CDM) beschreibt eine Hauptursache für Ausfälle durch elektrostatische Entladungen (ESD) in der Fertigung und Handhabung von integrierten Schaltungen (ICs). Um CDM-bedingte ESD-Ereignisse im Labor nachzustellen und so die Empfindlichkeit von Halbleiterbausteinen gegenüber auftretender CDM-Belastung zu charakterisieren, wird weltweit die standardisierte CDM-Prüfmethode eingesetzt. Vorherrschende Trends in der Halbleiterindustrie wie die Skalierung der Strukturgröße bis in den einstelligen nm-Bereich oder die stetige Zunahme der Datenübertragungsraten von High-Speed-IOs ($> 50\,\mathrm{Gbps}$) führen zunehmend zu einer reduzierten ESD-Festigkeit moderner Halbleitertechnologien. Dies stellt die Entwicklung von ESD-Schutzkonzepten sowie die ESD-Prüfmethoden vor neue Herausforderungen. Um diese zu meistern, wird eine höhere CDM-Testgenauigkeit benötigt, welche das gegenwärtige, aufgrund seiner Luftentladung sehr unzuverlässige, CDM-Prüfverfahren nicht bieten kann. Durch die geringe Reproduzierbarkeit des CDM-Tests motiviert, entwickelten Gieser und Wolf vor zwei Jahrzehnten, als das Risiko falscher CDM-Testergebnisse noch begrenzt war, eine kontaktbehaftete ESD-Testmethode namens Capacitively Coupled Transmission-Line Pulsing (CC-TLP).

Die vorliegende Doktorarbeit behandelt hauptsächlich die Frage, ob CC-TLP in der Lage ist, die gängige CDM-Prüfmethode zur Produktentwicklung und Charakterisierung anspruchsvoller Halbleitertechnologien, insbesondere in Bezug auf Gehäusebauformen und heutiger sowie zukünftiger High-Speed-Anwendungen, zu ergänzen oder sogar zu ersetzen. Hierfür sollte CC-TLP, wie das gegenwärtigen CDM-Prüfverfahren, genau die Fehlerorte und Fehlersignaturen von realen CDM-Ereignissen reproduzieren. Getestete Bausteine sollten dabei, innerhalb der Toleranz von $\pm 20\%$ des aktuellen CDM-Standards, bei gleichem Spitzenstrom ausfallen. Dies wurde bereits in den letzten Jahrzehnten in mehreren Korrelationsstudien zwischen CDM und CC-TLP bei CMOS-Technologien oberhalb 90 nm nachgewiesen. In Anbetracht vieler Fälle nicht korrelierender Ausfallschwellen zwischen konformen CDM-Testern, untersucht diese Arbeit die Korrelation zwischen CDM und CC-TLP bezüglich folgender, sehr fortschrittlicher Technologien.

A) Ein großes Chip-on-Flex (COF) Modul mit einem hochaufladbaren Foliensubstrat

B) Eine in 0.25 µm BCD-Technologie gefertigtes IC in einem sehr kleinen Chipgehäuse

C) Ein 28 nm CMOS-IC für Netzwerkanwendungen mit Ultra-High-Speed (25 Gbps) Schnittstelle

Die Motivation für die Untersuchungen war die Tatsache, dass das CDM-Prüfverfahren und CC-TLP bei den getesteten Produkten zu verschiedenen Ausfallschwellen bezüglich des Spitzenstroms führten. Um diese anscheinende Misskorrelation zwischen CDM und CC-TLP aufzulösen, untersucht diese Doktorarbeit wie kumulative Stresseffekte (A) sowie der Energiegehalt oder die Stromanstiegsrate (B,C) der Belastungsimpulse einen direkten Einfluss auf die Ausfallschwelle haben können. Eine wesentliche Voraussetzung dafür war die Charakterisierung und signifikante Verbesserung des CC-TLP-Aufbaus, welcher eine präzise Erzeugung, Steuerung und Überwachung intrinsischer Stressparameter wie der CC-TLP Stromanstiegszeit bzw. Stromanstiegsgeschwindigkeit ermöglicht. Um eine Auflösung der Stromanstiegszeit im einstelligen ps-Wertebereich zu erreichen, war zudem die Integrierung von Embedding- und De-Embedding-Verfahren nötig. Trotz jahrzehntelanger Anwendung des CDM-Prüfverfahrens mangelt es nach wie vor an Wissen über die Einflüsse kritischer Stressparameter jenseits des Spitzenstroms sowie über das Zusammenspiel von Tester und IC. Ein Hauptgrund hierfür ist, dass die Untersuchung dieser Parameter mit der schlecht reproduzierbaren CDM-Prüfmethode nicht direkt möglich ist. Dank der einstelligen ps-Auflösung und Präzision des hochreproduzierbaren CC-TLP-Testverfahrens, welches zusätzlich Tests auf Waferebene ermöglicht und die Möglichkeit bietet, Schlüsselparameter wie die Anstiegszeit oder die Pulsbreite der Spannung zu steuern, ist diese Arbeit eine der ersten, die den Einfluss kritischer Stressfaktoren an fortschrittlichen Halbleitertechnologien auf Baustein- und Waferebene direkt analysiert.

Darüber hinaus enthält diese Arbeit nicht nur CC-TLP-Untersuchungen von CDM-typischen Durchbrüchen der Gate-Isolierschicht, sondern erstmals auch die eines geschädigten pn-Übergangs (A). Die Arbeit präsentiert zudem ein innovatives Verfahren zum Abtasten des elektrischen Oberflächenpotenzials von beispielsweise Leiterplatten oder flexibler Elektronik (A), welches spezifische Informationen zur Identifizierung von ESD-Ursachen liefern kann. Schaltungssimulationen unterstützen die Experimente und bieten einen tiefen Einblick in die allgemeine Korrelation zwischen CDM und CC-TLP in Bezug auf die Variation spezifischer Prüfparameter. Diese Doktorarbeit liefert neue Erkenntnisse über die Untersuchung von ESD-Phänomenen und sollte eine entscheidende Rolle in der zukünftige Standardisierung von CDM und alternativer Testmethoden wie CC-TLP spielen.

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List of Acronyms

AMR	Absolute Maximum Ratings
ATE	Automated Test Equipment
ATIS	Analysis and Test of Integrated Circuits (A Fraunhofer EMFT research team)
BCD	Bipolar-CMOS-DMOS
BGA	Ball Grid Array
CBE	Charged Board Event
CBM	Charged Board Model
CCDM	Contact Charged Device Model (CDM)
CC-TLP	Capacitively Coupled Transmission-Line Pulsing
CDE	Cable Discharge Event
CDM	Charged Device Model
CDM2	Charged Device Model 2
CMOS	Complementary Metal-Oxide-Semiconductor
COF	Chip-on-Flex
DUT	Device under Test
ESPSP	Electrostatic Surface Potential Scanning Procedure
EM	Electromagnetic
EMC	Electromagnetic Compability

EMI	Electromagnetic Interference
EMMI	Emission Microscopy
EOS	Electrical Overstress
ESD	Electrostatic Discharge
ESDA	Electrostatic Discharge Association
FCBGA	Flip Chip Ball Grid Array
FCP	Field Charge Plate
FICDM	Field induced CDM
(FI)CDM	(Field induced) CDM
FinFET	Fin Field-Effect Transistor
Fraunhofer EMFT	Fraunhofer Research Inst. for Microsystems and Solid State Techn.
FWHM	Full Width Half Maximum
GGNMOS	grounded gate NMOS
GOX	Gate Oxide
GP	Ground Plane
HBM	Human Body Model
HMM	Human Metal Model
IC	Integrated Circuit
IoT	Internet of Things
JEDEC	Joint Electron Device Engineering Council Solid State Technology Association
LGA	Land Grid Array
high-Z CDM	High Impedance CDM
low-Z CCDM	Low Impedance Contact CDM

LU	Latch-up
M-CDM3	Modular Charged Device Model
MOS	Metal-Oxide-Semiconductor
PCB	Printed Circuit Board
PI	Polyimide
RF	Radio Frequency
SBD	Soft Breakdown
SCR	Silicon Controlled Rectifier
SEM	Scanning Electron Microscope
SMA	SubMiniature Version A
TC	Test Condition
TDR	Time-Domain Reflectometry
TDT	Time-Domain Transmissometry
TL	Transmission-Line
TLP	Transmission-Line Pulsing
TLU	Transient Latch-up
VF-TLP	Very-Fast Transmission-Line Pulsing
(VF-)TLP	(Very-Fast) Transmission-Line Pulsing
VNA	Vector Network Analyzer
WCDM2	Wafer Level Charged Device Model
WLCSP	Wafer Level Chip Scale Package

Chapter 1

Introduction

The main objective of the introduction is to present the large area of Electrostatic Discharge (ESD), to give a brief overview of the state of research and technology and to motivate the overall aim of this thesis.

1.1 The field of Electrostatic Discharge (ESD)

Most electrical failures of semiconductor devices in manufacturing processes and in the field fall under the concept of Electrical Overstress (EOS) [1]. The general term EOS describes any electrical stress that exceeds any of the specified Absolute Maximum Ratings (AMR) of a product and causes it to fail (reversibly or irreversibly, immediately or delayed) [1]. The root causes of EOS can generally be divided into four different kinds of electrical stress: Electrostatic Discharge (ESD), Latch-up (LU), Electromagnetic Interference (EMI) and other EOS causes like mishandling or misapplication [2].

ESD is a subset of EOS and a major failure mechanism of integrated circuits and sensors. Electrical charge and discharge phenomena become visible in daily life, in the form of e.g. flyaway hairs after brushing or small flashes of light when taking clothes out of the dryer [3, p. 1]. Probably all of us have experienced ESD in everyday situations like when walking across a carpet, especially on a dry winter day, and then touching someone else or a metal object [3, p. 1]. Especially sportsmen involved in ball games know only too well the electric spark, which occurs during physical contact with a second player after having bounced or dribbled the ball on a synthetic hall floor. On a larger scale, thunderstorm lightnings impressively demonstrate the devastating power of electrostatic discharges unleashed by nature. But what is hidden behind the abstract term ESD in the field of microelectronics?

By definition, the term ESD describes the transient discharge of static charge [4, p. 3]. In general, an ESD event consists of two main mechanisms, the charge generation and the discharge [3, pp. 16–21]. The charge generation is mainly governed by triboelectrification, induction, and conduction. Depending on the capacitance of the charged object, the resulting charge imbalance generates a voltage difference between the object and its environment. The discharge mechanism describes the charge balancing of electrostatic loads until the voltage of the object equals the voltage of its environment.

The field of ESD primarily deals with the characterization of charge and discharge mechanisms of semiconductors on wafer, device and system level and focuses on the development and standardization of ESD test methods used to closely simulate real-world ESD-events. The generated know-how is necessary to establish ESD-safe environments in manufacturing and comprises, for example, the mitigation of personnel generated electrostatic discharges [3, pp. 98–100]. Furthermore, ESD testing allows the classification of solid state electronics according to their ESD sensitivity. This facilitates the development and improvement of ESD protection for semiconductor components to ensure ESD-safety during manufacturing and long-term reliability in the field [4, p. 47]. As emerging technology advances, electronic devices become faster and more compact and thereby constantly open up new potential applications, e.g. in the field of flexible electronics, the ESD problematic nowadays is of particular importance in the electronics industry [5–7].

There are several ESD models and test methods trying to replicate various ESD-scenarios occurring at wafer, device or system level in the laboratory. An overview of all prevalent ESD test methods can be found in the Appendix (Table A.1). Regarding ESD at device level, there exist two main stress models: the Human Body Model (HBM) and the Charged Device Model (CDM). The HBM deals with the susceptibility of electronic devices to be damaged from being contacted by a charged human being. Complementary to this, the CDM [8, 9] deals with the charging of semiconductor devices through triboelectric or electrostatic induction processes [10] and their transient discharges when being grounded via one pin or pad. The CDM is the predominant model describing the extremely fast, high peak current discharge of charged semiconductor devices in manufacturing and automated handling environment [11].

Being termed as the ESD stress model, the standardized test method CDM was established worldwide for product qualification. In principle, the CDM method simulates a CDM discharge by approaching a previously charged Device under Test (DUT) by means of a metal pin, which triggers an air discharge resulting in a high current stress of the DUT in the ns-domain. The nature of the typical CDM damage is a gate oxide failure caused by the voltage drop, which was generated by the CDM discharge current.

1.2 Trends in ESD and deficiencies of the CDM test method

Nowadays, increasing CDM requirements regarding measurement precision, reproducibility and versatility in application have revealed more and more the limitations of the CDM test method, whose reproducibility is strongly affected by the air discharge and environmental conditions [12]. Prevailing circumstances, such as technology scaling towards the single-digit nanometer scale or the enormous increase of data rates of high-speed ICs, in combination with the deficiencies of the CDM test method compared to present-day and upcoming ESD requirements (Chapter 3) have aroused the development of a contact-mode test method called Capacitively Coupled Transmission-Line Pulsing (CC-TLP) [13, 14] (Chapter 4). This ultimately motivates the topic of this dissertation, namely the pulsed high current characterization of highly integrated circuits and systems.

1.3 Motivation of this thesis

One main focus of this thesis is to verify the capability of CC-TLP to reproduce the failure locations and failure signatures of ESD failures observed in the manufacturing process, which are addressed by the CDM test method. Starting with an “ancient” 3 µm NMOS technology, the correlation between CDM and CC-TLP was already demonstrated for 90 nm and 130 nm CMOS technologies, at packaged device and at wafer level in several studies in the last decade [15–19] (Section 7.1). Summarizing the latest results of previous research, this thesis extends previous investigations by correlation studies between CDM and CC-TLP on a very small packaged IC (package footprint 7.5 mm^2) manufactured in a 0.25 µm BCD technology [20, 21], on a 28 nm ultra-high-speed CMOS IC for network applications (25 Gbps) [22] and for the first time on a large, flexible 0.35 µm Chip-on-Flex (COF) assembly [5] (Section 7). The findings, including e.g. the first analysis of a pn-junction failure induced by CC-TLP, are especially highlighted by a parameter study, which investigates the CDM to CC-TLP-correlation from a theoretical point of view (Section 8). Thereby, this work strongly contributes to the establishment of the CC-TLP stress test method in the industrial environment and supports its way to become an industry standard.

Additionally, special CC-TLP measurements in complement to CDM testings showed that dealing only with peak currents as failure thresholds may not always be sufficient as there might exist additional critical stress parameters, e.g. the current slew rate [20–22], impulse shape or the energy content [5] of the stress pulse. CDM correlation issues reported today might also have the same root cause although obfuscated by the limited metrology bandwidth and the variability of the uncontrolled air discharge. Despite decades of application, there is still a significant lack of understanding about these influences as well as the interaction of the tester and the DUT including the package, particularly because the investigation of these parameters is not directly addressable by the poorly reproducible CDM test method. The highly reproducible test method CC-TLP, however, provides this capability, as it is already employable on wafer-level and enables, besides the monitoring of stress pulses with a ps-resolution, the controlling and tuning of parameters like the rise time or the pulse width. Therefore, another important aspect of this thesis is the revelation and investigation of these potential critical stress parameters as this seems to be the key to significantly improve CDM qualification procedures for classifying CDM sensitivities in the future.

1.4 Overview and outline of the dissertation

After giving a short introduction of the prevalent ESD stress models and test methods that are relevant for this thesis in **Chapter 2**, **Chapter 3** summarizes current and future ESD challenges in order to demonstrate the incapability of the CDM test method to fulfill them. The need for a reproducible ESD test method in the CDM-domain leads to the introduction of CC-TLP in **Chapter 4**. This chapter contains important information on the system calibration, reconstruction and tuning of the CC-TLP stress current waveform and the post measurement embedding/de-embedding techniques that have been necessary to address the single-digit ps-domain. It ends up with the presentation of other alternative CDM-like testing methods and modifications apart from CC-TLP. **Chapter 5** compares the peak current reproducibility of CDM and CC-TLP and discusses the consequence of using multizaps in CDM testing. **Chapter 6** contains a bandwidth characterization of the CDM and CC-TLP components used for the measurements within this thesis. It furthermore introduces a newly developed method (ESPSP) for scanning the surface potential across a DUT, used to gain information about the root cause of the electrostatic stress.

Chapter 7 provides a brief overview of previous correlation studies between CDM and CC-TLP in terms of the peak current failure thresholds and failure signature. It presents, in view of the influences of potential critical stress parameters, the CDM/CC-TLP correlation studies that are performed in the course of this thesis. Thereby, **Section 7.2** analyzes for the first time a pn-junction failure of a large COF assembly in which the CDM/CC-TLP correlation could be established according to impulse energy and multi-zap wear-out effects rather than peak current. Conversely, **Section 7.3** deals with a very small packaged IC, which has shown non-reproducible voltage failure thresholds in the CDM tests of three different CDM testers. Together with the high-speed IC which is investigated in **Section 7.4**, it shows a high sensitivity on the current slew rate. The experimental correlation studies are complemented by **Chapter 8** in which the correlation between CDM and CC-TLP is investigated theoretically. The **Conclusion** summarizes the thesis, highlights the major results and identifies, based on the findings presented in this thesis, meaningful approaches regarding further research in this field.

Chapter 2

Prevalent ESD qualification and characterization methods

Various forms of ESD appear in the field of semiconductor manufacturing and in the system end-user environment. This chapter particularly deals with Charged Device Model (CDM) testing, which is the globally employed, standardized ESD test method at device level used to emulate real world device level ESD events in the nanoseconds-domain during IC manufacturing and handling. The chapter further presents the ESD characterization method (Very-Fast) Transmission-Line Pulsing ((VF-)TLP), as its concept directly lead to the contact-mode test method Capacitively Coupled Transmission-Line Pulsing (CC-TLP), which is in focus of this thesis. For the sake of completeness, an entire overview of all existing ESD test methods can be found in Appendix A.

2.1 ESD qualification methods

The relevant ESD-types for semiconductors on device level can basically be assigned to two ESD stress models, the Human Body Model (HBM) and the Charged Device Model (CDM). The HBM describes the discharge of a charged person through a pin of the device, via a specified path through the IC and via the grounded pins to ground (Fig. A.1). As HBM is not of particular relevance for the context of this thesis, it can be found in Appendix A.1. Mostly relevant for this thesis is the CDM that is introduced in the following sections.

2.1.1 The Charged Device Model (CDM)

In the course of increasing automation of semiconductor manufacturing and processing in the last decades, CDM has gained in importance with respect to HBM (Appendix A.1). Proposed for the first time in 1970s and 1980s [8, 9], CDM is the primary model describing the discharge of charged semiconductor devices in manufacturing and automated handling environment [11]. In the CDM scenario, charge is stored in the packaged part itself, mainly in the capacitance between the conductive layers of the package and the surrounding ground. During the approach of the charged device to a conductive object at a different electrostatic voltage, a discharge takes place. Depending on the voltage difference, which can be between a few tens of Volts up to several Kilovolts, this can occur either through an air discharge as soon as the breakdown field strength of air is exceeded, or through field emission or contact of both objects, if the breakdown condition of the gas is not fulfilled [4, p. 11]. The field strength for breakdown of air is, depending on the humidity level and the level of ionization, typically around $3\,\mathrm{MV\,m^{-1}}$ [23]. In any case, the device is stressed by an extremely fast and narrow pulse with a high peak current in the nanoseconds-domain. This stress current enters the IC via a single pin and spreads over the distributed capacitance of the device with respect to the surrounding ground. The resulting voltage drops produced by the CDM stress current typically lead to voltage driven failures in the attached gate oxides, or other voltage susceptible devices.

2.1.2 CDM failure protection strategies

In order to protect the chip during manufacturing, on-chip ESD protection structures have to be implemented. Figure 2.1 depicts the schematic of a CMOS inverter with double diodes used to protect the MOS transistors against a CDM-induced gate oxide (GOX) breakdown.

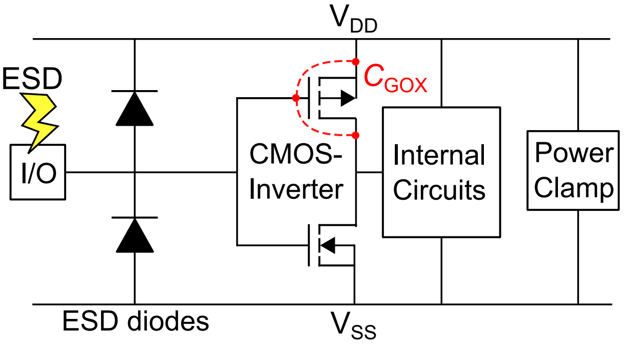

Figure 2.1 Schematic of double diodes as I/O ESD protection for a CMOS IC.

While being reverse-biased under normal operating conditions, the double diodes provide a low impedance shunt path for stress currents with an amplitude above the positive (V_{DD}) or below the negative power supply voltage (V_{SS}). A power clamp ensures the discharge of the V_{DD} line to V_{SS} during ESD stress. Besides double diodes (Fig. 2.1), there is a wide variety of

ESD protection circuits on-chip and on system level like grounded gate NMOS (GGNMOS) elements or Silicon Controlled Rectifier (SCR) structures. Key parameters of the ESD protection concept are the triggering speed, clamping voltage, series resistance and the capacitive loading budget [24, p. 24] of the protection structure. Especially for very fast rising CDM discharges, the dynamic behavior of the protection circuit plays a crucial role. Depending on the limited triggering speed of every ESD protection element, which is already given by the transit time of charge carriers [25, p. 133], a fast CDM discharge might lead to a critical transient voltage overshoot across the ESD protection element, leading to an increased voltage drop across the gate oxide capacitance C_{GOX} of the MOS transistors [26, 27]. In order to avoid CDM discharges from the outset, CDM countermeasures like the usage of air ionizers or dissipative materials aim to prevent the device from charging or from coming into contact with metal parts.

2.1.3 CDM testing

Testing the CDM and HBM (Appendix A.1) robustness of new products is a part of the standard production release process. This is intended to ensure the IC to survive in the manufacturing environment, which includes activities like manufacturing, packaging, labeling, assembling, testing, shipping, etc. [28]. Collected test results can help to identify weaknesses in the protection design and provide crucial information to the ESD protection designers to improve the layout in order to preserve safe ESD reliability during manufacturing. The standardized test method CDM is used to quantify the ESD robustness of packaged devices. The idea for an automated CDM tester firstly appeared between 1986 [29, 30] and 1989 [31] and the first CDM standards followed only a few years later [32, 33]. Nowadays, CDM stress testing is well-established for product qualification.

Before performing CDM tests on packaged devices, a calibration of the tester according to one of the different CDM standards [10, 34–36] is recommended. In principle, CDM test modules with predefined capacitances have to be stressed with different voltage levels in order to verify the recorded waveforms. Besides the rise time, the pulse width, the waveform overshoots and undershoots, especially the peak current value has to fulfill the required specification in order to exclude undesired effects during testing [4, p. 32].

The principle of CDM testing is illustrated in Figure 2.2. The Device under Test (DUT) is placed in “Dead Bug” position upside-down on a dielectric layer made of FR4 or similar epoxy-glass material [36] that covers the Field Charge Plate (FCP). This results in a well-defined capacitance $C_{\text{FCP-DUT}}$. The CDM discharge head consists of a square plane called Ground Plane (GP), which is positioned above the DUT and forms the capacitance $C_{\text{FCP-GP}}$ with the FCP and the capacitance $C_{\text{DUT-GP}}$ with the DUT. The GP is connected to the oscilloscope by the outer conductor of a 50 Ω coaxial cable. The cable core is leading from the oscilloscope to a spring-loaded pogo pin with a diameter of around 0.5 mm, which is routed through a hole in the GP enabling the pins or pads of the DUT to be contacted by the pogo pin from the top. A 1 Ω disk resistor between the pogo pin and the GP separates the inner and outer conductor of the coaxial cable and serves as a current sensor for the CDM measurements (Fig. 2.2).

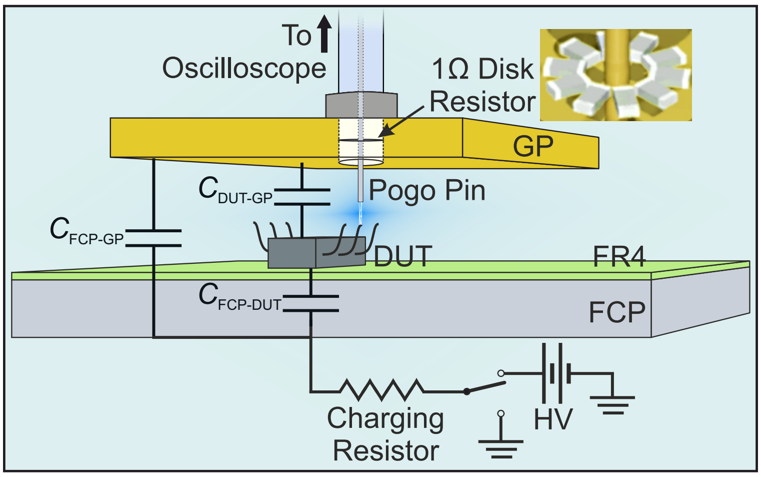

Figure 2.2 FICDM test setup schematic.

The CDM testing procedure basically consists of **five** steps: In a **first** step, the targeted pin or pad of the DUT is positioned directly below the pogo pin of the CDM discharge head. **Then**, the FCP is biased via a high ohmic charging resistor ($\sim 100\,\text{M}\Omega$, Fig. 2.2) to a target precharge voltage level. This directly leads to a field induced charge separation within the DUT. The high ohmic charging resistor is used to prevent premature damage of the DUT during charge separation. Analogously to this field-induced charging of the device [31] (hereinafter referred to as FICDM), also a direct charging of the DUT would be possible. The direct charging method is only allowed in the CDM standard for components in the automotive electronics industry [35] and will not be further discussed in this thesis. In a **third** step, the spring-loaded pogo pin of the CDM probe approaches one pin or pad of the DUT. On its way down, a statistically based so-called “lucky electron” triggers a spark channel between the pogo pin and the pin or pad of the DUT. This air discharge results in a high current stress of the IC, which is now charged. Similar to an ESD event in nature, the transient discharge occurs through only one pin or pad of the DUT within a few nanoseconds. The bypassing of the capacitance $C_{\text{DUT-GP}}$ by the pogo pin and 1 Ω disk resistor results in a charge redistribution between the capacitance $C_{\text{FCP-DUT}}$ and $C_{\text{FCP-GP}}$ [37]. The stress current can be measured through the voltage drop across the 1 Ω disk resistor. When performing the so-called dual polarity CDM, the pogo pin is subsequently lifted again and the FCP is grounded

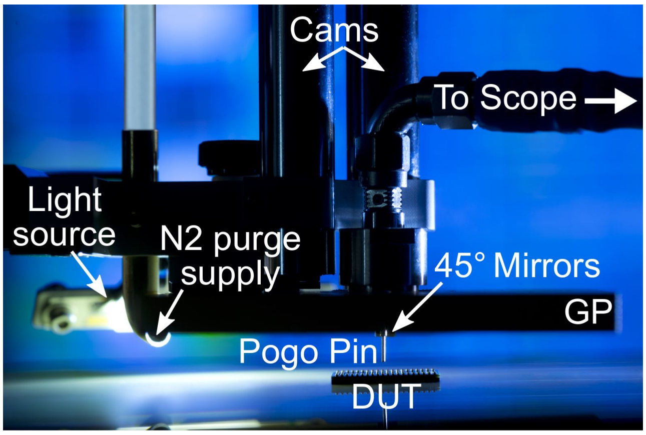

Figure 2.3 Photo of the CDM discharge head used during this dissertation, positioned above a BGA package.

in the **fourth** step. At that moment, the capacitance $C_{\text{FCP-DUT}}$ is still charged. By approaching the DUT again in the **last** step, $C_{\text{FCP-DUT}}$ discharges and the DUT is stressed with opposite polarity. A photo of the CDM discharge head used within this dissertation is depicted in Figure 2.3. To reduce the enormous peak current variations caused by the air discharge, the test area is purged with dry nitrogen during CDM testing. The package alignment is supported by two vertically orientated, cylindrical-shaped cameras, which allow a direct view of the pogo pin by means of two 45° mirrors.

2.2 ESD characterization methods

The ESD qualification tests are only capable of providing a failure level of the device. In order to tailor the suitable ESD protection element to the respective semiconductor device, ESD designers need more detailed information about the ESD-behavior of the device and especially of the protection structure. Hence, high current measurements in the ESD regime have to be performed. However, investigating the I-V characteristics by means of conventional DC current measurements would induce self-heating effects and the dissipated energy could lead to heat destruction of the DUT. This demands for a characterization method of devices and circuits in pulsed mode, which is introduced in the following paragraphs.

2.2.1 Transmission-Line Pulsing (TLP)

The idea of performing Transmission-Line Pulsing (TLP) for modeling of ESD phenomena was introduced in 1985 [38]. The structure of the pulse generator is based on a charged $50\,\Omega$ coaxial cable acting as a pulse source (Fig. 2.4). This charged Transmission-Line (TL) discharges through a relay and transmits a square-shaped impulse into one pin or pad of the DUT. The amplitude of the pulse is half of the precharged level. The pulse width t_{TL} is directly proportional to the length of the charged TL cable L_{TL} (Fig. 2.4) given by $t_{\text{TL}} = 2 \cdot L_{\text{TL}}/v_{\text{TL}}$ [39, 40], where v_{TL} describes the propagation velocity on the TL. The return path is established by the outer conductor of the picoprobe, typically positioned on a V_{DD} pin, defining a specific stress path through the chip in order to characterize the ESD protection structures between the stress pin (input) and the reference pin (output). A current transformer measures the stress current I_{DUT} (Fig. 2.4, blue). A second, high impedance, voltage-sensing picoprobe is added to measure the voltage drop V_{DUT} across the two pins. By default, the TLP test procedure uses a series of pulses with increasing pulse amplitude and monitors the electrical DC characteristic between the stress pin and reference pin after each stress pulse [4, p. 48]. Through the identification of the leakage current between the two pins, an ESD failure can be detected. Besides high current I-V characteristics, TLP provides inter alia information about the transient turn-on/off characteristics of ESD protection structures and the breakdown effects.

Many authors have published a correlation of the failure threshold level obtained by TLP and HBM stress measurements [41–43]. Thus, TLP is applicable multifunctionally, i.e. to characterize and to estimate the HBM immunity simultaneously. To characterize the behavior of protection elements during a HBM stress event, high impedance TLP setups with pulse widths t_{TL} of typically 100 ns are used.

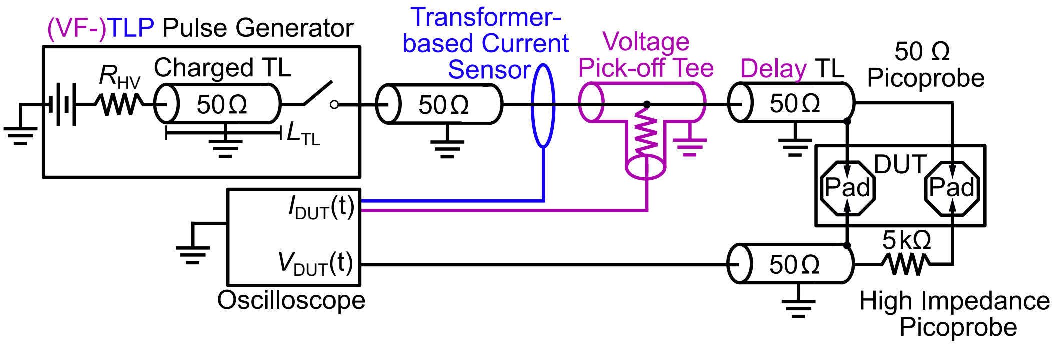

Figure 2.4 Kelvin (4-Wire) picoprobe measurement setup of TLP (blue components) and VF-TLP (purple components). Due to the longer pulse widths in TLP measurements, the stress current I_{DUT}, consisting of the superposition of the incident and reflected pulse, can be measured directly by means of a current sensor (blue). In VF-TLP measurements, the incident and reflected pulse have to be measured separately by means of a delay line and a pick-off tee (purple) and are superposed post-hoc (Section 4.3.3). Typically, a second, high impedance (5 kΩ) picoprobe measures the voltage drop V_{DUT} between the two pins.

2.2.2 Very-Fast Transmission-Line Pulsing (VF-TLP)

In order to gain a deeper insight into protection elements in the CDM regime and to study the breakdown conditions of gate oxides, Very-Fast Transmission-Line Pulsing (VF-TLP) was firstly introduced in 1996 [39]. By evaluating the behavior and triggering speed of protection circuits already on wafer level, VF-TLP provides crucial information for the ESD protection design to meet the ESD design window. The pulse widths used in VF-TLP are in the range of $t_{\mathrm{TL}} \approx 1\,\mathrm{ns}$ in order to study the DUT in a more adiabatic region with significantly reduced self-heating [44] and to imitate the conditions of the extremely fast and narrow CDM discharge events. The incident and reflected pulse are measured separately by means of a delay line and a pick-off tee (Fig. 2.4, purple) and are superposed by the time-domain reflectometer principle post-hoc [45] (Section 4.3.3). It is important to emphasize that the two-pin characterization method VF-TLP differs fundamentally from the single-pin qualification test method CDM. In CDM, the entire chip discharges through one pin or pad, whereas the stress current induced by VF-TLP follows a defined path between a stress pin and a reference pin (Fig. 2.4). Consequently, VF-TLP is an ideal tool to study the operation of IC protection structures under stresses similar to what is encountered in the CDM test, but is not necessarily able to replicate the CDM failure level of a complete product IC [39, 40].

Chapter 3

Critical evaluation of CDM testing

The following chapter addresses current industry trends, which lead towards a steadily increasing ESD sensitivity of advanced technologies, resulting in a growing need for an improved CDM test precision and monitoring.

3.1 Trends and challenges in the ESD protection of semiconductors

Prevailing trends in the semiconductor industry entail new challenges in the field of ESD protection. Maintaining the performance goal of Moore's law, silicon technology has scaled towards the deep sub-100-nm regime and beyond resulting in an increased ESD sensitivity of silicon devices to be protected [11]. Particularly, the resulting increase in current densities and power dissipation in metal regions and interconnects coupled with the reduction of gate oxide thicknesses, which leads to a reduced dielectric breakdown voltage (Fig. 3.1), are important factors.

At the same time, IC components are incorporated in larger, higher pin count packages with highly complex pin layouts, very small sized pads or balls and impedance controlled interconnects. These packages entail the hazard of unleashing very fast and high peak current discharges during a CDM event [11]. Ball Grid Array (BGA) and Land Grid Array (LGA) packages of more than 3000 pins and an area larger than $3000\,\mathrm{mm}^2$ are not uncommon for modern microprocessors [46]. Moreover, this often leads to more ESD-critical steps in manufacturing, automated handling, assembly and testing.

Approaching the limits of scalability, novel technology trends like 2.5D or 3D integration seem to be an alternative to transistor scaling. However, the evolution of multi-chip packaging

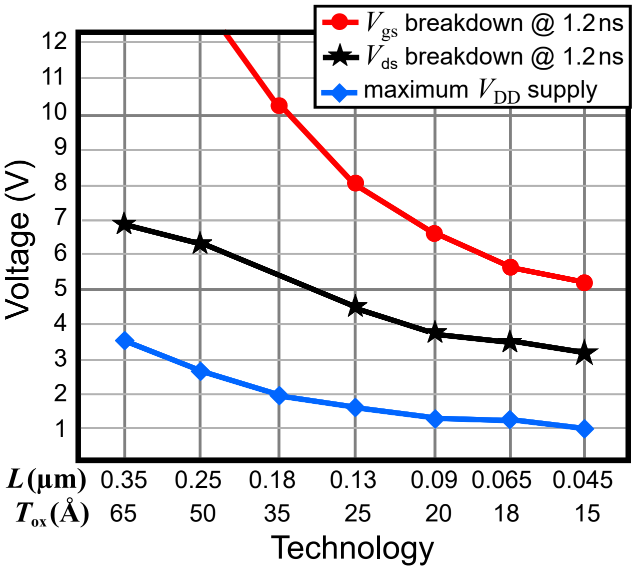

Figure 3.1 Trends of NMOS transistor breakdown voltages against technology scaling. A more advanced technology with a feature size transistor length L implies a reduced gate oxide thickness T_{ox}, which consequently results in a reduction of the gate oxide breakdown voltage V_{gs} (●) and drain to source breakdown voltage V_{ds} (★). The CDM stress on the NMOS transistor was mimicked with a 1.2 ns VF-TLP measurement. From [11], p. 33. Reprinted with permission.

further supports a growth in package size and adds a number of complex process steps posing new potential ESD hazards in manufacturing [46].

During our era of world-wide networking, the amount of data to be processed is expanding dramatically. However, a steady increase in data rates in high-speed IOs ($>$ 50 Gbps) requires more and more a limitation of the permitted ESD capacitive loading budget [24, p. 24], which comes at the expense of degraded ESD robustness [7, 22]. Hence, the minimum CDM sensitivity level of many high-speed IOs manufactured in a 22 nm technology and beyond already falls below 125 V (Fig. 3.2) and is forecast to reduce to below 50 V by 2020 [46].

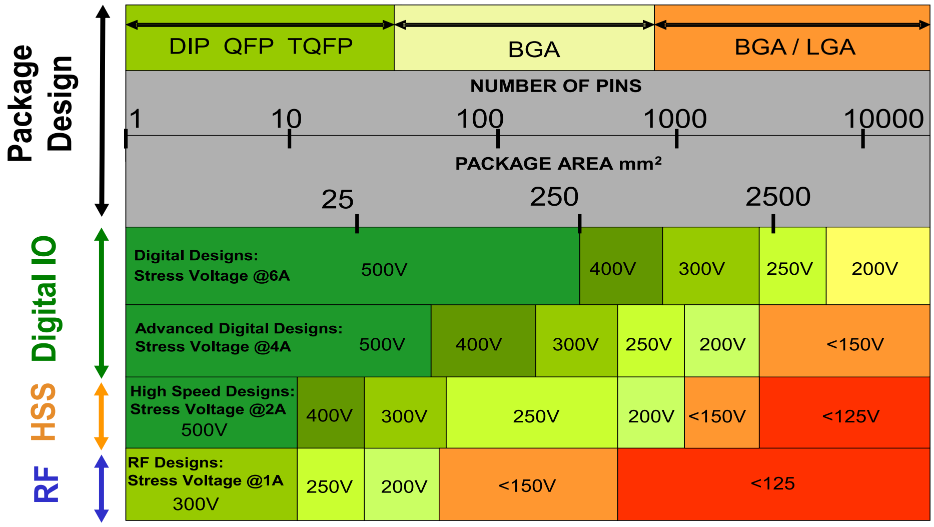
Package Design
Digital IO
HSS
RF
DIP QFP TQFP
BGA
BGA / LGA
NUMBER OF PINS
1
10
100
1000
10000
PACKAGE AREA mm²
25
250
2500
Digital Designs: Stress Voltage @6A
500V
400V
300V
250V
200V
Advanced Digital Designs: Stress Voltage @4A
500V
400V
300V
250V
200V
<150V
High Speed Designs: Stress Voltage @2A 500V
400V
300V
250V
200V
<150V
<125V
RF Designs: Stress Voltage @1A 300V
250V
200V
<150V
<125

Figure 3.2 CDM sensitivity levels of 22 nm technology node illustrating the projected effect of IO design and IC package size. From [46], p. 5. Copyright © 2016 EOS/ESD Association, Inc. Reprinted with permission.

A present trend known as Internet of Things (IoT) further pushes the ever-growing, prospective demand of high-speed devices for internet operations and network applications. The number of devices with high data exchange and processing capabilities is expected to grow from 18 billion in 2017 to 28.5 billion in 2022, exceeding three times the global population by 2022 [47]. While mobile data traffic has grown 18-fold between 2011 and 2016, the Cisco Visual Networking Index (VNI) predicts a sevenfold global mobile data traffic growth between 2016 and 2021, reaching 49 exabytes per month by 2021 [48]. The preservation of enhancing IC performances places severe constraints for design of onchip ESD protection and causes the closing of the ESD design window for sub-micron technologies. Moreover, the lower designed CDM protection levels raise the demand for an improved CDM control in production areas (Fig. 3.3).

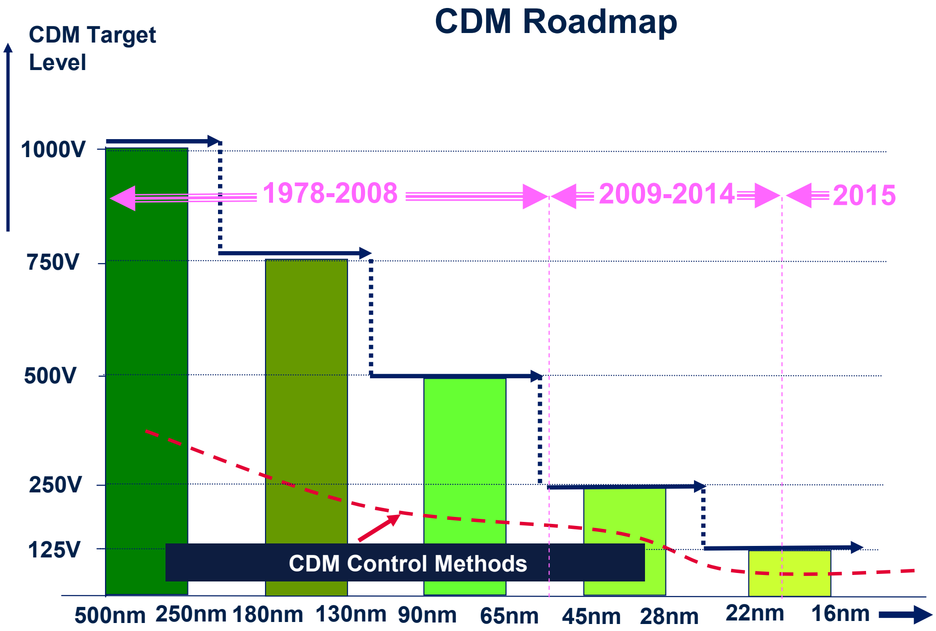

Figure 3.3 The continuous advancement of IC technologies leads to a reduction of the CDM target levels and an improvement of the corresponding control requirements at factory level. From [11], p. 77. Reprinted with permission.

3.2 Deficiencies of the CDM test method to fulfill present-day and upcoming ESD requirements

One key requirement to meet the ESD challenges of the advanced technologies listed in Section 3.1 is to have a test method which is capable of qualifying the further reducing CDM failure thresholds accurately. The following paragraphs shall reveal the limits of the CDM test method and motivate the development of the alternative contact-mode test method called CC-TLP.

Lack of repeatability and reproducibility

Several studies have revealed the limits of the CDM test method, as it lacks repeatability (strong variation of the discharge current even for one tester) and reproducibility (limited correlation between different testers) mainly due to the air discharge variation [20, 21]. This is compounded by the fact that CDM peak current repeatability further decreases with lower precharge voltages [49]. Conversely, modern ultra-deep sub-micron technologies with significant chip-to-chip variations and closing margins for test uncertainties require even higher CDM precision. Hence, CDM qualification is expected to soon become even more problematic for the industry. False positive CDM test results, based on CDM's test uncertainties, may risk yield losses in factory. False fails increase the risk of overdesign.

Strong influences of DUT, CDM testers and test environment

CDM testing is subject to complex RF-interaction between the CDM discharge head and the DUT as well as to strong environmental influences like the humidity in the test chamber, surface conditions of the pogo pin and the device pins, the approach velocity of the pogo pin to the device pin, etc. [12, 50]. Inadequate specifications of the CDM test equipment and large permissible variations in the tester setup parameters provoke that different CDM testers or CDM testing standards [10, 36, 51] often result in different CDM robustness levels for the same device [20, 21, 11] (Section 7.3).

Limited applicability of CDM

A third, but equally important motivation for the development of an alternative contact test method is that CDM testing is only employable on packaged devices and cannot be applied on wafers, bare dies and Wafer Level Chip Scale Packages (WLCSPs) with very small pins and pin pitches. Moreover, CDM is not capable of characterizing protection elements. Due to the vertically downward-pointing pogo pin of the CDM test head with a diameter of around 0.5 mm and the hardly controllable spark discharge, CDM reaches its limit with tighter packaged pins and is only capable of stressing pins or balls with a minimum contact pitch of around 0.3 mm.

Advanced technologies are based on hundreds of processing steps, mask sets and processing cost of millions of euros. Hence, potential weaknesses with respect to ESD, which would imply the necessity of a redesign, need to be identified as soon as possible. Assuming a tenfold increase of the total costs of remedying a deficiency in ESD protection at every production level from wafer to system [52], an early pre-check for the CDM susceptibility on wafer level before packaging could dramatically reduce expenses. CC-TLP can be applied on wafers and bare dies and and thus enables the access to CDM relevant data at an earlier development stage, which may also help to deliver the product to market within a shorter period.

Conflict between data quality and testing time

One direct consequence of the poor repeatability of the CDM test method is the usage of multiple zaps per pin and voltage level for statistical reasons. In the history of CDM testing, many debates were held about the appropriate number of CDM stress pulses that should be used. Mainly, a statistical benefit, which improves data quality, is in conflict with testing time consumption. The qualification test according to JESD22-C101F [10] requires at least one positive and one negative stress pulse per pin. While the ESD standard ANSI/ESD S5.3.1 [51] states three zaps per polarity, their joint standard ANSI/ESDA/JEDEC JS-002-2014 [36] requires to apply at least one discharge per polarity to each pin and to test a minimum of three units. The different and often not clearly defined CDM standard specification regarding the number of stress pulses per voltage level, like “at least one”, may consequently lead to an inconsistent classification and an unreliable correlation between different CDM tests. Section 5.2 examines this topic from a scientific point of view and provides new impulses on this issue by means of a purely statistical analysis. In addition to this conflict, the number of CDM pulses might have an influence on the degradation and ultimately on the failure threshold of some pn-junctions [5] (Section 7.2). The number of zaps as a potential critical stress parameter leads directly to the last aspect of this discussion.

Incapability of CDM to investigate potential critical stress parameters

The last aspect to mention here relates to the failure mechanism and potential critical stress parameters of CDM. From the beginnings of CDM testing, the ESD sensitivities of devices have been qualified in terms of voltage levels, which, for an ideal CDM tester, represent the maximal precharge voltages that are applied to the FCP of the tester (Fig. 2.2) and which the DUT withstands in the CDM qualification test. This voltage is the primary parameter that defines the CDM discharge current. In the newest CDM standard, the ANSI/ESDA/JEDEC JS-002-2014 [36], the classification is reported as test condition (TC) rather than voltage level, officially allowing the usage of an additional voltage factor in order to compensate a variation in the actual plate voltage setting and to meet the required waveform specifications. Nevertheless, in contrast to HBM, the CDM stress of a specific voltage level strongly depends on the die and package size and is also influenced by the type of CDM tester, the test standard, the testing environment and artifacts. The nature of the typical CDM failure is a gate oxide failure caused by a voltage drop, which is generated by the CDM discharge current (Section 2.1.1). Thus, the precharge voltage is a vague indicator for the CDM robustness and a well-defined current level is, instead of a voltage level, the more meaningful parameter to characterize the CDM susceptibility and a critical design goal for ESD designers [11]. This fact has been ignored for many years. One main reason for this is that the CDM stress current is often not recorded and even if, it is significantly dependent on the bandwidth of the test system, e.g. of the oscilloscope used [20, 21].

In addition, measurements on different devices showed that even dealing with peak current failure thresholds only may not always be sufficient, since different critical stress parameters, e.g. the rise time, impulse shape or the energy content of the stress pulse might exist and have an influence on the failure level. Despite decades of testing, there is still a significant lack of understanding about these influences as well as of the interaction of the tester and the DUT including the package. One principal objective of this dissertation is to gain a deeper insight into the impact of different critical stress parameters as this seems to be the key to significantly improve CDM qualification procedures for classifying CDM sensitivities in the future. Until now, the possibility to investigate these critical parameters in the CDM domain was only limited, as they are not directly addressable by the poorly reproducible CDM test method. Thus, an alternative, highly reproducible test method, like CC-TLP, which provides the ability to monitor stress transients with a ps-resolution and to control and tune parameters like the rise time or the width of its stress pulses, is required.

Chapter 4

Capacitively Coupled Transmission-Line Pulsing (CC-TLP)

The contact-mode test method Capacitively Coupled Transmission-Line Pulsing (CC-TLP) [13, 14] has been developed in order to complement the commonly used, but due to air discharge highly unreliable [53], CDM testing method for product qualification, development and characterization. It eliminates the uncontrollable air discharge and combines the narrow-pulse high current stress pulses known from CDM with the reproducibility of the two-pin VF-TLP [39, 40] (Section 2.2.2), by directly connecting only one pin or pad of the DUT.

4.1 The CC-TLP setup and measurement principle

The CC-TLP probe is mounted on a micro-manipulator and suspended over the device or wafer. The test head contains a round, gold-plated brass plane called Ground Plane (GP) (Fig. 4.1), which is connected to the outer conductor of a coaxial cable. The inner conductor of the coaxial cable leads through a semi-rigid conductor to the contact needle of the CC-TLP probe through a small hole in the GP. The contact needle contacts a single pin of the floating DUT. While in contact, a highly reproducible fast rising rectangular voltage pulse is created by the (VF-)TLP pulse generator and transmitted through the coaxial cable and the contact needle of the probe to the DUT (Fig. 4.1). The floating DUT couples capacitively to both the GP positioned above and the chuck underneath the DUT. The resulting background capacitance C_b corresponds to the distributed capacitance of a packaged device in CDM and establishes the ground return path. C_b starts to charge up via the DUT with the rising edge of the pulse and to discharge with the falling edge of the pulse. Hence, the CC-TLP stress consists of two pulses with opposite polarity (e.g. Fig. 4.6, green curve). This is equivalent to

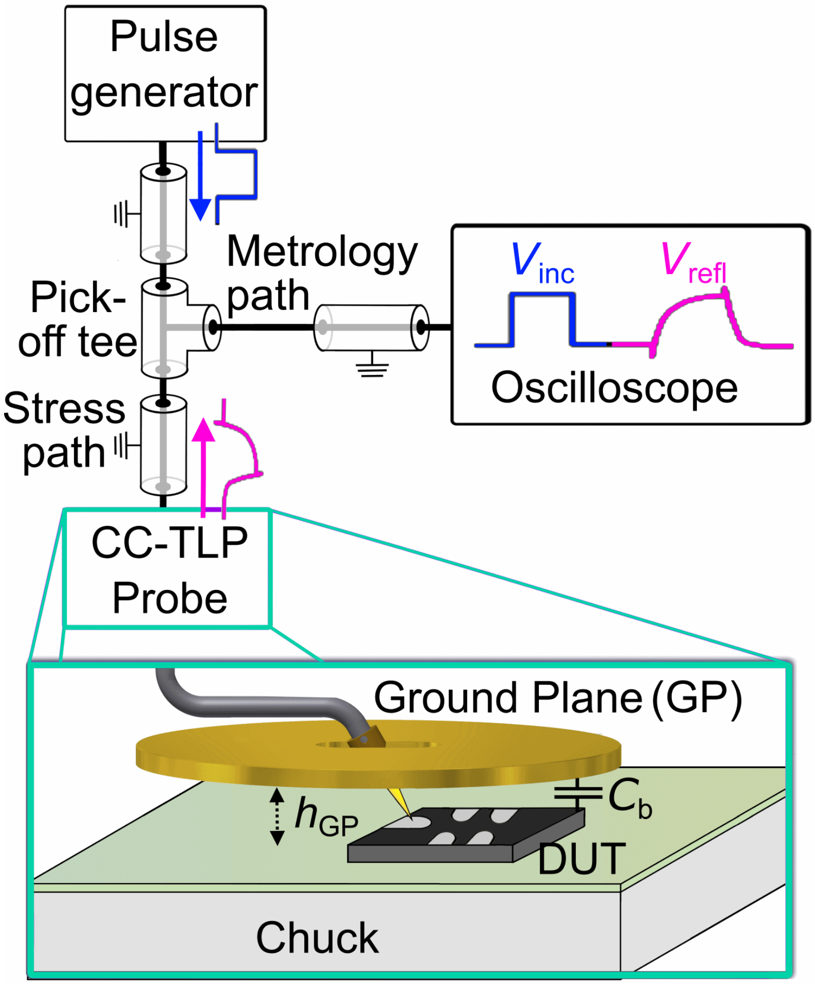
Pulse generator
Metrology path
Pick-off tee
Stress path
V_{inc}
V_{refl}
Oscilloscope
CC-TLP Probe
Ground Plane (GP)
C_b
h_{GP}
DUT
Chuck

Figure 4.1 Principle probe set-up for CC-TLP testing on package level.

two CDM stress pulses that are generated during dual polarity CDM testing (Section 2.1.3). The CC-TLP stress current $I_{TLP}(t)$ entering the DUT corresponds to the superposition of the incident pulse and the pulse which is reflected by the DUT [39, 40]:

$$I_{TLP}(t) = I_{inc}(t) + I_{refl}(t) = \frac{V_{inc}(t) - V_{refl}(t)}{50\,\Omega} \tag{4.1}$$

The ratio between incident voltage and current pulse $V_{inc}(t)/I_{inc}(t)$ is given by the system impedance $Z_0 = 50\,\Omega$. The reflected current pulse $I_{refl}(t)$ is phase shifted by π with respect to the reflected voltage pulse $V_{refl}(t)$, corresponding to an impedance of $-Z_0$. Optionally, a 6 dB or 10 dB attenuator at the output of the pulse generator is employed to reduce multiple reflections. Note that in Equation (4.1), the contact point of the CC-TLP needle with the pin or pad of the DUT is the reference point to which all parameters refer to. Since the

CC-TLP pulse widths can be very small ($< 0.5\,\text{ns}$) and with it the overlapping region of incident and reflected pulse at the DUT, a direct current measurement by means of a current sensor, which provides only limited bandwidths ($\leq 1\,\text{GHz}$), becomes inapplicable [54]. In order to determine the stress current $I_{\text{TLP}}(t)$ without distorting the signal, CC-TLP uses a $50\,\Omega$ SMA wideband pick-off tee and the remote sensing measurement principle [39, 40]: Identical to VF-TLP (Fig. 2.4), a fraction of both the incident $V_{\text{inc}}(t)$ and the reflected voltage pulse $V_{\text{refl}}(t)$ is split-off and fed into a single shot oscilloscope by means of a voltage pick-off tee between the pulse generator and the CC-TLP probe (Fig. 4.1). By time shifting the later arriving reflected pulse and superposing the two signals measured at the oscilloscope, the CC-TLP current $I_{\text{TLP}}(t)$ stressing the DUT can be determined by the time-domain reflectometer principle [45]:

$$I_{\text{TLP}}(t) = \frac{V_{\text{inc}}(t) - V_{\text{refl}}(t - \Delta t)}{50\,\Omega} \tag{4.2}$$

In contrast to Equation (4.1), the time and voltage parameters given in Equation (4.2) refer to the oscilloscope as reference point. Technically, the calculation of the stress current $I_{\text{TLP}}(t)$ requires the exact superposition of the fast rising edges of the measured incident voltage pulse $V_{\text{refl}}(t)$ and the reflected voltage pulse $V_{\text{refl}}(t - \Delta t)$, which is arriving after a delay time of Δt at the oscilloscope. Thereby, Δt is twice the transit time of the pulse along the stress path (Fig. 4.1). One prerequisite for this calculation is that the TL between pick-off tee and CC-TLP probe is sufficiently long with respect to the pulse duration, so that incident and reflected pulse do not partially overlap and can be determined separately. Further has to be considered that, while in CC-TLP the polarity of the stress current is defined by the transient pulse propagating to the DUT, the polarity of the CDM current is given by the polarity of the discharge, which corresponds to the polarity of the FCP. Thus, based on different definitions, the CC-TLP stress current is of opposite polarity as the CDM polarity [18]. Equation (4.2) does not consider resistive losses or dispersion effects of the signals between the DUT and the oscilloscope. Embedding/De-embedding techniques that take this effect into account, challenges of the time shift calibration on measured data and its impact on the peak current accuracy can be found in Section 4.3.

4.2 The CC-TLP stress testing procedure

In order to obtain the failure threshold current of the device tested by CC-TLP, typically a step stress is performed. This is done by stepwise increasing the pulse amplitude of the pulse generator. If the leakage current is a measure for the degradation of the DUT (e.g. in Section 7.3), the leakage current is monitored after each stress pulse by means of a curve-tracer or parameter analyzer with a second set of probes (Fig. 4.2, right side). The failure threshold current of the DUT is defined as the peak current of the stress after which the increase of the DC leakage characteristics exceeds a preassigned failure current. If a leakage current measurement is not possible (e.g. in Section 7.4), functional failure testing is used to determine a pass or fail of the DUT.

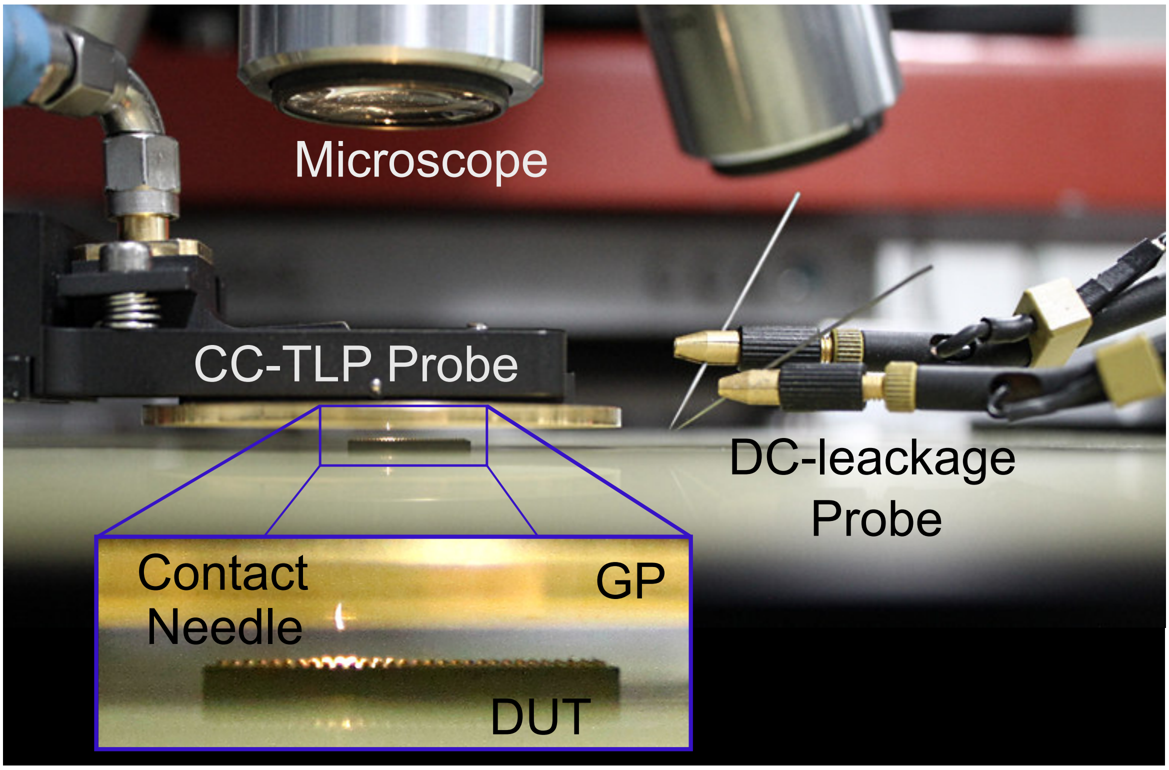

Figure 4.2 CC-TLP (left) and DC-leakage testing (right) at device level.

One of CC-TLP's main advantages is its wafer level capabilities resulting from its inclined steel needle with a tip radius of 12.7 µm or 25.4 µm (Fig. 4.3). In contrast to (FI)CDM and alternative test methods in the CDM-domain like Low Impedance Contact CDM (low-Z CCDM) or CDM2 (Section 4.5), CC-TLP can be applied on wafers, bare dies and Wafer Level Chip Scale Packages (WLCSPs) with very small pins and pin pitches. During waver-level testing, the CC-TLP GP might not only overlap the die that is contacted by the CC-TLP needle but also its neighboring dies. However, as investigated in [18], even the immediate neighboring dies experienced only about a quarter of the original CC-TLP stress. Beside the evaluation of the ESD robustness of a packaged device, bare die or wafer, CC-TLP is also capable to provide in-situ insight into the turn-on of the protection circuit. Prerequisite for that is a high bandwidth of the entire system, i.e. the CC-TLP probe, cables and adapters, the oscilloscope, etc.

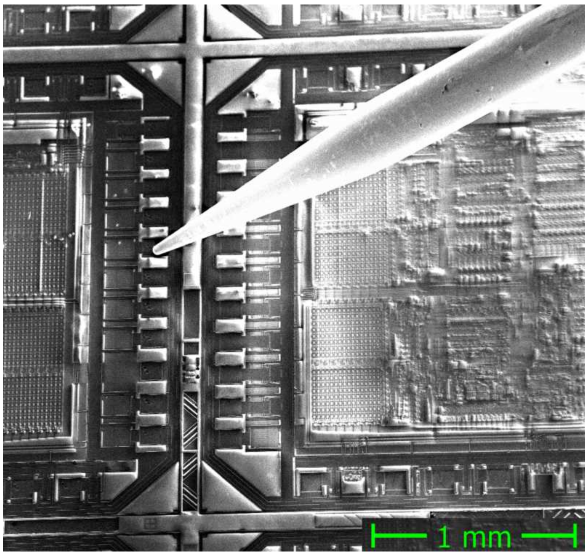

Figure 4.3 Scanning Electron Microscope (SEM) image of a CC-TLP contact needle. With the contact needle, even wafers and packaged devices with very small pins and pin pitches can be contacted accurately. For comparison, the 0.5 mm thick, vertically downward-pointing CDM pogo pin in combination with the hardly controllable spark discharge is not capable of addressing these small-scale structures.

4.3 System calibration and reconstruction of the stress current waveform

The following paragraphs outline the main aspects of the CC-TLP calibration and point to possible error sources that could influence the results of CC-TLP.

The CDM sensitivity is qualified in terms of voltage levels [10, 51] or test conditions [36], which represent, for an ideal CDM tester, the precharge voltage that is applied to the FCP of the tester. In CDM, this voltage is the primary parameter that defines, together with the background capacitance of the DUT, the CDM discharge current. However, in a typical CDM failure scenario, the discharge current is the relevant parameter, as it generates a voltage drop across an internal gate oxide capacitance of the DUT causing a CDM typical gate oxide rupture (Section 2.1.1). In contrast to CDM, the primary parameter of CC-TLP is directly the decisive stress current $I_{\mathrm{TLP}}(t)$, which is reconstructed from the voltages captured by the oscilloscope following Equation (4.2). This raises the question of how the CC-TLP stress current reconstruction can be realized experimentally, including the treatment of e.g. dispersion effects that are not considered in Equation (4.2) and how the CC-TLP stress current can be aligned with the CDM stress levels. Besides important aspects like the calibration and application of the CC-TLP measurement procedure, this section particularly indicates the main challenges of the reconstruction of the stress current.

4.3.1 Mechanical calibration of the CC-TLP setup

Similar to CDM, the first step before starting a CC-TLP measurement is the mechanical alignment of the system. This includes the parallel orientation of the GP with respect to the working surface, the compensation of any tilt angles and the adjustment of the GP height h_{GP} (Fig. 4.1) with respect to the contact needle tip. The latter specifies the length of the contact needle that protrudes from the GP and thus defines the capacitive coupling between the DUT and the GP [5] (Section 4.4). By placing the GP on the surface of a specially developed calibration plate with milled slots of different depths between 0.1 mm and 1.0 mm [17] and lowering the contact needle until it is in contact with a selected milled slot, the CC-TLP setup is terminated by a short-circuit (Fig. 4.4). This allows a precise electrically guided adjustment of the separation height h_{GP}, which is set to 0.3 mm in most of the CC-TLP measurements.

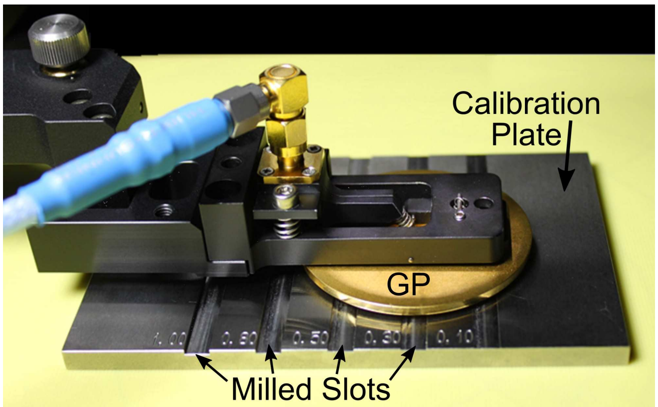

Figure 4.4 Adjustment of the CC-TLP GP height h_{GP} with respect to the contact needle tip by means of a calibration plate.

4.3.2 Correction of dispersion and distortion effects

As being interested in the superposition of incident and reflected pulses at the DUT (Eq. (4.2)), but only measuring both pulses at the location of the oscilloscope (Fig. 4.1), resistive and frequency dependent losses of the TLs, especially of the pick-off tee and the impact of parasitic resistances in series and parallel to the DUT have to be removed. To reconstruct the incident and reflected voltage pulse at the location of interest, i.e. at the tip of the CC-TLP needle, which is in contact with the pin or pad of the DUT, the reference plane have to be moved from the oscilloscope to the DUT.

Open/Short-calibration

Similar to (VF-)TLP (Section 2.2.2), the reconstruction of the incident and reflected voltage pulse can generally be realized by an Open/Short calibration. Hereby, voltage losses of the measured signals are partially corrected by simply multiplying the measured signals by an appropriate factor in the time domain. The factor that contains the attenuation across the stress path, for example, can be determined by comparing the pulse plateau of the incident and the reflected pulse when performing an open-circuit measurement (i.e. the CC-TLP needle is not in contact). Based on the (VF-)TLP calibration techniques described in [41, 55], a CC-TLP open-circuit and short-circuit measurement (Section 4.3.1) further provides necessary information to correct parasitic resistances parallel or in series to the DUT.

Nevertheless, the Open/Short-calibration technique properly reconstructs only the plateaus of the incident and reflected pulse at the DUT, which eventually allows for an appropriate reconstruction of the peak current of the stress pulse. However, as revealed in this thesis (Section 7.3 and 7.4), the rise time or slew rate of the stress current can be an additional critical stress parameter beyond the peak current. The investigation of the ultra-high-speed (25 Gbps) IC in Section 7.4 showed that subtle differences of the rise time of only a few picoseconds had a direct influence on the failure threshold. Challenging the limits of today's metrology, this finding required a CC-TLP rise time evaluation in the single-digit ps-domain. As the Open/Short calibration does not consider any frequency dependent losses that are necessary for a precise evaluation of the rising edge of a stress pulse, a more complex reconstruction technique had to be realized. This mathematical post-processing correction technique is generally known as embedding/de-embedding.

Embedding/De-embedding of the CC-TLP system

An embedding/de-embedding technique [56–58] considers frequency dependent losses and is the most precise method for the reconstruction of the CC-TLP stress current at the location of the DUT. It entails a complex implementation and long computation times but is a key prerequisite to reach a single-digit picosecond-resolution of the rise time in CC-TLP (Section 7.4). For the purpose of embedding/de-embedding the CC-TLP system, the frequency response of the pick-off tee, the CC-TLP probe and all cables and connectors of the CC-TLP setup are characterized using a high-frequency Vector Network Analyzer (VNA) (Section 6.1.2). The measured scattering parameters (S-parameters) of each of these components describe a complex transfer function $H(s)$. This enables the calculation of the reflected and transmitted waveforms in the time domain for any incoming waveform passing the component in the following way:

As a first step, the incoming time signal $V_{\text{inc}}(t)$ has to be Laplace transformed to $\mathcal{L}\{V_{\text{inc}}(t)\} = V_{\text{inc}}(s)$. The outgoing signals, i.e. the signal which is reflected $V_{\text{refl}}(s)$ and transmitted $V_{\text{trans}}(s)$ at the component can be derived from the incoming signal $V_{\text{inc}}(s)$ by multiplication with the complex transfer function $H(s)$. Subsequently, one obtains the outgoing signals $V_{\text{refl}}(t)$ and $V_{\text{trans}}(t)$ in the time domain by means of an inverse Laplace Transform $\mathcal{L}^{-1}$. A more simplified method is to convolve the incoming signal $V_{\text{inc}}(t)$ with the inverse Laplace transformed of the transfer function $\mathcal{L}^{-1}\{H(s)\}$, the so-called impulse response function $h(t)$, in the time domain instead. This powerful tool used to virtually "add" the impact of an electrical component on an incoming signal is defined as embedding.

Conversely, losses of a pulse having passed a component or being reflected by the component can also be removed. This is known as de-embedding. De-embedding of distortion effects from a measured signal request either the multiplication with the inverse transfer function $G(s) := 1/H(s)$ in the Laplace domain (Fig. 4.5, top left picture, red path) or directly the convolution with the inverse Laplace transformed of the inverse transfer function $g(t) := \mathcal{L}^{-1}\{G(s)\} = \mathcal{L}^{-1}\{1/H(s)\}$ (Fig. 4.5, top left picture, blue path) in the time domain.

A combination of both tools, embedding and de-embedding, allows the isolation of the DUT from the measurement setup. Therefor, it is necessary that the post-processing algorithm handles the incident and reflected pulse separately. In concrete terms, this means that for the reflected voltage pulse $V_{\text{refl}}(t)$, the impact of the return path from the DUT to the oscilloscope, i.e. the reverse propagation along the stress path and the metrology path (Fig. 4.1) has to be de-embedded. The same applies for the metrology path passed by the incident voltage pulse $V_{\text{inc}}(t)$. Since the incident pulse measured at the oscilloscope has not propagated along the stress path to the DUT yet, one has to embed the impact of the stress path post hoc.

Figure 4.5 exemplarily illustrates the de-embedding of the pick-off tee from the incident voltage pulse measured at the oscilloscope. The stress pulse enters the pick-off tee from the top (Fig. 4.5, bottom right picture). It is split and propagates across a high ohmic resistor ($R = 2.2\,\text{k}\Omega$) along the metrology path port of the pick-off tee to the oscilloscope. Having measured the voltage pulse $V_{\text{meas}}(t)$ at the metrology path port of the pick-off tee, the de-embedding technique aims to reproduce the waveform of the pulse before it has entered the pick-off tee $V_{\text{de-emb}}(t)$. As implied by the S-parameter measurement (Fig. 4.5, bottom left picture), the capacitive coupling of the pick-off traces (Fig. 4.5, bottom right picture, $\boldsymbol{C_{\text{parasitic}}}$) strongly enables higher frequencies to bypass the high ohmic resistance, leading to

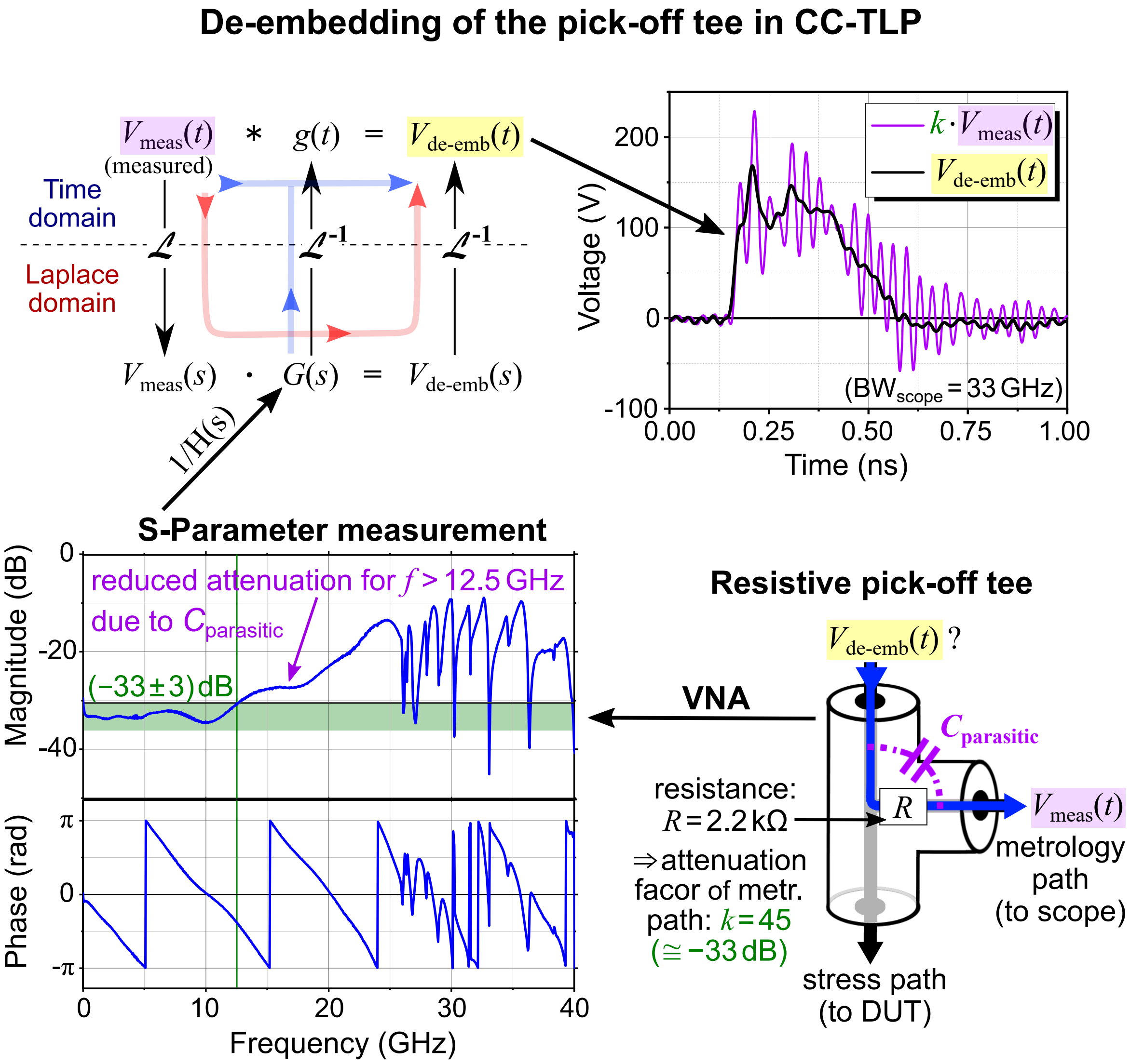

Figure 4.5 De-embedding of the pick-off tee from the measured voltage pulse.

a reduced attenuation for frequencies higher than 12.5 GHz. Thus, a simple multiplication of the measured signal by a constant pick-off attenuation factor $k \cdot V_{\text{meas}}(t)$ is not adequate to reconstruct the incoming waveform (Fig. 4.5, top right picture, purple waveform). Feeding the de-embedding algorithm (Fig. 4.5, top left picture) with the complex S-parameters measurement of the pick-off tee allows for almost complete elimination of the measured high frequency oscillations caused by the capacitive coupling of the pick-off traces $(V_{\text{de-emb}}(t))$ (Fig. 4.5, top right picture, black waveform). The metrology path of the pick-off tee was de-embedded from the measured signal.

4.3.3 Time shift calibration

After reconstruction of the pulses, the calculation of the stress current requires the exact superposition of the incident current pulse and its reflection at the DUT (Eq. (4.2)). In order to overlap both pulses numerically, the later arriving reflected pulse $V_{\mathrm{refl}}(t)$ is shifted by the time step Δt, corresponding to the additional path, towards the earlier arriving incident pulse $V_{\mathrm{inc}}(t)$. Thereby, Δt is twice the transit time of the stress path (Fig. 4.1).

The most straightforward method to determine the time shift Δt is to take the time difference between the rising edge of the incident and the reflected pulse. Depending on the specification of the edges (e.g. the point in time with the highest slope or at zero crossing), the time shift may spread in the range of some tens of picoseconds. That may not seem to be much, however, as the peak current of the stress is reached in the range of these superposed rising edges, this may have a significant influence on the resulting peak current [20]. Generally, the peak current of pulses with fast rising edges, i.e. with higher frequency content, tends to be more sensitive towards time shift variations. CC-TLP tests on an IC manufactured in a 0.25 µm BCD technology and assembled in a very small package with a footprint of only 7.5 mm^2 (Section 7.3) exemplifies how sensitive the peak value of the reconstructed current may responds to the value of the time shift Δt (Fig. 4.6).

A more sophisticated technique to determine the time shift Δt is to minimize the residual current I_{R}, while measuring an open-circuit [20]:

$$I_{\mathrm{R}} := \frac{\int_{t_1}^{t_2} |V_{\mathrm{inc}}(t) - V_{\mathrm{refl}}(t - \Delta t)|}{t_2 - t_1} \qquad \text{(continuous time)} \tag{4.3}$$

$$I_{\mathrm{R}} := \frac{\sum_{i=1}^{n} |V_{\mathrm{inc}}(t_i) - V_{\mathrm{refl}}(t_i - \Delta t)|}{n} \qquad \text{(discrete time)}$$

Time t_1 and t_2 has to be chosen in a way that the measured incident pulse $V_{\mathrm{inc}}(t)$ lies within the time interval $[t_1, t_2]$. Figure 4.7 shows the dependency of the residual current on the time shift Δt while measuring an open-circuit. In an open-circuit measurement, the residual stress current I_{R} should be near zero. Since only the time interval $[t_1, t_2]$ around the incident pulse is investigated (Eq. (4.3)), the residual current I_{R} rises when the reflected pulse is shifted into the integration area and almost vanishes for an optimum overlap of $V_{\mathrm{inc}}(t)$ and $V_{\mathrm{refl}}(t - \Delta t)$. This indicates the optimal time shift Δt. Note that the optimum time shift in contact with the DUT may need a small re-adjustment with respect to the time shift when measuring an open-circuit. A possible error indication for a miscalibrated time shift is a significant undershoot before the rising edge of the stress current. In this case, Δt is too large, i.e. the reflected pulse was shifted too much in time.

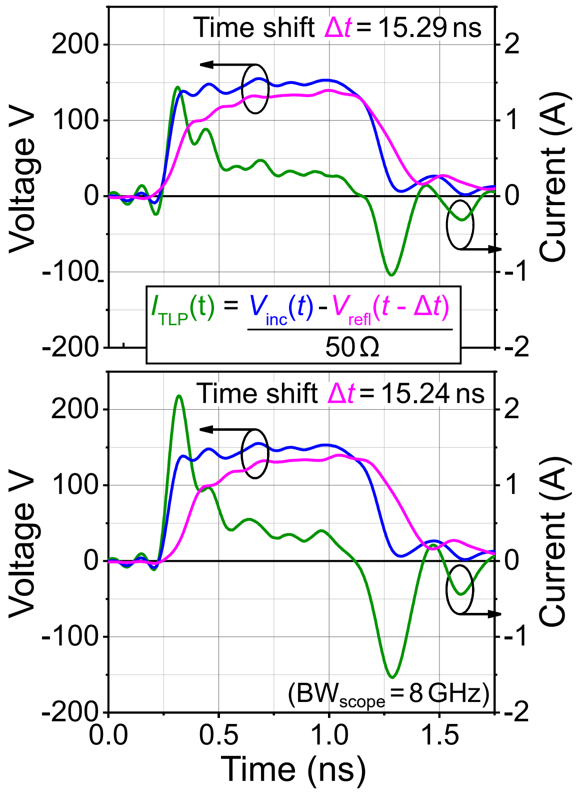

Figure 4.6 A deviation of the time shift Δt of only 50 ps, which can already result from the selection of the time shift determination method, can lead to a peak current variation up to 40%.

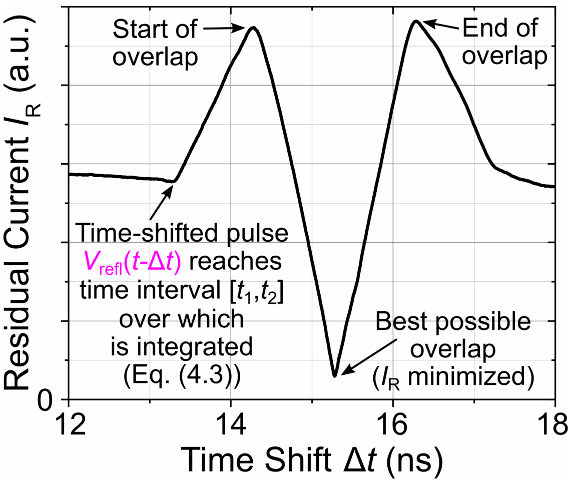

Figure 4.7 Dependency of the residual current I_R on the time shift Δt while measuring an open-circuit (Eq. (4.3)).

4.4 Adaption of the CC-TLP stress current waveform

One major distinguishing criterion between CDM and CC-TLP is their difference in source impedance. While CC-TLP is a well-defined 50 Ω system, CDM's source impedance is mainly given by the spark resistance of the air discharge, which shows a strong variation from pulse to pulse. The average source impedance of CDM $R_{S,CDM}$ is expected to be around 28 Ω [59]. Consequently, one may suppose that the longer RC-decay of CC-TLP's stress current, even if calibrated to the same peak current as CDM, could lead to a possible overstress of the DUT compared to CDM (Chapter 8). Hence, it is reasonable to tailor the CC-TLP stress current waveform to the one of CDM in order to induce the same failures.

For this purpose, the length of the charged TL within the (VF-)TLP pulse generator (Fig. 2.4) and with it the pulse width of the incident voltage pulse $V_{inc}(t)$ can be tuned. This leads to an adapted pulse width of the CC-TLP stress current $I_{TLP}(t)$ [18].

Secondly, the (RC-) decay of the stress current waveform can be controlled by varying the capacitive coupling of the DUT. This is achieved by changing the height h_{GP} of the CC-TLP GP above the DUT (Fig. 4.1) as described in Section 4.3.1. A decrease of the capacitive coupling between DUT and FCP, e.g. by increasing their distance by means of small PVC sheets (Fig. 7.22), showed a similar effect. One has to consider that a reduced RC-constant may also effectively result in a shorter CC-TLP pulse width.

The third and within the context of this thesis most important control mechanism is the possibility to tune the rise time t_{r} and with it the slew rate SR of the CC-TLP stress current (Chapter 6). The bandwidth BW of the test system indicates how well it preserves the fast rising edge of an input signal. Switching between components of different bandwidths or adding rise time filters into the stress path enables a variation of the rising edge of the CC-TLP stress current and its adaption to the rising edge of CDM (Eq. (6.2)). The possibility to vary the rise time of the CC-TLP stress current allows for the investigation of the influence of the rise time or slew rate on the peak current failure threshold and to draw conclusions on the triggering behavior of the ESD protection elements.

Another aspect to be mentioned is that the rectangular incident voltage pulse of CC-TLP $V_{\mathrm{inc}}(t)$ generates a bipolar stress current $I_{\mathrm{TLP}}(t)$, i.e. the DUT starts charging with the rising edge and subsequently discharges with the falling edge of the pulse (e.g. Fig. 4.6, green curve). Changing the length of the charged TL within the (VF-)TLP pulse generator (Fig. 2.4) helps to control the amplitude of the second pulse of opposite polarity, which occurs during the discharge of the DUT. CC-TLP's bipolar nature corresponds with the dual CDM stress procedure specified in all CDM standards [10, 34–36]. Nevertheless, the distinction of both stress polarities by suppressing the second CC-TLP pulse allows for the identification of the more critical stress polarity of an IC and supports the debugging of failure modes. Another possibility to suppress the peak current of the discharge would be to apply an incident pulse with a slowly falling edge instead of the rectangular pulse, as used by the alternative contact-mode test method low-Z CCDM [60] (Section 4.5.2). However, this would disable the application of CC-TLP on wafer level, as the resulting long-term charging or discharging of the large wafer capacitance is not consistent with the short CDM event anymore.

4.5 Alternative (contact-mode) testing methods in the CDM domain

The necessity of a reproducible test method in the CDM-domain becomes obvious when looking at the number of different CDM-like test setups popping up in the last two decades. All CDM test setup modifications and alternative contact-mode test setups pursue the objective of reproducing CDM failures with an increased reproducibility and repeatability in comparison to the default CDM setup (Section 5.1).

4.5.1 Modifications of the (FI)CDM setup

There are different attempts trying to maintain the principle of the default (FI)CDM setup (Section 2.1.3), i.e. maintaining the air discharge, but with some modifications in order to increase CDM's reproducibility and repeatability. They range from the purging of the test area with dry nitrogen to control the humidity during CDM testing to, for example, specific investigations to increase CDM's discharge reproducibility by pre-ionizing the air by means of radioactive substances [61].

Contact-first CDM

One recently developed technique is the so-called **Contact-first CDM** [62]. It uses a relay-triggered discharge of the DUT. Firstly, the pin or pad of the DUT is contacted by the so-called DUT contact pin. During being in contact with the pin or pad, the end of the DUT contact pin is contacted by the discharge pogo pin inside the discharge head. Thus, the spark can be relocated into an environmentally controlled chamber. This provides, besides an exact adjustability of the nitrogen atmosphere in the discharge chamber, a well-defined spark gap characteristic, which leads to an increased repeatability at lower precharge voltages. However, parasistics like an increased inductance caused by the extended pogo pin affect the CDM waveform. At present, only one contribution [62] provides verified measurement data using Contact-first CDM. Further correlation studies between CDM and Contact-first CDM for different technologies regarding failure thresholds are not available yet.

4.5.2 CDM-like contact-mode test methods

In order to significantly increase the reproducibility of a test method in the CDM-domain, one has to eliminate CDM's largely uncontrollable air discharge. **CC-TLP** [13, 14], which has been introduced around the turn of the millennium, is the pioneer in the field of alternative contact-mode test methods and the main object of investigation of this thesis (Chapter 4 and onwards).

CDM2 and WCDM2

More than 10 years later, a new CDM test method called **CDM2** [63] appeared, which charges and discharges the DUT through a controlled $50\,\Omega$ impedance environment. Similar to the CDM2 tester, which is deployable on package-level, a wafer-level CDM test setup called **WCDM2** [64] follows. However, the discharge of the package or wafer through a $50\,\Omega$ TL leads to an increased RC-constant with respect to CDM's source impedance, which is mainly given by the spark resistance $R_{\mathrm{S,CDM}} \approx 28\,\Omega$ [59]. In CC-TLP, the pulse width of the stress pulse can be controlled by tuning the length of the charged TL in the (VF-)TLP pulse generator (Fig. 2.4). In contrast, in CDM2 and WCDM2 one has only little impact on the stress pulse width as it depends, similar to (FI)CDM, on the capacitance of the DUT. Therefore, both methods tend to overstress the DUT or could address different, energy-related failure modes if the background capacitance of the DUT becomes too large [14, 18]. This might be a reason why there are less correlation studies available in the literature [65].

Low Impedance Contact CDM (Low-Z CCDM)

The source impedance is one main difference between CDM ($R_{\mathrm{S,CDM}} \approx 28\,\Omega$ [59]) and CDM-like contact-mode test setups like CC-TLP, CDM2 or WCDM2 (based on $50\,\Omega$ systems). Focused on the elimination of this impedance difference, **low-Z CCDM** [60] was introduced in 2015. It connects at least two parallel $50\,\Omega$ coaxial cables to the discharge path and optionally uses a surface mount resistor between inner and outer conductor near the pogo pin in order to reduce the impedance. This results in a better waveform matching to (FI)CDM. This is an advantage over CC-TLP, as the waveform has not to be adapted according to the package of the DUT. The mercury relay driven stress pulses show an increased peak current reproducibility in comparison to the discharges of (FI)CDM. Similar to the time-domain reflectometer principle used for CC-TLP (Section 4.1), low-Z CCDM is based on the Time-Domain Transmissometry (TDT) principle [66]. Instead of a rectangular pulse as generated by the (VF-)TLP pulse generator in CC-TLP, low-Z CCDM injects a step pulse with a slowly falling edge in order to suppress the peak current of the second pulse and thereby to enable unipolar stress testing. However, this aspect together with the relatively thick ($\sim 0.5\,\mathrm{mm}$), vertically downward-pointing pogo pin, which is a legacy from the CDM test head, disables low-Z CCDM to be used at wafer level like CC-TLP. In comparison to CC-TLP, the thick pogo pin earlier reaches its limit when testing highly complex layouts with very small sized, tight package pins, pads or balls. The connection of several coaxial cables and their transition to the pogo pin may also limit the bandwidth of the setup, which may become visible in high frequency measurements. By eliminating the air discharge, it is in any case essential to verify that the newly developed test method is still able to replicate real world CDM events. This is only possible by demonstrating the correlation with (FI)CDM through studies on different semiconductors and technologies. At present, around four years after its introduction, only one correlation study between low-Z CCDM and (FI)CDM for a 14 nm bulk Fin Field-Effect Transistor (FinFET) test chip [60] is available.

Due to the lack of test data and correlation studies with respect to (FI)CDM for almost all the newly developed CDM-like test methods — except for CC-TLP — a direct comparison is only possible to a very limited extent. The question remains still open, which test methods or modifications might co-exist, which will become a standard or standard practice and, in the long term, be able to complement or even replace the commonly used, but due to air discharge highly unreliable CDM testing method for product qualification, development and characterization.

Chapter 5

Peak current reproducibility of CDM and CC-TLP

In the following chapter, the peak current reproducibility of CDM and CC-TLP is compared. The poor reproducibility of CDM's air discharges with respect to the contact-mode test method CC-TLP leads to the usage of multizaps per pin and voltage level in CDM testing. This raises a conflict between the benefit when using multiple CDM stress pulses and the increased testing time. This chapter presents, to the knowledge of the author, the first statistical analysis of this conflict. Based on the high reproducibility of CC-TLP, the last part of this chapter exemplarily demonstrates the creation of a peak current map that can help to characterize the connection between different pins or pads of an IC.

5.1 Peak current distribution of CDM and CC-TLP

The CDM discharge current is highly dependent on several parameters like the precharge voltage, the approaching speed of the pogo pin, the surface conditions and cleanliness of the pogo pin and the device pins and environmental influences. Besides the limited precision and bandwidth of the CDM metrology chain, the main uncertainty is the barely controllable air discharge, which occurs when the pogo pin approaches the pin or pad of the DUT. Hence, the spark resistance and in turn the CDM peak current may vary for each pulse. In all CDM measurements performed within this thesis, the test chamber was purged with clean dry nitrogen to eliminate variations of the humidity during CDM testing (Fig. 2.3). Figure 5.1 compares the peak current distributions of more than 500 pulses performed by CDM testing (pink) and CC-TLP (green) on a BGA solder ball [19]. A low CDM precharge voltage of 110 V was used. The pulse voltage of CC-TLP was adjusted to provide similar peak currents as CDM. The peak current variations (Fig. 5.1, left pictures) are illustrated by means of boxplots (25th and 75th percentiles) with whiskers (5th and 95th percentiles). While the CDM peak current distribution scatters mostly between $\pm 30\%$ with many outliers in the negative section, the CC-TLP data is extremely reproducible with a variation of only $\pm 5\%$. It becomes evident that the peaks of both test methods approximately follow a normal distribution $\mathcal{N}(\mu, \sigma^2)$ (Fig. 5.1, middle pictures). Please note that the scaling in the middle pictures only refers to the discrete distributions and not to the continuous normal distributions functions. The skew of the CDM data (Fig. 5.1, top right picture) indicates that the CDM peak currents follow a continuous normal distribution, superimposed with an unknown distribution due to field emissions [19].

In accordance to the prevailing CDM standards, multizaps per pin and voltage level are allowed [10, 36] or even required [51] as a tool against the poor CDM reproducibility. The effect of using CDM multizaps is discussed in the following section.

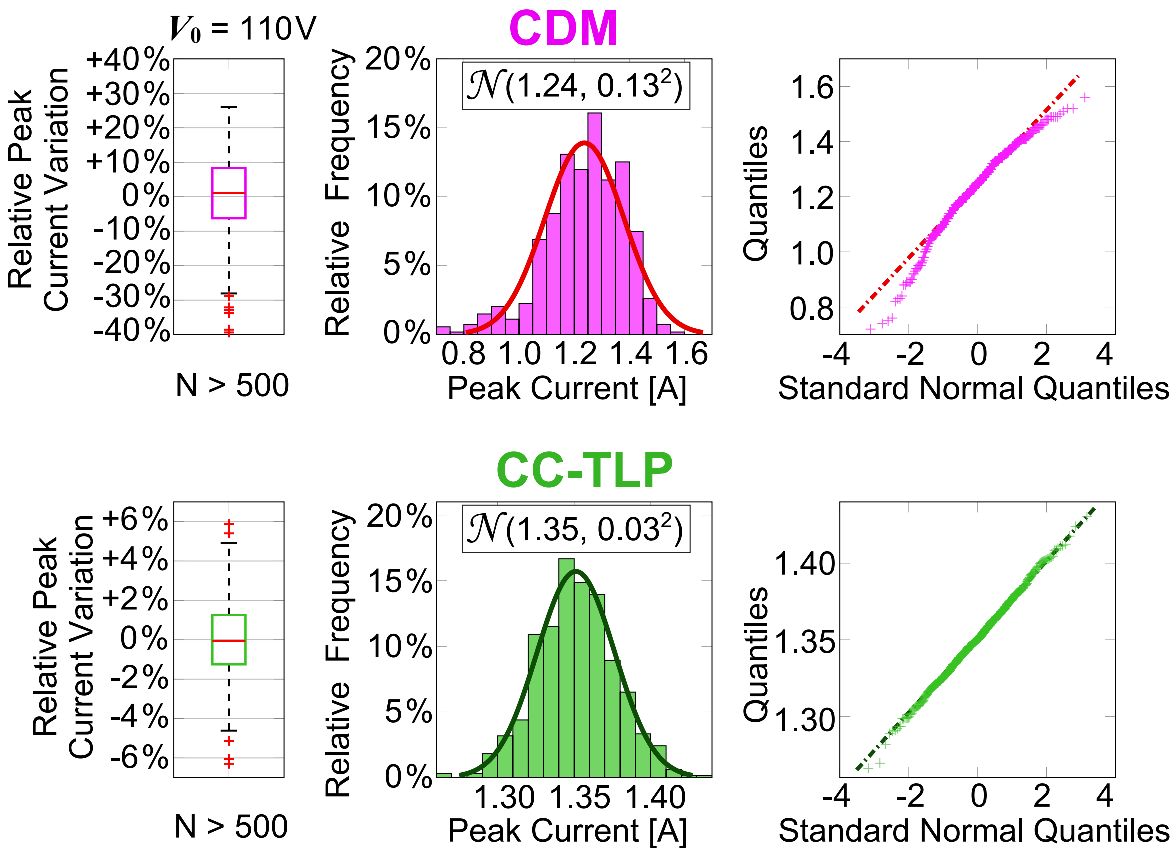

Figure 5.1 Statistics of the peak current distributions derived from more than 500 CDM and CC-TLP low voltage stress pulses on a BGA solder ball [19].

5.2 Usage of multiple CDM stress pulses

The poor reproducibility of CDM directly leads to the usage of multizaps per pin and voltage level. Unless the waveform of each single zap is monitored and runt pulses are repeated, multiple zaps help to reduce the impact of accidental runt pulses. This decreases the sensitivity towards outliers that do not reach the nominal peak current level and thus increases the possibility not to produce false pass results. In all the CDM tests discussed in this thesis, three stress pulses per pin and voltage level were used. For analysis, only the highest peak current I_p of each set of three stress pulses should be considered (hereinafter referred to as "Maximum-of-three-pulses" method). In case of no DUT failure, I_p was the highest stress peak current of the set below the current failure threshold. Hence, it marks a lower limit for the peak current failure threshold. On the other hand, if the DUT fails, the highest peak current of the set was definitively above the peak current failure threshold. This means I_p marks an upper limit for the peak current failure threshold.

However, there is a great disagreement concerning the appropriate number of pulses. CDM qualification tests according to JESD22-C101F [10] require at least one positive and one negative stress pulse per pin, whereas the ESD standard ANSI/ESD S5.3.1 [51] states three zaps per polarity. Their joint standard ANSI/ESDA/JEDEC JS-002-2014 [36] requires to apply at least one discharge per polarity to each pin and to test a minimum of three units. Generally, a statistical benefit that counteracts the poor CDM reproducibility conflicts with the testing time consumption for performing additional CDM pulses. The minimum number of CDM pulses per voltage level and pin that are required in order to provide pertinent information about the CDM robustness of a DUT depends on many different parameters like the number of tested devices (statistics), the variation of the gate oxide thickness of the devices, the failure mechanism and criteria (physical damage, functional failure, degradation), the existence of cumulative stress effects, etc. Consequently, it is not reasonable to generally define one minimum number of required CDM pulses that is applicable for all devices, even if this number is experimentally substantiated with some tested examples [67]. If the discharge currents are recorded, which is not mandatory according to prevalent CDM standards, a direct reaction only on missing or runt pulses could partially also be conceivable. This study takes a completely different approach by directly investigating the root cause, the poor reproducibility of CDM. To the knowledge of the author, this is the first work that quantifies the statistical benefit of using multiple CDM pulses and provides the crucial information required for everyone to select the appropriate number of CDM zaps considering the conflict between reproducibility and minimum testing time consumption.

5.2.1 Experimental approach

The low voltage CDM distribution composed of more than 500 stress pulses at a BGA solder ball (Fig. 5.1) is replotted together along with the distribution that is obtained when only the maximum of three consecutive pulses (“Maximum-of-three-pulses” method) is considered (Fig. 5.2).

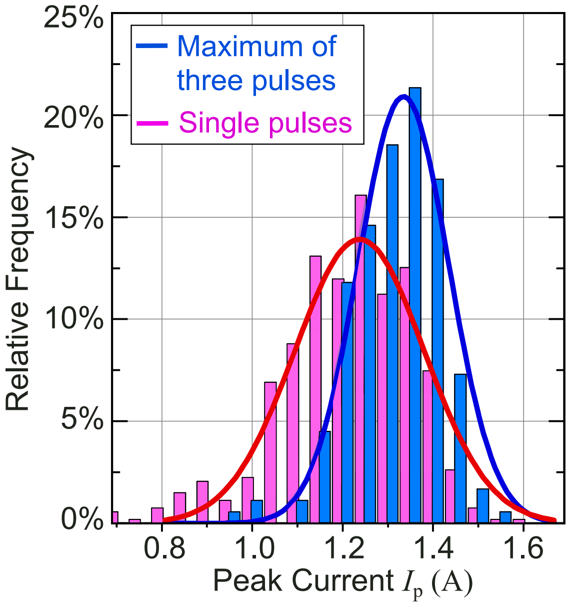

Figure 5.2 Low voltage CDM peak current distribution derived from more than 500 stress pulses on a BGA solder ball using all single pulses (pink) or the “Maximum-of-three-pulses” (blue) method. The scaling only refers to the discrete distributions and not to the continuous normal distributions functions.

In a first approximation, one can assume that the single CDM peak currents follow a normal distribution [19] (superimposed with an unknown distribution due to field emissions). The “Maximum-of-three-pulses” distribution also seems to follow a normal distribution $\mathcal{N}(1.33, 0.10^2)$ (blue), but shows a higher mean value and a smaller standard variation in comparison with the distribution when using every single pulse $\mathcal{N}(1.24, 0.13^2)$ (pink). The standard deviation of the peak current reduces by around **25%**. In the following section, these experimental results are used to verify the theoretical deviation of the statistical benefit when using multiple CDM pulses.

5.2.2 Theoretical approach

In order to better weigh the pros and cons of multiple stress pulses, this section offers a purely mathematical analysis [21]. As statistically verified in Section 5.1, an appropriate starting point is the assumption that the single CDM peak currents follow approximately a continuous normal distribution. In Figure 5.3, a normal distribution $f(I_p) = \mathcal{N}(\mu, \sigma^2)$ (red curve) with a standard deviation of σ around a mean value μ exemplarily represents a possible distribution of CDM peak currents I_p of one voltage level. Its cumulative distribution function $F(I_p) = \int_{-\infty}^{I_p} f(x)\,dx$ (red dashed line) gives the area under the probability density function $f(I_p)$ and describes the probability for a stress pulse to have a peak current less than or equal to I_p. This distribution is compared with the distribution that is obtained when the maximum of three pulses is considered $F_{\max(3)}(I_\mathrm{p})$. The cumulative distribution function $F_{\max(3)}(I_\mathrm{p})$ (blue dashed line) describes the probability that the maximum peak current of three stress pulses is less than or equal to I_p. Obviously, this is equal to the probability that all the three peak current values are less or equal to I_p. Consequently, following mathematical expression can be revealed:

$$F_{\max(3)}(I_\mathrm{p}) = F(I_\mathrm{p})^3 \tag{5.1}$$

One is now able to obtain $f_{\max(3)}(I_\mathrm{p})$ (blue line) by deviation of $F_{\max(3)}(I_\mathrm{p})$. In general terms, the CDM distribution using the "Maximum-of-n-pulses" method can be expressed by:

$$f_{\max(n)}(I_\mathrm{p}) = \frac{\mathrm{d}}{\mathrm{d}I_\mathrm{p}}\left(F_{\max(n)}(I_\mathrm{p})\right) \overset{(5.1)}{=} \frac{\mathrm{d}}{\mathrm{d}I_\mathrm{p}}\left(F(I_\mathrm{p})^n\right) = nf(I_\mathrm{p})F(I_\mathrm{p})^{n-1} \tag{5.2}$$

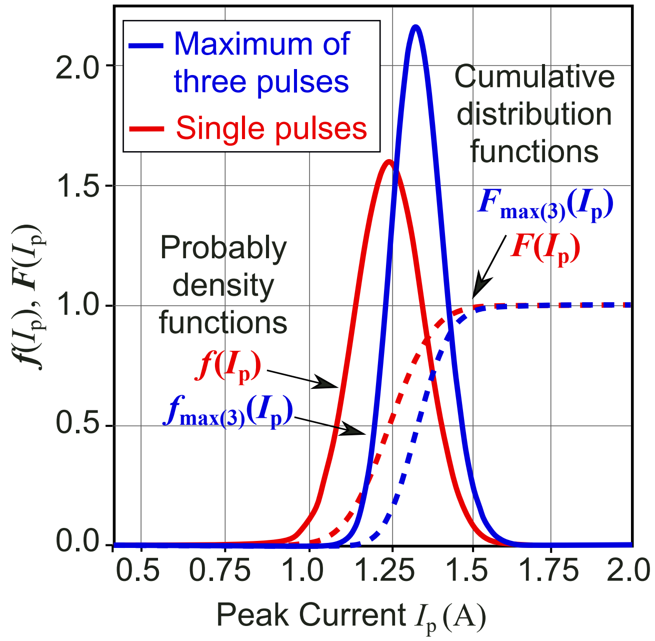

Figure 5.3 Theoretically derived peak current distribution of one CDM voltage level showing that the standard deviation when using the maximum of three pulses (blue) is around **25%** less than for using every single pulse (red).

The calculation shows that the probability density function $f_{\max(3)}(I_\mathrm{p})$ (blue curve) is also normally distributed around a higher mean value:

$$\mu_{\max(3)} = \int_{-\infty}^{+\infty} I_\mathrm{p} f_{\max(3)}(I_\mathrm{p})\mathrm{d}I_\mathrm{p} \approx \mu + 0.85\sigma \tag{5.3}$$

Having N sets of three stress pulses, the standard deviation of the sampled mean $\mu_{\max(3)}$ is given by $\sigma_{\max(3)}N^{-1/2}$ [68], where $\sigma_{\max(3)}$ stands for the standard deviation of the peak currents when using the "Maximum-of-three-pulses" method.

The benefit of using the "Maximum-of-three-pulses" method instead of single pulses is that the standard deviation of its distribution $\sigma_{\max(3)}$ reduces to 0.75σ:

$$\sigma_{\max(3)} = \sqrt{\int_{-\infty}^{+\infty} (I_\mathrm{p} - \mu_{\max(3)})^2 f_{\max(3)}(I_\mathrm{p}) \mathrm{d}I_\mathrm{p}} \approx 0.75\sigma \tag{5.4}$$

This means that the "Maximum-of-three-pulses" method improves the CDM reproducibility by **25%** with respect of the standard deviation σ when using only one CDM pulse per pin and voltage level.

$$\Longrightarrow \quad \Delta\sigma_{\max(3)}/\sigma \approx \mathbf{0.25} \tag{5.5}$$

This result perfectly fits with the measured reduction in standard deviation in the experimentally approach (Section 5.2.1). Using the maximum of **two**, **five** or **ten** pulses would decrease the peak current variation by **17%**, **33%** or **41%**. On the left-hand axis, Figure 5.4 displays the relation between **the average reduction in peak current variation** $\Delta\sigma_{\max(n)}/\sigma$ and the number of pulses n when using the "Maximum-of-n-pulses" method instead of every single pulse (●). The experimentally obtained results for $n = 2, 3$ (Section 5.2.1) (**✕**) perfectly match the analytically derived results (e.g. Eq. 5.4). Based on the law of error propagation, the error bars in Figure 5.4 represent the precision of the Gaussian function fit to the measured distributions. The non-negligible size of the error bars is mainly owed to the "relatively" small number of measured stress pulses (~ 500). Hence, instead of measured peak currents, the distribution of a large amount of artificially generated, normally distributed random numbers (~ 100000) were used to verify the theoretical approach for a higher number of multizaps ($n > 3$).

As statistically expected, the average improvement of standard deviation $\Delta\sigma_{\max(\mathrm{n})}/\sigma$ progressively decreases with every additional pulse (Fig. 5.4, ●). Let t_0 be the default time which is required to perform a CDM test on a device when using only single pulses. If one neglects the preparation time needed for the package alignment in the beginning of every test, the additional testing time when using the "Maximum-of-n-pulses" method $\Delta t_{\max(n)}$ would increase almost linearly with the number of pulses n. This fact in combination with the quantification of the statistical benefit when using multiple CDM pulses provides information about the **average reduction in peak current variation per additional testing time** $(\Delta\sigma_{\max(n)}/\sigma)/(\Delta t_{\max(n)}/t_0)$ (Fig. 5.4, ◆, right-hand axis). While this quantity is, for instance, slightly above 16% for $n = 2$, it reduces to 12% for $n = 3$. This leads to the result that the ratio of standard deviation improvement to additional testing time $(\Delta\sigma_{\max(n)}/\sigma)/(\Delta t_{\max(n)}/t_0)$ increases by more than **25%** for two instead of three CDM

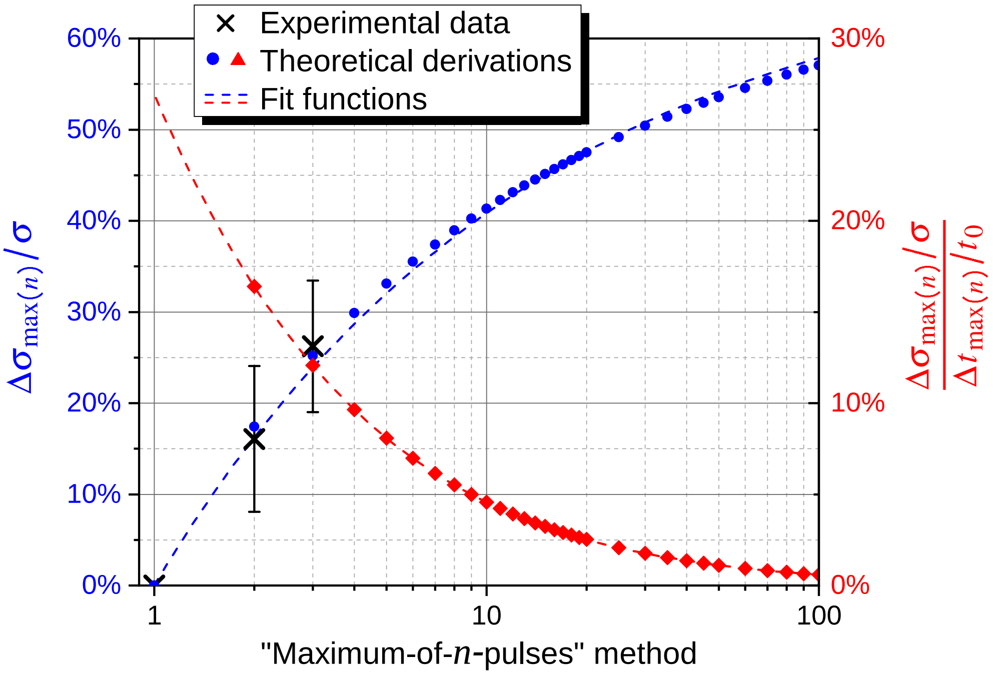

Figure 5.4 Average reduction of CDM's peak current standard deviation $\Delta\sigma_{\max(n)}/\sigma$ and average reduction of CDM's peak current standard deviation per additional testing time $(\Delta\sigma_{\max(n)}/\sigma)/(\Delta t_{\max(n)}/t_0)$ when using the "Maximum-of-n-pulses" method instead of only single pulses, including experimentally obtained data (✕ with error bars) as well as the results from the theoretical approach (● and ◆). The fit function (blue dashed line) can be described by $\Delta\sigma_{\max(n)}/\sigma \approx 0.7(1-n^{-0.385})$, with $n \in \mathbb{N}$.

pulses per pin and polarity. Thus, gaining a **17 %** improvement of the highly required CDM test accuracy $\Delta\sigma_{\max(\mathrm{n})}/\sigma$ by using the "Maximum-of-**two**-pulses" method could be a rational compromise in the standardization debate on the usage of either three [34, 35] or at least one CDM pulse [10, 36] per pin and polarity. However, this conclusion is only one possible interpretation of the results. Depending on the desired improvement of CDM reproducibility and the willing to invest additional testing time, the combination of both graphs depicted in Figure 5.4 should fill in the missing gaps in the required knowledge for everyone to weigh up and to decide about the appropriate number of CDM pulses.

Nevertheless, it is always important to consider that the number of pulses might be a potential critical stress parameter. If the failure mechanism is subject to cumulative stress effects as for the failing pn-junction damage investigated in Section 7.2.3 [5], the "Maximum-of-n-pulses" method might have an influence on the degradation and ultimately on the failure threshold. Thus, a consistent classification and a reliable correlation between CDM testers requires a clear specification of the number of stress pulses per pin and voltage level.

5.3 Creation of a peak current map

The high reproducibility of CC-TLP provides alternative application possibilities. As demonstrated in [22], CC-TLP measurements can help to characterize the connection between different pins or pads of an IC, for example to identify different types of ground nets of an IC (Section 7.4.1). By equally stressing all pins with a constant low CC-TLP voltage, the charge sourcing capabilities of the connected domains are measured. Figure 5.5 illustrates the resulting CC-TLP color-coded peak current map and a corresponding map generated by CDM with a constant low precharge voltage. As expected, the CC-TLP data are much more consistent for the different types of pins and do clearly identify the different types of ground nets (labeled with 1, 2, 3).

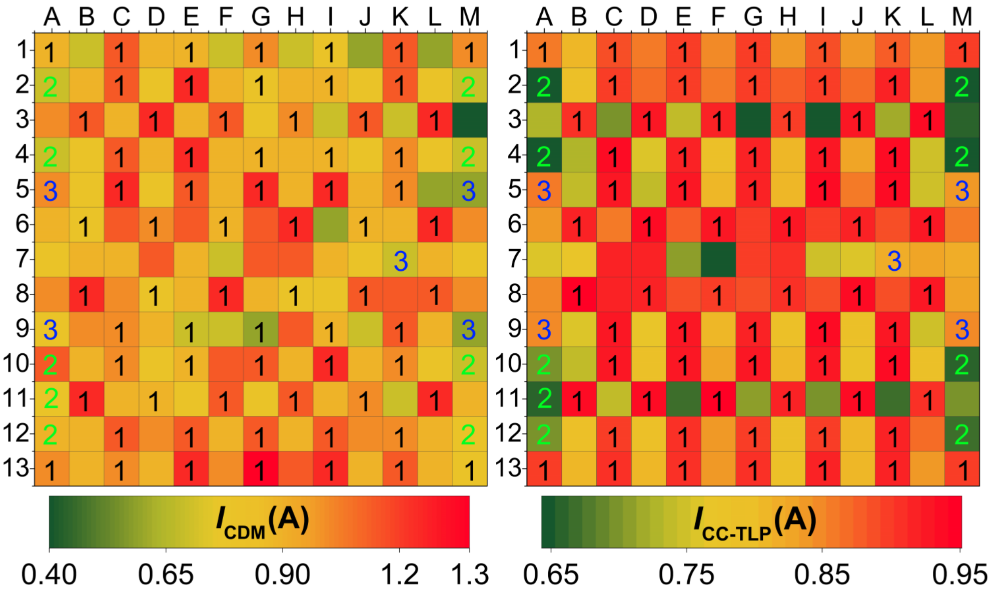

Figure 5.5 Peak current map of the chip measured by CDM (left) and CC-TLP (right) representing the CDM test condition TC 85 [36] on all pins. GND pins of different power nets are labeled with 1, 2, 3.

Chapter 6

Test system characterization

This chapter provides a brief overview over the bandwidths of the components used for the CDM and CC-TLP measurement setups in this dissertation. Furthermore, a newly developed electrostatic surface potential scanning procedure (ESPSP) is demonstrated. All three procedures (CDM, CC-TLP and ESPSP) were operated on the full-custom modular ATIS M-CDM3 test system, which was developed in the course of this dissertation.

6.1 Characterization of the CDM and CC-TLP test system

By performing S-parameter measurements by means of a VNA, the transfer function of all the used components was obtained. The complex transfer function fully describes the spectral reflection (S_{11}, S_{22}) and transmission (S_{12}, S_{21}) for any incoming signal (Section 4.3.2).

6.1.1 RF performance analysis methodology

The bandwidth BW of a component indicates how well it preserves the fast transition of an input signal. It is usually expressed by the frequency for which the spectral signal of the transfer function has reduced by half, i.e. for which frequency it falls below the -3 dB threshold [45]. The following formula relates bandwidth BW and rise time t_r for ideal step pulses in non-dispersive systems [69]:

$$t_\mathrm{r} \cong \frac{k}{BW}, \qquad k \approx \begin{cases} 0.35 & \text{, if } f_\mathrm{scope} \leq 1\,\mathrm{GHz} \\ 0.35 - 0.45 & \text{, if } f_\mathrm{scope} \geq 1\,\mathrm{GHz} \end{cases} \tag{6.1}$$

The rise time t_r is defined as the time that the signal takes to rise from 10% to 90% of its step height. Relation (6.1) can be used as a common rule of thumb to estimate the shortest possible rise time of CDM's and CC-TLP's stress current waveforms with respect to the bandwidth of the test system. The total bandwidth BW_System of a system is limited by the bandwidth of all of its components, i.e. the cables, the CDM or CC-TLP probe, the pick-off tee etc. Mathematically, the total bandwidth is specified by the bandwidth of the product of all transfer functions. Simplified, the total bandwidth can also be estimated by the bandwidths of the individual components [45]:

$$BW_\mathrm{System} \cong \frac{1}{\sqrt{\frac{1}{BW^2_\mathrm{Cables}} + \frac{1}{BW^2_\mathrm{Pickoff}} + \frac{1}{BW^2_\mathrm{Scope}} + \ldots}} \tag{6.2}$$

Accordingly, based on Equation (6.1), an assessment of the rise time of the system t_rSystem is given by:

$$t_\mathrm{rSystem} \cong \sqrt{t^2_\mathrm{rCables} + t^2_\mathrm{rPickoff} + t^2_\mathrm{rScope} + \ldots} \tag{6.3}$$

A key factor for the ESD susceptibility of some components or structures is the slew rate SR of the rising edge, which is generally defined as the mean change of current (or voltage) per time unit. SR is equivalent to the absolute change of current (or voltage) during the rise time $\Delta I_{10\%\text{-}90\%}$ per rise time:

$$SR := \overline{\left(\frac{\mathrm{d}I(t)}{\mathrm{d}t}\right)} \equiv \frac{\Delta I_{10\%\text{-}90\%}}{t_\mathrm{r}} \tag{6.4}$$

For a reproducible test system like CC-TLP, the rise time of the waveform is, in contrast to the slew rate, independent on the pulse voltage or stress current amplitude.

6.1.2 Bandwidth of used CDM and CC-TLP equipment

The following section deals with the frequency response of the components used in the CDM and CC-TLP measurements in the context of this thesis. The gained information are important to interpret measured failure thresholds, especially in cases where the current slew rate is a critical stress parameter (Section 7.3 and 7.4).

The modular test system

In the course of this dissertation, the full-custom modular ATIS M-CDM3 test system was developed. It is able to operate both, FICDM testing on package and CC-TLP on package and on 200 mm wafer level. Containing a XYZ-motion system with enormous mechanical precision (4.88 nm) and repeatability, the adaptable tester owns humidity control for CDM measurements and is able to check the failure criterion between stress pulses by means of DC-leakage testing. Additionally, the newly developed surface potential scanning method (ESPSP), which uses a non-contacting electrostatic voltmeter, can be employed (Section 6.2). Most of the tests included in this thesis were performed on the M-CDM3 system.

The CDM and CC-TLP test head

The frequency response of the CDM and CC-TLP test head is represented by the S_{11}-parameter measured by means of a VNA and illustrated in Figure 6.1.

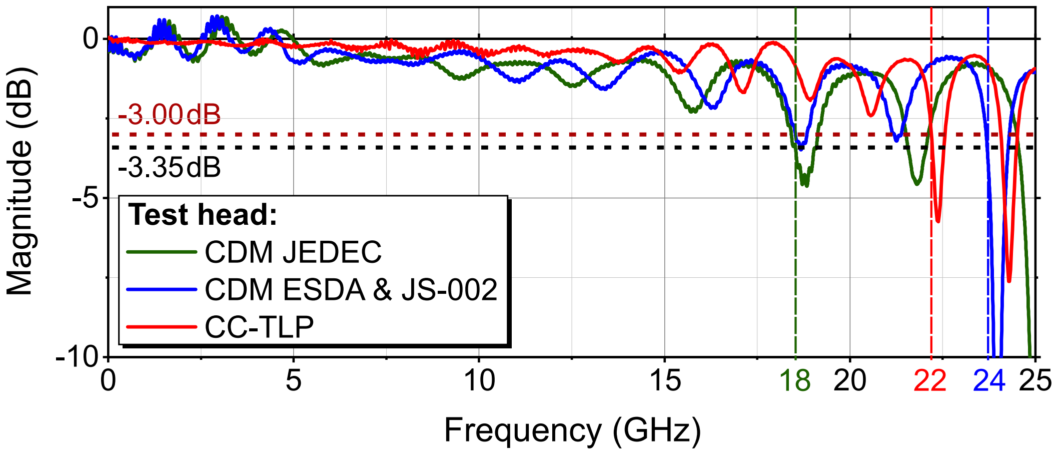

Figure 6.1 Measurement of the reflection coefficient S_{11} of the CDM and CC-TLP test head in open-circuit (no contact). The positive values of S_{11} for frequencies below 5 GHz refer to a measurement artifact based on the highly sensitive VNA cables and are regarded as meaningless and unphysical.

The CC-TLP test head (Fig. 6.1, red curve) has a flat -3 dB frequency response up to 22 GHz (Fig. 6.1, dark red dashed line). The pogo pin and the GP of the CDM discharge head are connected by a 1 Ω disc resistor (Figure 2.2), serving as a current sensor between inner and outer conductor. This corresponds to a reflection coefficient of -0.35 dB[1]. Consequently, the effective bandwidth to be exceeded by the CDM discharge heads equals -3.35 dB (Fig. 6.1, black dashed line). In the CDM measurements according to the standard JESD22-C101F [10]

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[1] Ideal response: $S_{11}\left[\text{dB}\right] = -20\log\left|\frac{V_{\text{refl}}}{V_0}\right| = -20\log\left|\frac{Z_2-Z_1}{Z_2+Z_1}\right| = -20\log\left|\frac{1\,\Omega-50\,\Omega}{1\,\Omega+50\,\Omega}\right| \approx -0.35$

(Fig. 6.1, green curve), a discharge head free of ferrites and tuning cavities was employed, which well exceeds a S_{11}-bandwidth of 18 GHz. The CDM test head used for the ESD standard ANSI/ESD S5.3.1 [51] and ANSI/ESDA/JEDEC JS-002-2014 [36] (Fig. 6.1, blue curve) shows a flat response up to 24 GHz with a momentary approach of the -3.35 dB bandwidth at around 18 GHz and 22 GHz.

The CC-TLP pulse source

For the CC-TLP tests, a commercial (VF-)TLP generator with a minimum rise time of 100 ps is used per default. For special investigations, a fully customized ultra-fast home build (VF-)TLP pulse generator with a minimum rise time of only 30–40 ps was deployed. In order to generate pulses with even shorter rise times, a wetted reed relay with an improved performance was designed in the context of this dissertation. It provides a very flat frequency response of both opened reeds up to 22 GHz, with one resonance peak at 11 GHz. Using Time-Domain Reflectometry (TDR) and VNA measurements, the distinct capacitive behavior of the closing blade of the reed relay was identified as cause of the initial fast rising edge and the typical, initial overshoot of the rectangular pulse. By means of local diameter variations of the surrounding aluminum cylinder, the impedance mismatch of the pulse path was eliminated eventually leading to a reduction of the overshoot of the rising edge.

The CC-TLP pick-off tee

The stress path of the 50 Ω SMA wideband voltage pick-off tee connects the (VF-)TLP generator with the DUT (Fig. 4.1). Both, the incident $V_{\mathrm{inc}}(t)$ and the reflected voltage pulse $V_{\mathrm{refl}}(t)$ are split by means of a voltage pick-off tee, which is located between the pulse generator and the CC-TLP probe and propagate along the metrology path to a single shot oscilloscope (Fig. 4.1). A resistor within the metrology path determines the attenuation factor (Fig. 4.5, bottom right picture) that is applied to the voltage pulses traveling to the oscilloscope (type A: 33 dB, type B: 26 dB, type C: 22 dB). Figure 6.2 depicts the transmission coefficients (S_{21}) of the pick-off's stress and metrology paths used within this thesis. The capacitive coupling of the pick-off traces (Fig. 4.5, bottom right picture) leads, especially for high frequencies, to a reduced attenuation along the metrology path. The colored areas in Figure 6.2 mark a range of ±3 dB around the specified attenuation. The exceedance of the ±3 dB range already for low frequencies indicates the importance of post measurement corrections (Section 4.3.2). The pick-off tees that are used within this thesis

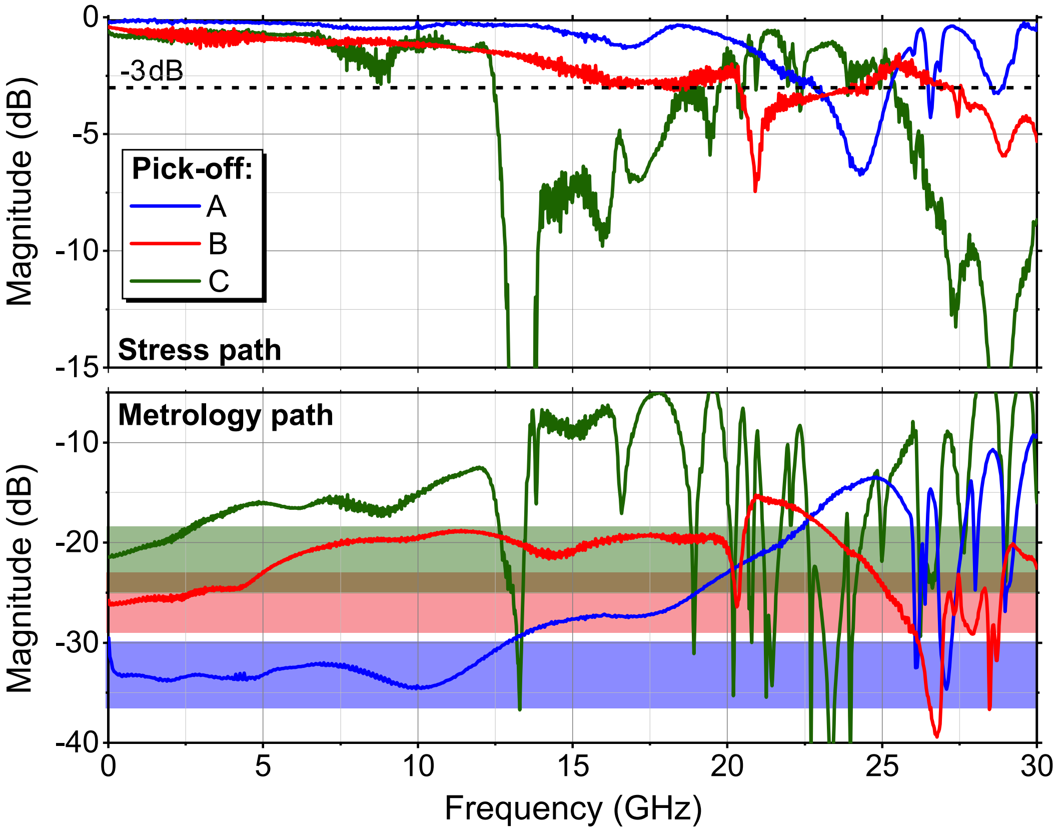

Figure 6.2 Measurement of the transmission coefficient S_{21} of three different pick-off tees along the stress and metrology path.

provide a -3 dB bandwidth from 13 GHz to 22 GHz in the stress path and a ±3 dB bandwidth from 4 GHz to 12 GHz in the metrology path.

The oscilloscope, SMA cables, connectors and attenuators

To obtain maximum resolution, a 33 GHz single shot oscilloscope (Keysight DSOX96204Q) with a sampling rate of 80 GSa/s was deployed for both, CC-TLP and CDM stress testing. For special investigations, the 63 GHz high performance oscilloscope channel with a sampling rate of 160 GSa/s was used. The impact of the high performance microwave cables (< 1 m) used for the CDM and CC-TLP setup is negligible (< 2 dB/m at 20 GHz [70]). All the other components used in the CDM and CC-TLP setup were specified to provide a bandwidth of 18 GHz and more.

Further comparisons between CDM and CC-TLP, for example regarding costs or the effort for maintenance and repair, are given in [12].

6.2 Characterization of the Electrostatic Surface Potential Scanning Procedure (ESPSP)

In the course of this dissertation, an innovative method of scanning the surface potential across a DUT was developed (Fig. 6.3). The procedure helps to gain a deeper insight into the electrostatic behavior of the DUT and provides required information for ESD-relevant countermeasures. Particularly suitable for scanning are e.g. flexible electronics like COFs [5] (Section 7.2.1) or the highly chargeable cable connectors, which were identified to be the root cause for the increased failure rate in the study described in Section 7.4.2 [20]. In order to charge the DUT before the scan, an air ionizer, which usually emits positively and negatively charged ions to neutralize static charge on insulated surfaces, was readjusted to provide only one type of charge carriers. Employing a Monroe non-contacting electrostatic voltmeter with a chopper sensor in combination with the full-custom modular ATIS M-CDM3 test system, a lateral resolution of a few millimeters and a potential resolution of 1 V was achieved. By means of several test studies, other scanning parameters and their influences on the outcome like the aperture time (< 50 ms), aperture angle of the observation cone (64°), probe-to-surface spacing, underlying materials etc. were investigated and optimized. During scanning the foil line-by-line, the data, representing the charge distribution on the scanned DUT, is processed and depicted by means of a contour plot in real-time (Fig. 7.1 and Fig. 7.15).

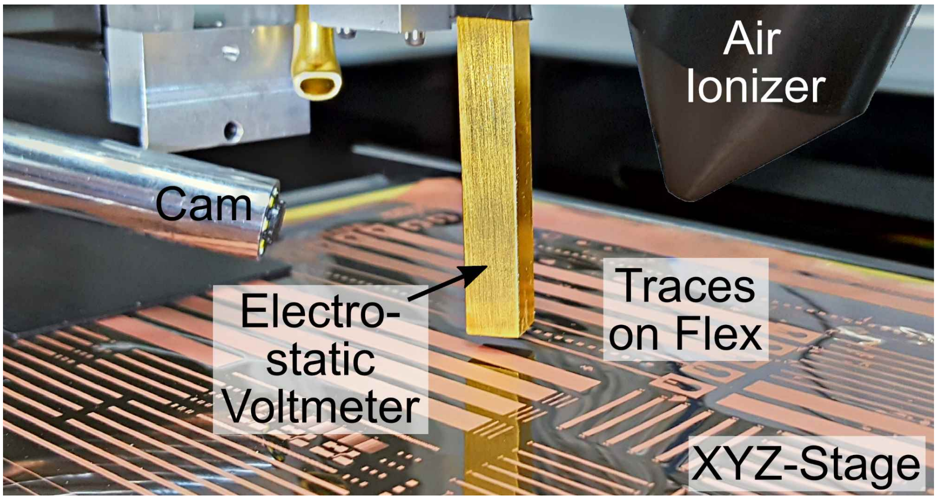

Figure 6.3 Electrostatic Surface Potential Scanning Procedure (ESPSP) by means of a non-contacting electrostatic voltmeter used to gain information of the charge distribution on different test traces printed on a flexible foil.

Chapter 7

Correlation studies between CDM and CC-TLP

Like (FI)CDM testing, CC-TLP needs to reproduce exactly the electrical and physical failure signatures of real world CDM events. In addition, for a correlation between CDM testing and CC-TLP, both test methods have to provide equal peak current failure thresholds, i.e. tested devices have to fail at about the same peak stress current within the $\pm 20\%$ tolerance of the current CDM standard. This chapter gives an overview of previous CDM to CC-TLP-correlation studies and presents the CDM/CC-TLP correlation studies that have been performed in the course of this thesis. The studies reveal critical stress factors that have, besides the peak current, a direct influence on the failure threshold.

7.1 Overview of CDM/CC-TLP correlation studies

Starting with an "ancient" 3 µm NMOS technology, the correlation between CDM and CC-TLP was already investigated for 90 nm and 130 nm CMOS technologies, at packaged device and at wafer level in several studies in the last decades [15–19]. All of these studies demonstrated an excellent correlation between CDM and CC-TLP in terms of the peak current failure thresholds and failure signatures.

The research in the course of this dissertation extends previous investigations through a CDM/CC-TLP correlation study of a pn-junction failure on a large, flexible 0.35 µm Chip-on-Flex (COF) assembly [5] (Section 7.2) and two slew rate sensitive ICs from modern semiconductor technologies: one with a tiny package manufactured in a 0.25 µm BCD technology [20, 21] (Section 7.3), and one 28 nm ultra-high-speed (25 Gbps) CMOS IC for network applications [22] (Section 7.4). A recent CDM/CC-TLP study on a GGNMOS device with an unusual window failure distribution demonstrated a similar influence of the current slew rate on the peak current failure threshold [71]. In the course of this dissertation, an excellent correlation between CDM and CC-TLP could also been shown on an ultra-high-speed ($>$ 50 Gbps) cutting-edge technology manufactured in a single-digit nanometer technology, which highlights the capability of the CC-TLP test method for future applications. These experimental studies are supported by a parameter simulation study, which investigates the CDM/CC-TLP correlation from a theoretical point of view [21] (Chapter 8).

7.2 CDM to CC-TLP-correlation of a large Chip-on-Flex (COF) assembly

Critical stress parameters: Pulse energy and multizaps

Based on correlation study [5], air discharge CDM and contact-mode CC-TLP was compared for the first time for a large Chip-on-Flex (COF) assembly, e.g. used for Internet of Things (IoT) applications. The correlation of CDM and CC-TLP on flex is examined with CC-TLP at wafer level regarding peak current, other stress parameters and their failure thresholds together with the failure signatures. There are at least five aspects, which make this study so important:

Firstly, to the knowledge of the author, this work is one of the first to analyze the specific ESD issues of COFs. This thesis will show that flexible electronics with electrically insulating foil substrates are highly chargeable and provide new challenges concerning ESD. **Secondly**, the flexible substrate with its long copper traces exceeds under test significantly the size of standard packages. Here, one key question is the feasibility of CDM and CC-TLP stress tests on the COF assembly, as the GP does not overlap the sensitive chip (Fig. 7.2). This brings up new aspects regarding CDM testing and results should also be applicable for very large scale packages exceeding the size of the GP. **Thirdly**, the study investigates the impact of the electrically coupled traces on foil that are situated between pad and chip on the stress current (Fig. 7.2). For this purpose, the current waveforms were analyzed and the entire discharge environment including the chip was studied by means of simplified circuit simulations. This provides first insights into a very general question — namely, whether and how far the calculated stress current I_{TLP} at the contact of the CC-TLP needle with the pin or pad of the DUT (Eq. (4.2)) differs from the stress current, which eventually enters the chip after it was routed through the package, i.e. through e.g. traces, substrate or bonding wires. **Fourthly**, for the first time a CDM/CC-TLP correlation of a pn-junction failure, and not of a CDM typical gate oxide rupture (Section 2.1.1 and 2.1.2), was investigated. This directly leads to the **fifth** and most important aspect for this dissertation: The energy content of the stress pulse as well as the number of stress pulses had a direct influence on the failure threshold of the tested COF assemblies. Thus, the CDM/CC-TLP correlation could be established according to impulse energy and multi-zap wear-out effects rather than peak current.

7.2.1 Chargeability and ESD risk evaluation of the COF assemblies

The development of a process to enable fabrication and integration of ultra-thin silicon in foils is one of the milestones in flexible electronics, which has opened the door for various applications like flexible displays, wearables and foldable electronics in recent years. Specific advantages like light weight, flexibility and foldability, lower costs, potential transparency and new application opportunities [72] have attracted the interest of numerous electronics manufacturers. However, flexible electronics also imply an increased and specific demand for both mechanical and electrical reliability. While several groups are investigating the mechanical reliability of COF samples [73], the attention received by ESD analysis of COFs is rather minimal. To the knowledge of the author, this study [5] is the first to analyze the specific ESD issues of COFs. The bendability of these components requires mechanical support for processing and as such yields a higher risk of triboelectric charging. Electrically insulating substrate materials like Polyimide (PI) enable the storage of a significant amount of charge on their surface and may easily charge up to hundreds of volts. In its application as a flexible and bendable substrate, the charging of the foil can hardly be avoided. The same applies to the handling of the COFs during ESD tests. Even if one assumes a non-charged foil after its roll-to-roll production process, the challenge arises when the entire roll must be cut into individual foils afterwards.

Hence, in order to assess the risk of ESD, the charging of the foil as a critical aspect concerning ESD on COFs was analyzed [74]. For this purpose, an innovative method of scanning the surface potential across the polymer substrate with its copper traces was developed (ESPSP, Section 6.2). Only if all necessary ESD precautions are precisely applied, is it possible to keep the surface potential of the foil down to levels in the region of some tens of Volts (Fig. 7.1, Unstressed foil). The PI foil is extremely sensitive to triboelectric effects (Fig. 7.1). To demonstrate this effect, sticking and pulling off an adhesive strip (Fig. 7.1, Adhesive strip) or applying electrical stress on the left side of the foil (Fig. 7.1, Electrical stress) can lead to voltages below $-800\,\mathrm{V}$ on this side. According to the triboelectric series [75], PI has a charge affinity of about $-70\,\mathrm{nC/K}$. This explains why it accumulates a strong negative charge when it is rubbed against most other materials.

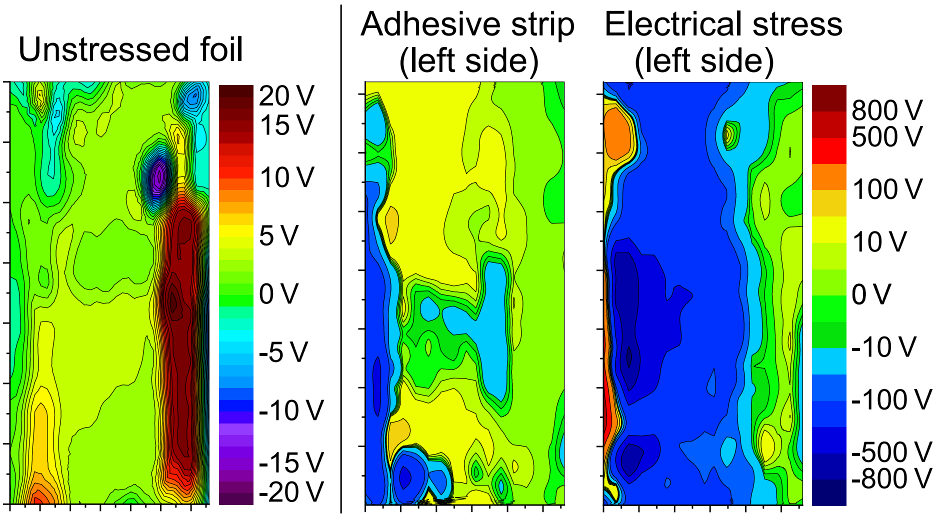

Figure 7.1 Electrostatic surface potential on foil measured by the ESPSP (Section 6.2). The automated scanning of 34 vertical lines per picture generated the contour plot.

Once the foil is charged, the trapped charge remains and decays very slowly unless an air ionizer is used. In the meantime, the foil is surrounded by electrostatic fields, which may influence or separate charge carriers in other parts. This further complicates the prevention of ESD events. The electric fields might also lead to a charge displacement in the copper traces on foil, which would likely have an effect on ESD testing. Overall, the high chargeability of the foil is one main aspect that shows the risk to COFs concerning ESD as well as the difficulty of performing ESD tests on it.

7.2.2 Feasibility of CDM/CC-TLP stress tests on the COF assembly

To investigate the ESD discharge of the COF, CDM and CC-TLP measurements were performed. For the stress testing, the CDM pogo pin or the CC-TLP probe needle contacts one of the pads at the edge of the flex, which has a number of passivated traces connecting to the pads/bumps of the flip chip. Figure 7.2 depicts the principle of the probing setup for the CC-TLP investigations. The particular challenge involved here is that the traces are longer than half the side length of the square CDM GP (32 mm) and the radius of the CC-TLP GP (25 mm). Thus, in both methods the GP and the chip do not overlap (Fig. 7.2). This implies that their capacitive coupling is very low and can only be induced by fringing fields. Hence, the configuration provides an unconventional way of performing CDM and especially

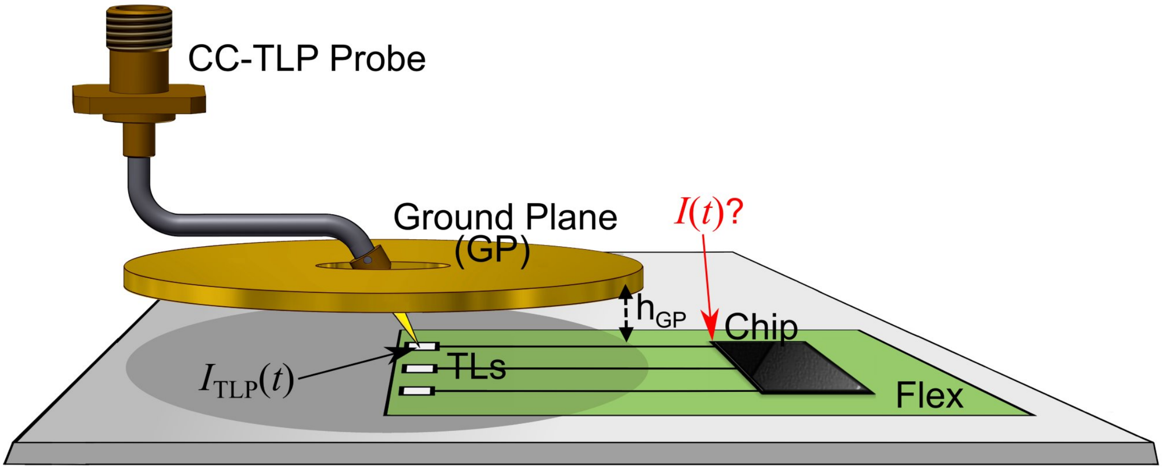

Figure 7.2 CC-TLP probing set up during stress testing on flex. The probe needle is in contact with the pad of one trace, which leads to the COF. For reasons of clarity, only three of many traces are illustrated.

CC-TLP tests, which could lead to irregular results. Nevertheless, this extreme case should also provide some generic insight into the probing of large-scale packages.

Circuit Simulations

In order to gain a better understanding of ESD tests on a COF technology, particularly the impact of the electrically coupled traces on foil on the stress current seen by the chip, it is advantageous to initially create a simulation model of the ESD event. This was realized by means of the Keysight (Agilent) ADS circuit simulation tool.

Simulation Model

Figure 7.3 illustrates the key components of the schematic CC-TLP simulation model on flex. In the CC-TLP simulation, the dataset of a real measured voltage pulse was imported and assigned to the pulse generator for the incident pulse. In the measurement as well as in the simulation, an attenuator behind the TLP source can optionally be used to reduce reflections. On the right side, a generic RC network models the complex IC with many inputs and narrow traces on flex that — in combination with the tester setup — can be looked at as Transmission-Lines (TLs). Optionally, some inductive elements can also be added in series. In addition, each of these TLs is capacitively and inductively coupled with two adjacent neighbors. For both stress methods, the pad to be contacted is positioned at the end of one of the TLs, which extend for several centimeters (Fig. 7.2). The TLs all lead in parallel to the flip-chip-on-flex interconnections.

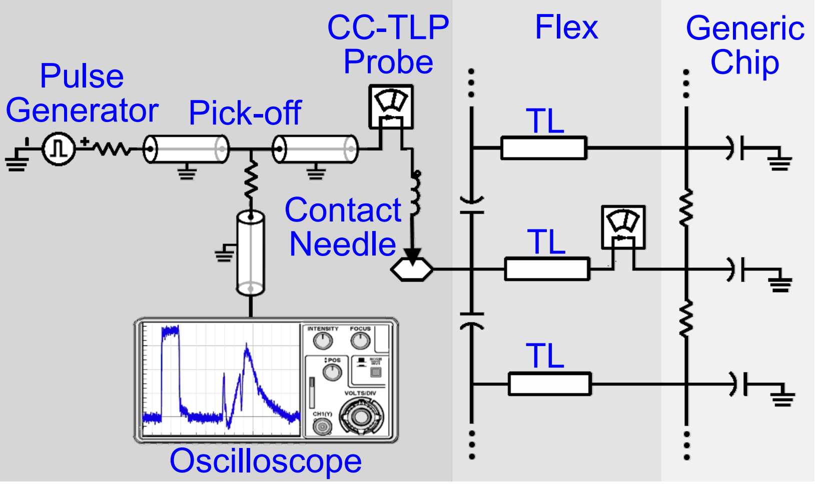

Figure 7.3 Applied lumped element model of the CC-TLP simulation setup on flex. The probe needle is in contact with one of the electrically and inductively coupled TLs of the COF assembly (Inductive coupling is left out to simplify the diagram).

The CDM simulation setup contains the same model for the COF. The model of the CDM tester is equivalent to the one in [76]. In the CDM simulation the whole chip, including all the TLs, is charged up before it is discharged through a 1 Ω disk resistor to the Ground Plane (GP). After making some measurements, it turned out that the COF circuit chosen for this study is highly sensitive to CDM and that the precharge voltage required to generate CDM failures is well below 100 V. A good fit between the simulation and the measurement was obtained when choosing an average resistance of 10 Ω [59] for the air discharge in a nitrogen atmosphere.

Impedance Extraction of the TLs

A significant difference between the CDM and CC-TLP setup is the characteristic impedance of the TLs. In CC-TLP, the round GP establishes the return path and is positioned directly above the TLs at a distance of $h_{\mathrm{GP}} = 500\,\mu\mathrm{m}$ by default (Fig. 7.2). In CDM, the square GP is, due to the length of the pogo pin, much farther away at a distance of around 3.5 mm. Here, the main coupling is formed by the FCP below the foil $C_{\mathrm{FCP\text{-}DUT}}$, which forms a capacitance with the GP $C_{\mathrm{FCP\text{-}GP}}$ (Fig. 2.2). The characteristic impedance of the TLs was quantified by a Time-Domain Reflectometry (TDR) step response measurement using a TDS8000 sampling oscilloscope. Together with the sampling rate, the rise time of the step generator (30 ps) determines the geometric resolution.

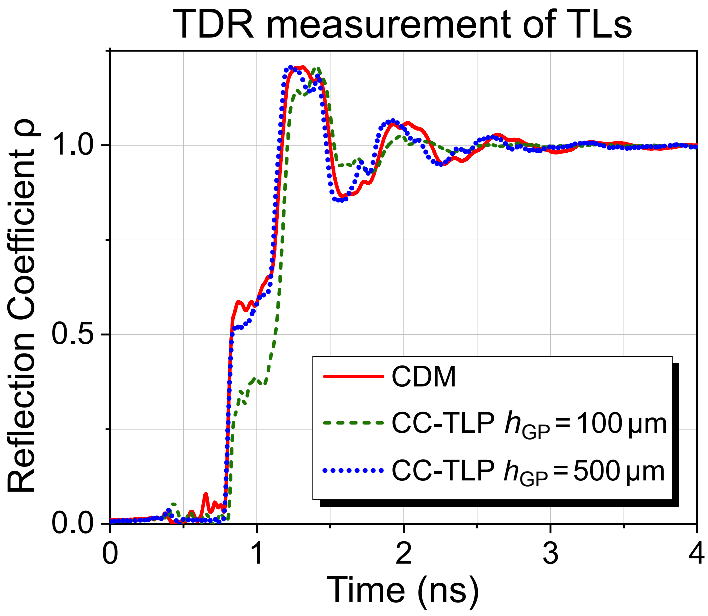

Figure 7.4 Reflection coefficients of copper strips on flex without chip measured by the TDS8000. The first step arises due to the impedance rise at the transition from the CDM pogo pin or the CC-TLP contact needle to the TL. The results were used to determine the characteristic impedances of the TLs for the simulation model. The curves for separation heights h_{GP} of 300 µm and 800 µm were left out to simplify the diagram.

During the TDR-measurement, the CDM and CC-TLP probe was in direct contact with the input pad of a TL on the flex board from which the chip was removed to generate an open termination at the end of the TL. In order to allow the measurement of the characteristics impedance change from the pogo pin to the TL, the 1 Ω disk resistor of the CDM probe was removed. Figure 7.4 illustrates the analysis of the TDR traces resulting in characteristic impedances of the TLs of 190 Ω for CDM and of around $\{100, 150, 160, 170\}\,\Omega$ for CC-TLP with separation heights of $h_{GP} = \{100, 300, 500, 1000\}\,\mu m$ between GP and flex. This relation can be explained by the fact that the characteristic impedance of a TL depends inversely on the capacitance per length. Because of the low capacitive coupling between the DUT and the GP in CDM, a decrease of the GP-foil distance from around 3.5 mm to 2.7 mm through a stronger tension of the spring-loaded pogo pin does not lead to any impedance change.

Transient Simulation Results

The TDR measurement provided the necessary parameters for the simulation models. In Figure 7.5, the simulated (red) and measured (black) waveforms are compared. Unknown simulation parameters, like e.g. of the generic IC, have been estimated and optimized by fitting the simulated curve to the measured one.

Generally, the simulated curves match the measured ones, which is an indication that the model and the choice of its parameters describe the system in a proper way. The wave-shaped curve of the CDM transient (Fig. 7.5, top left graph) shows the characteristic impact of the TLs on foil. The discharge current oscillates between the chip and the 1 Ω resistance of the

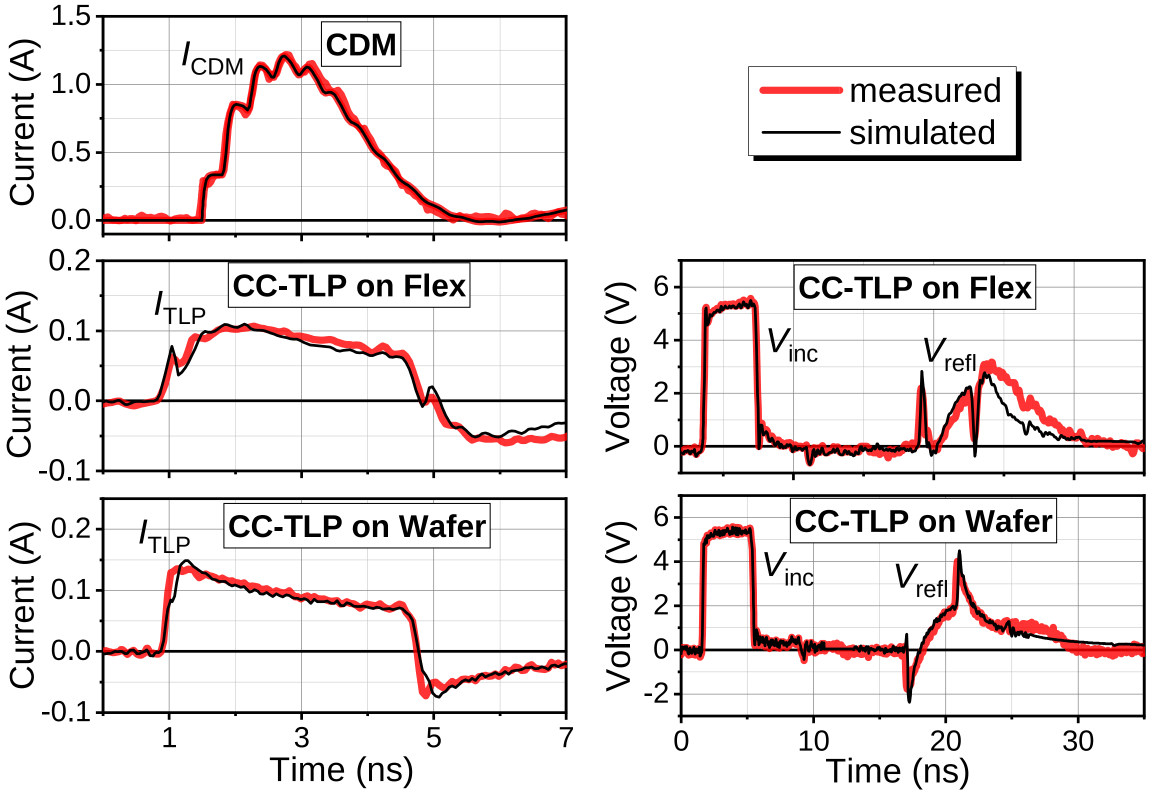

Figure 7.5 Comparison of measured and simulated transients of CDM and CC-TLP on flex and on wafer. The two curves on the right are voltage transients of the incident and the reflected CC-TLP pulse. The three curves on the left are the corresponding current transients plus the discharge current of a typical CDM pulse (on top).

CDM head, which leads to a ringing of the current transient. The period of one of these steps is around 0.3 ns, which is consistent with the TDR analysis as well as with the theoretical calculation of the signal propagation time.

In general, the current I_{TLP} flowing from the CC-TLP contact needle into a DUT can be calculated by the superposition of the measured incident voltage pulse $V_{\mathrm{inc}}(t)$ and the reflected voltage pulse $V_{\mathrm{refl}}(t-\Delta t)$ (Eq. (4.2)). In the case of a non-COF technology, where the contact needle is directly connected to the pin or pad of the DUT without additional TLs between, $I_{\mathrm{TLP}}(t)$ corresponds to the stress current seen by the DUT. In the case of the investigated COF technology, the TLs may have an impact on the stress current $I(t)$ seen by the IC as well as on the measured signal $I_{\mathrm{TLP}}(t)$ (Fig. 7.2). This impact depends strongly on the capacitive and inductive coupling between the TLs and cannot directly be extracted from the measured data. However, the simulation provides an instrument to evaluate the influence of the TLs on the stress current. Since the capacitive and inductive coupling are adaptable parameters in the simulation model, they can be estimated and optimized by fitting the simulated curves (Fig. 7.5, black curves) to the measured current transients (Fig. 7.5, red curves). By varying the coupling parameters around their optimized values, the simulated stress current at the end of the TL, reaching the chip, is only a few percent higher than the peak current at the end of the CC-TLP probe needle (Fig. 7.6). This means that the measured current I_{TLP} (Eq. (4.2)) is a good measure for the real stress current $I(t)$ that reaches the IC. The verified simulation model allows the investigation of waveforms at various locations, helping to distinguish between different influences and parameters. The shape of the reflected pulse in CC-TLP on flex (Fig. 7.5, middle right graph) is basically created by the following three impedance discontinuities or mismatches: the inductance of the contact needle, the impedance rise from the contact needle to the TL and the impedance fall from the TL to the chip during its capacitive charging. The superposition of these three reflections creates the original reflected pulse measured in CC-TLP. By removing the TL, the inductance of the needle is followed directly by the impedance fall from the transition to the chip. Consequently, this corresponds to the measured and simulated CC-TLP waveform on a wafer (Fig. 7.5, bottom graphs).

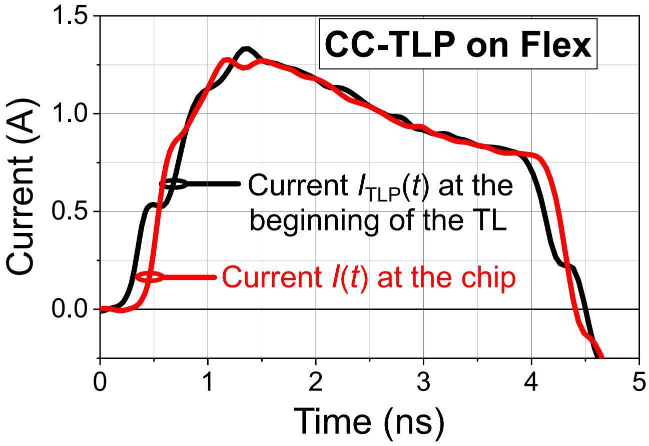

Figure 7.6 Influence of TLs on the CC-TLP stress current. The reconstructed current $I_{\mathrm{TLP}}(t)$ equals the current at the end of the CC-TLP needle, which was injected into the TL (black curve). This simulation shows that its peak current, is only 5 percent higher than the peak current at the end of the TL $I(t)$, which is seen by the chip (red curve). The positions of the current measurement can be found in Figure 7.3 (current probes).

7.2.3 Failure threshold analysis

Having investigated the basic operating principles of CDM and CC-TLP applied to the COF assembly and having demonstrated their theoretical feasibility, the thesis proceeds to analyze the correlation between CDM and CC-TLP regarding their current failure threshold. To reduce measurement differences within the metrology chains, the 33 GHz oscilloscope was used for both methods. The CDM test was performed following the JEDEC specification JESD22-C101 [10] with three positive and negative pulses per pad and voltage level (Section 5.2). The JEDEC test head is free of ferrites and tuning cavities and well exceeds a -3 dB

S_{11}-bandwidth of 18 GHz (Section 6.1.2). As CC-TLP is a contact-mode test model with no air discharge, there is no lack of reproducibility as it is in CDM (Section 5.1). Therefore, only one positive stress pulse per pad was used. In preliminary investigations, the positive polarity was determined as being the more sensitive one for the IC. In this polarity, the current flows through the reverse biased junction, eventually causing its failure. In this configuration, the CDM test delivers a failure current threshold of around 0.7 A, while the failure current threshold of CC-TLP on flex is higher, with around 1.2 A. However, by reducing the CDM stress sequence from three positive pulses to one positive and one negative pulse per pad, the failure current rises to around 1.2 A and thus complies with CC-TLP on flex. To exclude any polarity effects, CDM was also performed with just a single pulse of the most sensitive polarity, reproducing the same result. It becomes obvious that in this case, in contrast to typical CDM gate oxide ruptures, the cumulative damage increases the leakage in the junction until the failure criterion is met, thereby defining the failure threshold of the DUT. This was a first indication that beyond peak current the overall stress time and with it, the dissipated energy could be an alternative failure criterion of this IC. For additional verification of the correlation, CC-TLP at wafer level was performed. This test yielded the same failure signature at the same peak current failure threshold of 1.2 A.

In this context, another hint on an energy dependent failure mechanism was found: Figure 7.7 shows the lowest current transients of CC-TLP and CDM that lead to a failure of the IC. As expected, by changing the height h_{GP} of the GP above the flex (Fig. 7.2) the waveform of the current transient changes. This is explained by the fact that the characteristic impedance of the TLs depends inversely on the capacitance per length (Fig. 7.4). This means that for a defined peak current, the higher the separation h_{GP}, the higher pulse voltage is needed to generate an equivalent current. However, besides that, the failure current threshold rises also with increasing height h_{GP} (Fig. 7.7, black, blue and pink waveform). This effect was observed by stepwise increasing the pulse amplitude of the TLP system and monitoring the leakage current after each stress pulse. The CC-TLP currents failure thresholds on flex were specified to $\{1.1, 1.2, 1.4\}$ A, for separation heights of $h_{\mathrm{GP}} = \{300, 500, 1000\}\,\mu\mathrm{m}$. In addition to that, Figure 7.7 depicts the lowest failure current waveform of CC-TLP on wafer (orange hatched area), which amounts to 1.2 A. A variation of the GP-foil distance results in a deviation from the initially measured threshold level of 1.2 A. The peak current for $h_{\mathrm{GP}} = 1000\,\mu\mathrm{m}$ is almost 30% higher than the peak current for $h_{\mathrm{GP}} = 300\,\mu\mathrm{m}$. However, the integration of the current curves over the charging period as well as the integration of the square of the curves yields to a very similar value (less than 4% variation). This clearly indicates that the total transferred charge ($Q = \int I(t)\,\mathrm{d}t$) and as such the energy dissipated

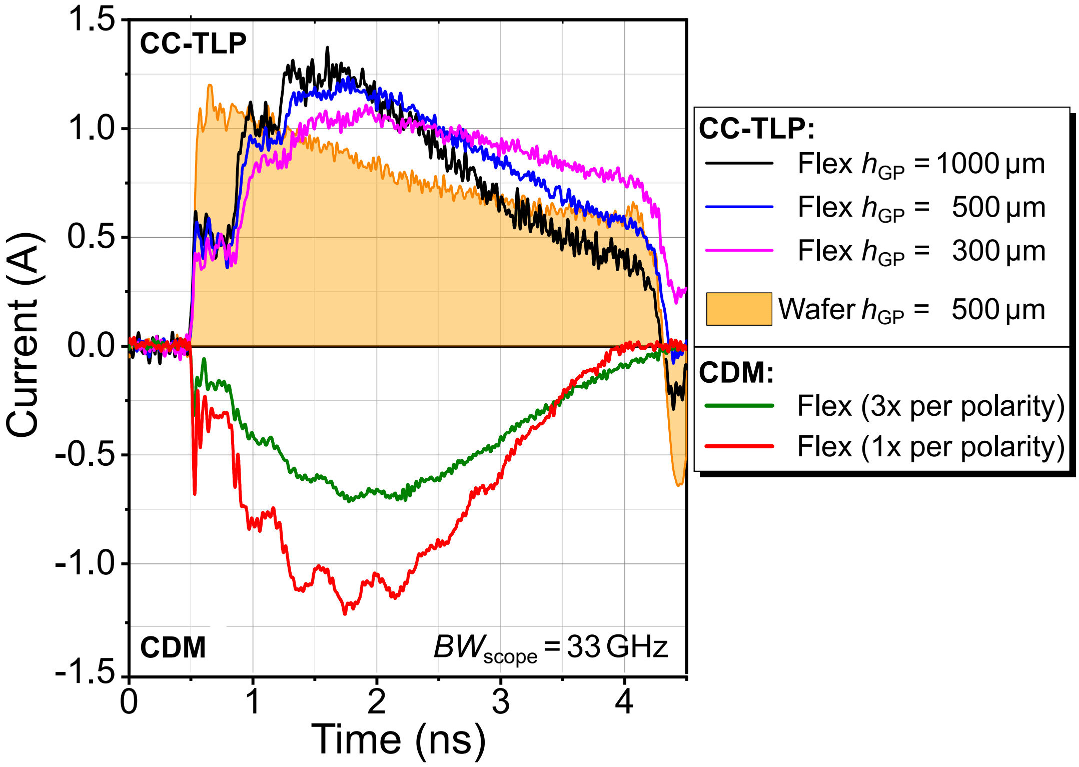

Figure 7.7 Lowest failure current waveforms of CDM on flex and CC-TLP on flex and on wafer. Based on different definitions, a positive stress current of CC-TLP corresponds to a negative stress current in CDM (Section 4.4). For the default distance between GP and flex of $h_{\text{GP}} = 500\,\mu\text{m}$, the peak current of CC-TLP on flex and on wafer correlate. Besides, all the CC-TLP waveforms together with the CDM failure waveform for one pulse per polarity and pin as well as the square of these waveforms show a very similar area under the curve.

in the junction ($E = \int RI(t)^2\,\mathrm{d}t$) have a dominant influence on triggering the failure. This argumentation also holds with respect to the lowest failure current waveform of CDM on flex, when performing only one pulse per pad and polarity (Fig. 7.7, red waveform). The default usage of the “Maximum-of-three-pulses” method (Section 5.2.1), i.e. three CDM pulses per pad and polarity (Fig. 7.7, green waveform), reduces the CDM current failure threshold from around 1.2 A to only 0.7 A.

CDM discharges of today’s typical IC packages are below the 3 ns pulse width region. In contrast to the typical gate oxide breakdowns in the CDM-domain, energy driven ESD damages of junctions are usually induced by stress pulses in the HBM-domain (Appendix A.1), i.e. pulse width around 100 ns. For the tested COF assemblies, the charged package is represented by the flex including its many long TLs, producing transients with around 4 ns duration (Fig. 7.7). Being on the upper limit of typical CDM pulse widths, this might have contributed to the occurrence of a pn-junction failure. Overall, this is a very important finding as it shows that even for pulse widths of only some nanoseconds, it is not always sufficient to look only at the peak currents of CDM and CC-TLP as the energy content may play a crucial role, especially in the case of a junction failure.

7.2.4 Summary and conclusions

This study highlighted emerging challenges for ESD testing on large flexible electronic assemblies. The strong tendency for charging and slow decay of the stored charge on the substrate foil complicates the prevention of ESD events and is a risk for ESD testing. Contour plots, generated by an innovative automated scanning setup (ESPSP), provide a quantitative understanding of the origin and location of the mobile and immobile charge on the COF assembly. The study demonstrates the feasibility of CDM testing on a COF assembly that significantly exceeds the size of standard packages. There is no direct overlap between the GP of CDM or CC-TLP and the chip on foil and their GPs mainly couple with the long interconnect traces on the polyimide film. The CC-TLP method provides a reduced characteristic impedance for the traces, compared to CDM, originating from the reduced GP height above the circuit. Nevertheless, a correlation of CDM's and CC-TLP's failure current threshold on flex with CC-TLP at wafer level was obtained. Their correlation in this unconventional test case gives further justification for the establishment of the CC-TLP stress test method in the industrial environment. Besides that, the simulations provide a deeper insight into the ESD event on the COF itself. By means of a simulation model that reproduced the measured waveforms very well, the impact of the electrically coupled traces on foil was investigated. It was demonstrated that the reconstructed current in CC-TLP $I_{\mathrm{TLP}}(t)$ is an appropriate measure for the stress current that flows directly into the chip. Unlike gate oxide related leakage, for this stressed chip with a sensitive pn-junction in the direct discharge path, the number of stress pulses obviously has an influence on the degradation and ultimately the level at which the failure threshold is reached. This is quite an important finding as this means that even for the adiabatic conditions in the CDM-domain, ESD failures can be more closely related to the dissipated energy than the peak current. In this case, a reliable correlation requires a clear specification of the number of stress pulses, which is, apart from different definitions like “at least one” or “at least three”, freely selectable according to the prevalent CDM standards. In this study, the very repeatable impulses of CC-TLP simulate CDM failure mechanisms, in this case a pn-junction, very well and in a highly controllable way.

7.3 CDM to CC-TLP-correlation of a very small packaged IC

Critical stress parameter: Current slew rate

Starting from poorly reproducible test results of three different CDM testers on a very small packaged IC designed in a 0.25 µm BCD technology, this chapter examines the question if this can be resolved by CC-TLP [20, 21]. It thereby reveals the current slew rate as the reason for the poor reproducibility of CDM failures and analyzes the significance of this critical stress parameter as an additional failure threshold.

7.3.1 Miscorrelation between three different CDM testers

The starting point of the investigations were the poorly correlating results from standard qualification tests, performed by three different CDM testers, listed in Table 7.1. There is a wide range of possibilities of characterizing the susceptibility of a device to damage from ESD under CDM conditions. Apart from the choice of the ESD standards, e.g. JESD22-C101F [10] or ANSI/ESD S5.3.1 [51], which have recently been replaced by the joint standard ANSI/ESDA/JEDEC JS-002-2014 [36], one can choose between a handful of different CDM testers and test equipment. All three CDM tests were performed according the CDM standard JESD22 C101F [10], which requires an oscilloscope with single shot bandwidth of 1 GHz for calibration. The qualification test itself has no upper limitation on the bandwidth and requires at least one positive and one negative stress pulse per pin. Despite the monitoring

Table 7.1 CDM test results illustrating the response of three pins of the DUT to CDM and reporting the ratio of the total sample size (left number) and the number of failing samples (right number). The number of the failing pins is denoted in brackets.

	Miscorrelation between three different CDM testers					
Tester	**A**		**B**		**C**	
Pulses per pol.	1		3		1	
Scope *BW* (GHz)	6		4		8	
< 500 V	27/0		12/0		6/0	
500 V	18/4	(1,2)	6/0		3/0	
625 V	9/5	(1,2)	6/0		3/0	
750 V	18/5	(1,2,3)	6/3	(2)	3/3	(1,2)
875 V	-	-	6/3	(1,2)	-	-
1000 V	18/8	(1,2,3)	6/2	(1,2)	3/3	(1,2)
1500 V	18/8	(1,2,3)	-	-	3/2	(1,2)

and recording of waveforms or respective peak currents is not mandatory according to the standard, all stress currents were recorded. However, the usage of different number of CDM pulses and different bandwidths of the oscilloscope complicates the comparison of the different CDM tests (Table 7.1).

In the three CDM tests, stress levels between 250 V and 1.5 kV were used. While first device failures were found at 500 V for tester A, tester B and C started to generate failures only at 750 V. For tester A and B at least half of the tested devices passed the test, even for 1.5 kV. Even for single CDM testers, the threshold voltage was not reproducible. Pin 3 only failed for tester A. In order to be able to understand this miscorrelation, a deeper failure threshold analysis by means of CC-TLP was performed, which raises the question if CC-TLP is able to resolve the correlation issues between the three different CDM testers.

7.3.2 Waveform analysis

As the reconstruction of CC-TLP's stress currents depends on the exact superposition of the fast rising edges of the measured voltage pulses (Section 4.3.3), the 33 GHz oscilloscope (Section 6.1.2) was used. The correlation study was started by characterizing the waveforms of the test systems by stressing the ground pin of the DUT. The ground pin was chosen, because it has the least impedance which results in the largest discharge currents. Polarity split tests showed that the failing pins are sensitive to negative CDM stress (Section 4.4). The results are shown in Figure 7.8. In contrast to the large COF assembly in the previous study (Section 7.2), the IC is assembled in a package with a very small footprint of only 7.5 mm^2. Thus, the duration of the measured current waveforms is fairly small. In order to induce the same failures, CC-TLP has to generate a current waveform similar to the CDM discharge currents. The pulse width of the stress current $I_{\mathrm{TLP}}(t)$ in CC-TLP is determined

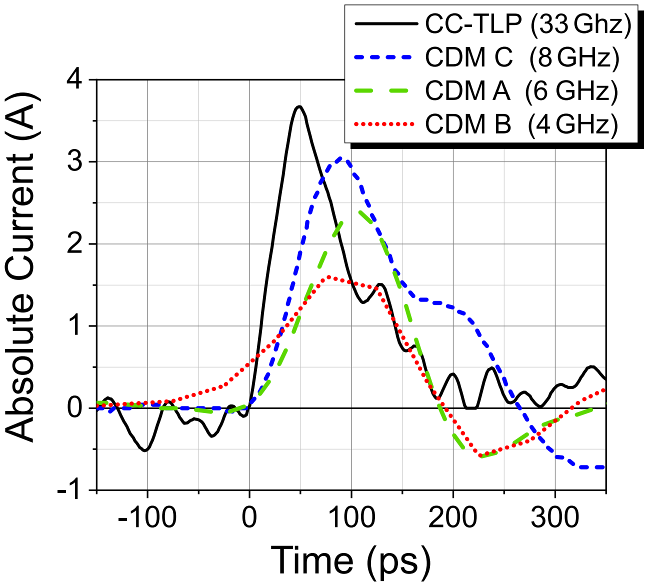

Figure 7.8 Current waveforms of CDM testers A, B and C for +500 V CDM stress of the ground pin and CC-TLP with a higher current level.

by the background capacitance C_b, which can be controlled by the distance of the GP h_{GP} above the DUT (Fig. 4.1) and the pulse width of the VF-TLP generator (Section 4.4). By setting the separation height to $h_{GP} = 300\,\mu\text{m}$, a 1 ns voltage pulse triggers a stress current waveform with a pulse width of around 300 ps. The resulting CC-TLP transients at the interface of the DUT show comparable current waveforms with respect to CDM (Fig. 7.8). The difference in amplitudes of the CDM curves is caused by the variations arising from the air discharge and due to the difference in the bandwidths of the oscilloscopes used (Table 7.2).

Table 7.2 Reconstruction and comparison of rise time, bandwidth and current slew rate of the signals (Fig. 7.8), measured by the respective oscilloscopes of the CC-TLP and the CDM testers.

	CDM			**CC-TLP**
Tester	**A**	**B**	**C**	
Scope bandwidth (GHz)	6	4	8	33
Signal rise time t_r (ps)	72	128	55	49
Signal bandwidth BW (GHz)	5.9	3.3	7.7	8.7
Current slew rate SR (A/ns)	26	10	44	60

Table 7.2 compares the rise times t_r of the waveforms shown in Figure 7.8. The signal bandwidths BW reconstructed from the rise times of the CDM waveforms (Eq. 6.1) match the bandwidths of the used oscilloscopes very well. These bandwidths seem to represent the limiting factor of the given CDM systems. For CC-TLP, the highest measured bandwidth is with only 8.7 GHz much lower than the bandwidth of the oscilloscope (33 GHz). This fact initiated the further improvement of the system's bandwidth, particularly the relay switch in the pulse generator and the pick-off tee in the course of the dissertation (Section 6.1.2 and 6.1.2). Obviously, the bandwidth of the CC-TLP system is limited by the bandwidth of the individual components (Eq. (6.2)). Inserting the measured bandwidths of the CC-TLP test head ($\sim 22\,\text{GHz}$), the pick-off stress path (type C) ($\sim 13\,\text{GHz}$), the cables ($> 20\,\text{GHz}$) and the oscilloscope ($\sim 33\,\text{GHz}$) (Section 6.1.2) leads to a system bandwidth around $10\,\text{GHz}$, which is close to the signal bandwidth derived from the signal rise time (8.7 GHz). The slew rate SR can have major impact on the susceptibility of some components or structures to fail due to ESD and is defined as the mean change of voltage or current per unit of time (Eq. (6.4)). With 49 ps, the stress current waveform of CC-TLP has the shortest rise time (highest slew rate: $SR = 60\,\text{ns}$). The definition and a detailed description of the rise time, slew rate and the limiting bandwidth factors of CC-TLP can be found in Chapter 6.

7.3.3 Failure threshold analysis

For a deeper analyzes, the stress currents of tester B were recorded during the CDM test. Due to the air discharge, the CDM peaks show a relative deviation of up to ±20% of the mean value. This is consistent with former statistical analysis of CDM current variations [53] (Section 5.1). Although tester C provided the most stringent results (Table 7.2), in-situ measurements of its peak current variation showed a spread of up to ±65% for some stress levels and pins [20]. Nonetheless, the failure thresholds of testers B and C are in good agreement. This indicates that a failure dependency on the number of pulses per pin as demonstrated in Section 7.2 can be excluded for the tested device. In addition, a pre/post CDM stress drift analyzes verified that no passing unit suffered from any degradation or wear-out effect after the stress. Nevertheless, the soft transition from PASS to FAIL of testers A and B and the <100% failure rates of all CDM testers imply that the reproducibility of the CDM testers is limited.

For CC-TLP, the failure threshold was determined by a step stress. It was measured by increasing stepwise the pulse amplitude of the (VF-)TLP pulse generator and monitoring the leakage current after each stress pulse (Fig. 4.2). The evolution of the leakage currents is shown in Figure 7.9. For CC-TLP, all pins that were stressed above the failure threshold showed a clear leakage current. The failure signature was found to perfectly match the electrical failure signature of the failing units after CDM stress [20]. In contrast to CDM, the failure thresholds determined by CC-TLP were very reproducible (e.g. Fig. 7.9). Single CC-TLP stress pulses as well as multiple CDM discharges gave the same test results, which shows that step stressing has no impact on the failure current. Overall, the failure thresholds determined with CC-TLP lies within the ones measured by the three CDM testers. A possible reason why pin 3 showed no fail when stressed with tester B is the large failure threshold of pin 3 (∼ 50% larger than pin 1). The corresponding stress level of 1.125 kV was not covered by tester B. Tester C shows a <100% failure rate at 1.5 kV, possibly caused by partial discharges as shown in [50] and potentially preventing a failure of pin 3.

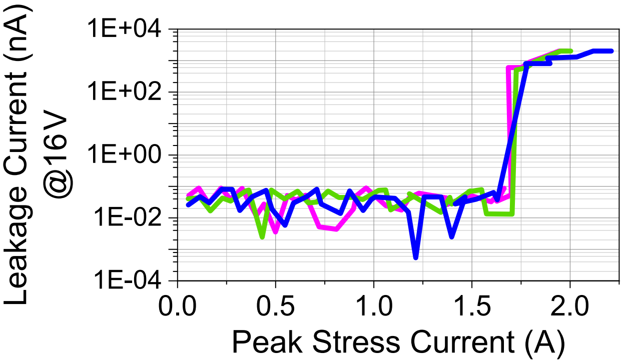

Figure 7.9 DC leakage current evolution at pin 2 of three different DUTs as function of the CC-TLP stress current. The electrical DC characteristic before and after the CC-TLP measurement can be found in [20].

7.3.4 Correlation of electrical and physical failure signatures

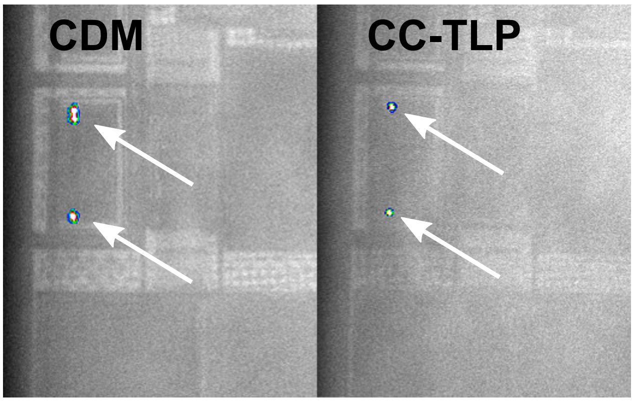

Figure 7.10 Backside photon Emission Microscopy (EMMI) images of DUTs with failures of pin 2. The spots indicate the failure locations after CDM stress (left) and CC-TLP stress (right).

In the course of the physical failure analyzes, the damaged DUTs have first been investigated for their electrical failure signatures by means of DC curve-traces of the damaged pins. All three device pins damaged by CDMor CC-TLP stress showed very similar failure signatures [20]. Afterwards, the failure location was narrowed down by backside photon Emission Microscopy (EMMI) (Fig. 7.10). Both images show emission spots at the same location. Finally, the devices were deprocessed in order to investigate the detailed failure location and microscopic failure signature. After polysilicon etching, scanning electron microscope (SEM) images were taken of a CDM stressed device and of a corresponding CC-TLP stressed device (Fig. 7.11). They show the damaged gate oxide of a transistor connected to the stressed pin. The CC-TLP measurement has caused the same failure signatures in the same location as the CDM stress. This damage represents the primary failure mechanism of the given stress. As a secondary effect, it was found in a deeper analysis of some damaged devices that the drain-to-source junction of a driving 5 V transistor suffered from a melt filament. A conceptual IC schematic and details about this secondary damage can be found in [20]. In conclusion, all aforementioned figures in this section demonstrate the excellent correlation between CDM and CC-TLP stress.

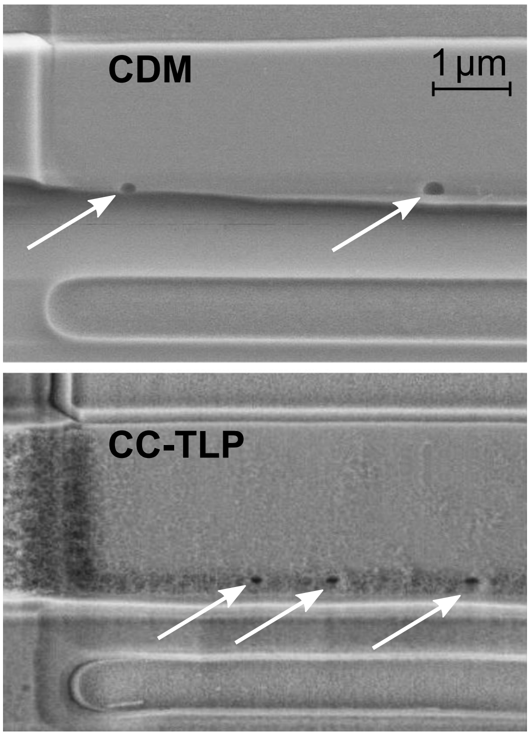

Figure 7.11 SEM images of a gate oxide damaged by CDM stress (top) and CC-TLP stress (bottom).

7.3.5 Reproducibility issues of CDM failure thresholds

The results of the CDM tests show a poor reproducibility of the threshold voltages between 500 V and 700 V with no hard limit (i.e. 100% failure rate) for the CDM robustness. In contrast, the failure threshold determined by CC-TLP is highly reproducible and lies within this range. In this investigation, the most sensitive pin (pin 2) was stressed. The rise time of the CC-TLP setup was varied by rise time filters that were inserted into the stress path. The peak currents of the stress ($I_\mathrm{p} := \max(I_\mathrm{TLP}(t))$) and corresponding slew rates ($SR := \overline{\mathrm{d}I_\mathrm{TLP}(t)/\mathrm{d}t}$) of the rising edges are plotted in Figure 7.12 for the different rise time configurations.

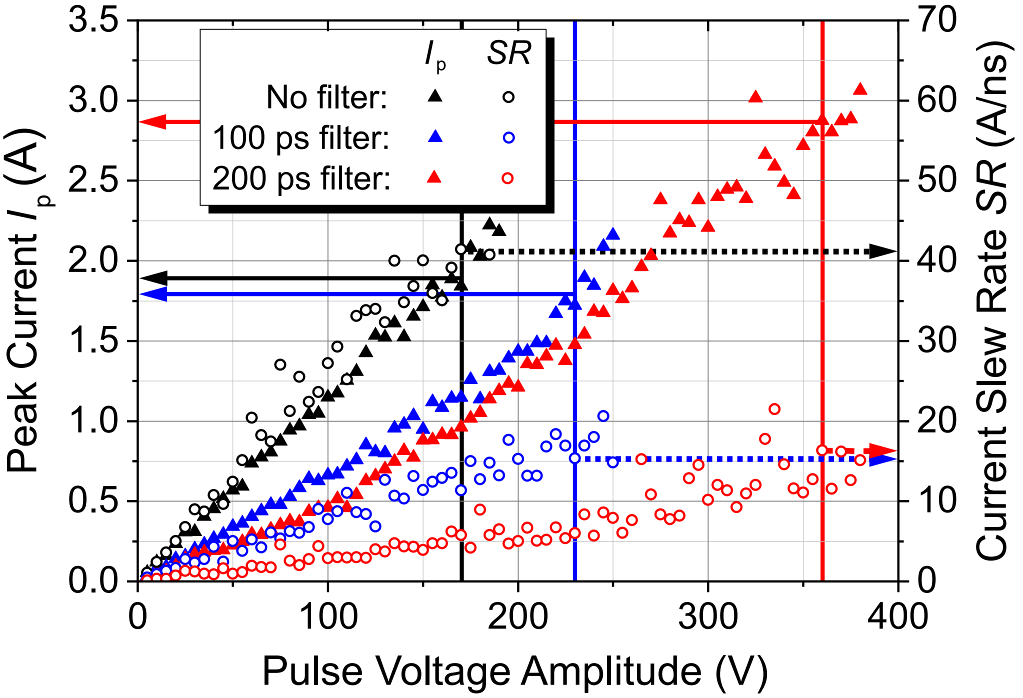

Figure 7.12 Peak currents (▲) and corresponding slew rates (○) for a CC-TLP step stress of pin 2 without (black), with a 100 ps (blue) and with a 200 ps (red) rise time filter in the stress path. The vertical lines mark the respective failure thresholds.

In the default CC-TLP setup without any filters, pin 2 was found to fail for currents above 1.7 A (Fig. 7.12, ▲, ◄—). The corresponding slew rate amounted to 41 A/ns (Fig. 7.12, ○, ··►). Having inserted a 100 ps rise time filter into CC-TLP's stress path (▲), a higher pulse voltage was required in order to cause a failure. This is because the high-frequency part of the waveform and thus a contributing to its amplitude in time-domain was cut off by the filter. Nevertheless, the threshold current (◄—) remained at around 1.7 A, whereas the corresponding slew rate (○) dropped to only 15 A/ns (··►). However, employing a 200 ps rise time filter (▲), the failure threshold current increased to slightly less than 2.8 A (←), whereas the slew rate (○) remained at 16 A/ns (⇢). Several repetitions of those tests led to the same result.

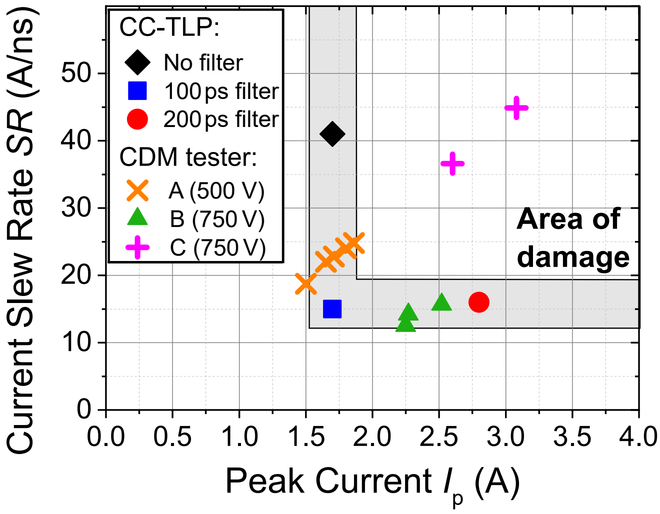

Figure 7.13 Threshold currents and threshold slew rates derived from CC-TLP step stress of pin 2 with different rise time filters (◆, ■ and ●) and corresponding data measured at CDM tester A (✕), B (▲) and C (+).

This indicates that both a threshold current (∼ 1.7 A) and a threshold slew rate (∼ 15 A/ns) have to be exceeded in order to cause a failure, which is plausible given the naturally limited triggering speed of any ESD protection structure. Performing CC-TLP tests using different rise time filters, the slew rate was identified to be a critical stress factor for the tested devices. Diagram (Fig. 7.13) visualizes the three CC-TLP threshold current and slew rate pairs as well as the corresponding data pairs of the CDM testers. The CC-TLP data pairs define the thresholds of the “Area of damage” (Fig. 7.13, top right) , for which a damage of the DUT is expected. The evaluation of the current slew rate of pin 2 stressed by CDM tester B showed that its data pairs are distributed around the slew rate threshold (Fig. 7.13, ▲). Hence, the CDM slew rate variation caused by the air discharge (Fig. 7.14) may explain the low failure rates above 625 V for tester B in Table 7.1.

The threshold slew rate is clearly exceeded by testers A (✕) and C (+), even if a typical CDM slew rate spread of ±25%, as indicated in Figure 7.14, is assumed. Since the data of tester A (✕) is distributed around the peak current threshold in Figure 7.13, its peak current variation might be the limiting factor for its low failure rate at 500 V. In spite of enormous peak current variation, tester C (+) provided the most stringent results (Table 7.2), which becomes visible in the fact that its data pairs clearly exceeded both, the current and the slew rate threshold and thus lie within the “Area of damage” (Fig. 7.13).

For higher stress levels, parasitic effects may play a crucial role for the poor CDM reproducibility. As explained in [50], CDM tester discharges can be divided into a more reproducible discharge regime and a non-reproducible discharge regime. The latter is reported

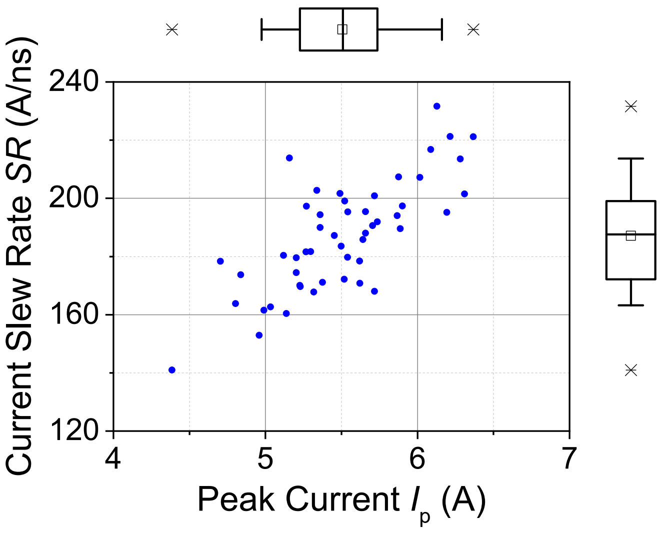

Figure 7.14 Peak current to slew rate distribution of 50 positive stress pulses obtained with tester B on pin 2 under test condition TC 750 of JS-002-2014 [36], measured by a 33 GHz oscilloscope. The distribution is illustrated by means of boxplots (25th and 75th percentiles) with whiskers (5th and 95th percentiles).

to be facilitated by a high charging voltage, a spiky pogo pin, a curved device pin, a slow contact velocity, an inaccurate alignment and a high humidity. From these contributing factors, a curved device pin and a high humidity can be excluded for the given CDM tests, since the given IC is assembled in a QFN-like package and the humidity is controlled by air conditioning. Unfortunately, none of the other factors can be excluded as well. Hence, in particular the passing devices at 1.5 kV could be traced back to partial discharges while operating tester A and C in the non-reproducible discharge regime. Unfortunately, the root cause of the 500 V failure threshold obtained with tester A is still unknown. However, it should be noted that the 500 V and 625 V fails of tester A could not be repeated with the same tester in subsequent CDM tests of the same DUT, which opens the door for speculations on a temporarily miscalibrated or a defective tester.

7.3.6 Summary and conclusions

Three different CDM test systems and a CC-TLP system were compared regarding their mode of operation, their discharge waveforms, the reproducibility of their measurement results and the resulting failure thresholds, failure locations and failure signatures of a small DUT. Special attention was paid to the characteristics of the metrology chain and the failure thresholds of the DUT. It was found that the failure thresholds and failure locations as well as the electrical and microscopical failure signatures obtained with CC-TLP measurements matched those obtained with the CDM testers very well. Hence, these results demonstrate an excellent correlation between CDM tests and CC-TLP measurements. At the same time, it became obvious that the major drawback of CDM testing is its limited reproducibility and repeatability, which is not an issue at all for CC-TLP measurements thanks to its contact-based mode of operation. In addition, it was found that differences of the measurement chain become especially important for the extremely narrow discharge pulses of small devices. This work clearly points out the advantages of CC-TLP over CDM testing, particularly its minimal parasitic influences, which enable highly reproducible and repeatable stress pulses and test results as well as its ability to control and tune the rise time and pulse width of its pulses for special investigations. By means of a special investigation of the current slew rate, it was shown that both a threshold current and a threshold slew rate have to be exceeded in order to cause a failure.

7.4 CDM to CC-TLP-correlation of an ultra-high-speed interface IC

Critical stress parameter: Current slew rate

Challenging the limits of today's metrology and test setups for CDM and CC-TLP, this study identifies critical stress parameters for a 25 Gbps communication device in the CDM-domain. Only CC-TLP stress in combination with a 33/63 GHz single shot oscilloscope was able to relate significant differences of failure current distributions to the rise time spread in the order of few tens of picoseconds and to obtain a conclusive sharp pass/fail transition at a certain peak current level. Thereby, several potential critical stress parameters were analyzed as well as the role of the integrated DC-blocking capacitor, which is required in many high-speed applications. Knowing the impact of the stress parameters may help to identify the limits of each method.

7.4.1 Failure mode: ESD during PCB assembly

The object of investigation is a 28 nm CMOS IC for network applications with ultra-high-speed (25 Gbps) interfaces. It is packaged in a 14 mm × 14 mm flip chip BGA (FCBGA) with a metal lid for heat spreading. The steady increase in data rates in high-speed IOs, technology scaling and IO voltage reduction have come at the expense of degraded ESD robustness, which entails new challenges in ESD protection for the network industry [7] (Section 3.1). Particularly for high-speed I/O's, IC designers have to minimize the parasitic capacitance of ESD protection structures [77] in order to prevent performance degradation. These low capacitance levels typically result in a reduced ESD robustness. In order to reduce noise on other signals, 82 of the 169 solder balls are "GND" ($\sim$50%). As a first characterization, the different types of ground nets were identified as illustrated in Section 5.3.

The investigated device passes ESD qualification tests (HBM: ± 2 kV, CDM: ± 200 V [78]) but shows a failure rate above 1% after the board assembly. Through a detailed inspection at each manufacturing process step, the press-fit process of charged through-hole connectors was identified to be the root cause [78]. These charged up during transportation inside transport trays that have been wrongly labeled as "antistatic". A detailed description and simulations of the connectors discharge scenarios can be found in [79]. The research within this thesis extends previous studies through characterizing the ESD sensitivity of the RF components at the component level. It examines the peak current threshold correlation between CDM and CC-TLP and thereby analyzes potential critical stress parameters with single-digit ps-resolution and precision.

7.4.2 Charge distribution on the cable connector

Previous ESD case studies [78, 79] examined the direct discharge from a cable connector to the high-speed interface signal pin of this IC at the press-fit assembly process. The highly charged connectors are able to initiate ultra-fast, hardly measureable ESD events reducing the yield in manufacturing. Complementing previous electrostatic investigations of the connectors [79], the surface potentials of the charged connectors were investigated by means of the non-contacting electrostatic voltmeter scanning method (ESPSP, Section 6.2). Prior to that, the connector had been triboelectrically charged within the highly insulative transport tray emulating the transportation process. Thereby, the surface potential of the transport tray partially even exceeded the limit of the electrostatic voltmeter of -3.5 kV. In order to measure the surface potential of the connector, the connector was picked out of the tray pocket and placed on a dissipative surface. Figure 7.15 illustrates an exemplary potential distribution of the cable connector. The purple/blue area with the highest magnitude of negative potential shows that a large amount of negative charges is trapped on the plastic insulator of the connector's interface (Fig. 7.15, peaks in contour profile) inducing mobile charge on the adjacent metal pins and surrounding shield represented by dark red color. A higher resolution was obtained by cutting off the tips of the pins. Being too small in comparison with the aperture of the electrostatic voltmeter, they reduce the precision. The scanning of connectors out of a static dissipative transport tray used in today's process yielded, with only a few Volts, much less severe charging.

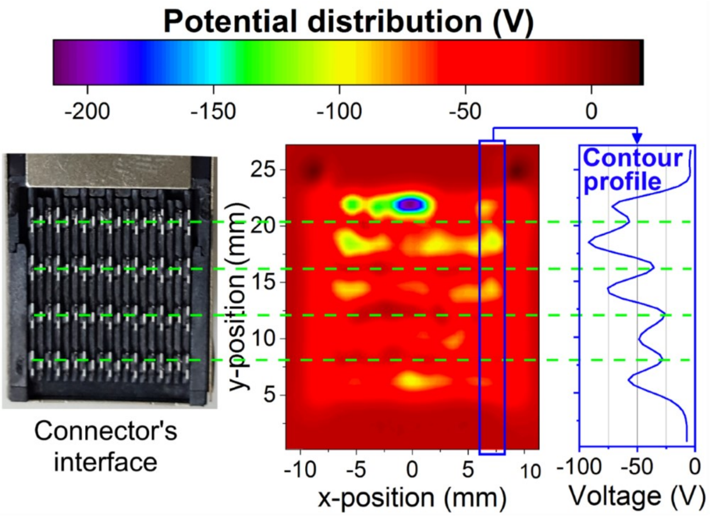

Figure 7.15 Electrostatic potential distribution (center) on the connector's interface (left) and contour plot (right).

7.4.3 ESD sensitivity characterization of the IC

In addition to the analysis of the electrostatic distribution of the charged connectors and their press-fit assembly process on PCB [78, 79], a holistic understanding of the ESD issue requires the characterization of the ESD sensitivity of the ICs. Prior to the stress procedure, the CDM tester was calibrated according to the joint standard ANSI/ESDA/JEDEC JS-002 2014 [36]. For the CC-TLP tests, a commercial (VF-)TLP generator with a minimum rise time of 100 ps per default was used. For special investigations, a fully customized ultra-fast home build (VF-)TLP pulse generator with a minimum rise time of only 40 ps was deployed. The GP is positioned directly above the DUT at a distance of $h_{\mathrm{GP}} = 0.5\,\mathrm{mm}$ by default. Besides, several pick-off tees are used. All components used are characterized in detail in Section 6.1.2.

A DC-decoupling capacitor in front of the high-speed input buffer [78] prevents the detection of the input gate oxide damage by means of DC leakage measurement. Hence, functional tests were performed on an evaluation board with a high-speed signal loopback connection as pass/fail criteria. The bit error rate and the evaluation of the eye pattern of its TX to RX loop are used to check the signal integrity in order to detect degradation and failure of the independently operating channels. Later, the device manufacturer exemplarily validated the failures by means of ATE and bench testing.

7.4.4 Failure threshold analysis

Approximately 100 high-speed pins from different devices were stressed by CDM. For each of the 12 differential channels, one input pin per input pair was stressed. As the failure of one channel did not affect neighboring channels directly or via the core, each device was reused until all channels had failed. Since CDM suffers from the lack of reproducibility due to the air discharge, each high-speed pin was stressed with three positive and three negative pulses at the defined Test Condition (TC). The term TC refers to the field plate voltage needed to produce waveform parameter conditions specified in the CDM standard ANSI/ESDA/JEDEC JS-002 2014 [36]. Figure 7.16 displays the initially measured CDM and CC-TLP distribution of peak currents to failure. For the measured CDM peak currents, there is a broad pass/fail distribution with a wide overlap of pass and fail starting at 2.5 A (TC 250). 100% fail starts at 5 A. This wide distribution was initially attributed to Soft Breakdown (SBD) effects [80], other device internal stress dynamics related to the package with built-in passives, or the existence of additional relevant stress parameters besides the peak current. In contrast to CDM, CC-TLP generated first failures for peak values around 5 A (Fig. 7.16, bottom distri-

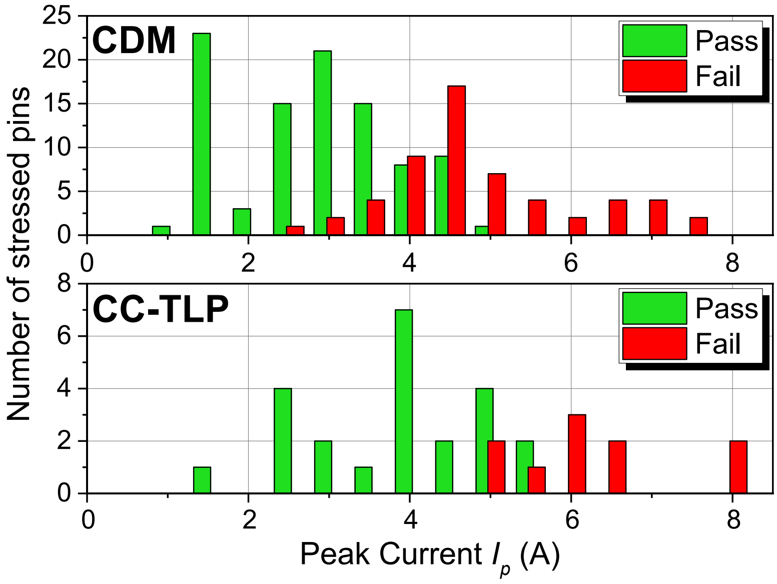

Figure 7.16 Number of failed and passed high-speed pins with respect to absolute CDM peak current $I_{\mathrm{CDM}}(t)$ (top) and CC-TLP peak current $I_{\mathrm{TLP}}(t)$ (bottom). Due to CDM's limited reproducibility, a higher statistic was set up.

bution), however with a rather sharp transition between pass and fail. In contrast to previous studies for gate oxide failures of less advanced technologies so far [20, 21, 15–19], looking at peak current failure thresholds, there is no explicit correlation between the low end of the distribution of CDM and CC-TLP peak currents. This fact as well as the wider distribution of CDM requires a more detailed analysis of critical stress factors and failure mechanisms.

7.4.5 Identification of the critical stress parameters

CC-TLP's ability to control and tune several parameters and the high reproducibility in comparison with to CDM provide a deeper insight into the impact of different potential critical stress parameters in the CDM-domain. The following sections describe the in-depth analyzes of potential critical stress parameters, which could be able to explain measured miscorrelation between CDM and CC-TLP for low current failures (Fig. 7.16). In this course, several parameters with potential influence on the current failure threshold were varied.

Transmission-Lines (TLs)

By stressing the same pins multiple times just below threshold, cumulative stress effects of the stress pulses, as revealed in the correlation study in Section 7.2 [5], were excluded. Another hypothesis and meaningful starting point in this analysis was that a difference between the current transients of CDM and CC-TLP could induce different failures and be the reason why only CDM testing was able to address the low peak current failures at 2.5 A. The waveforms of the 24 high-speed pins (12 differential pairs) can be categorized in three

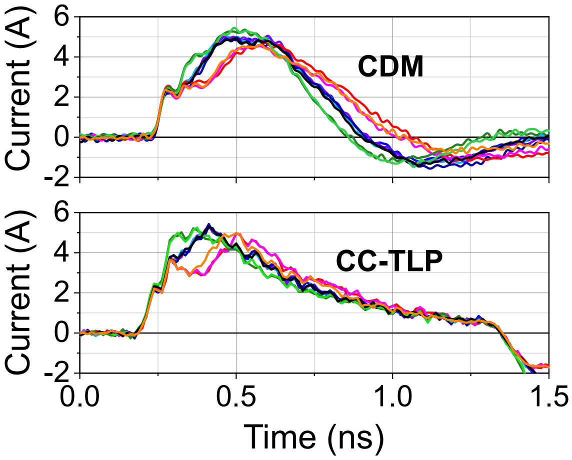

Figure 7.17 Waveform groups of the 24 high-speed pins all stressed according to test condition TC 400 [36].

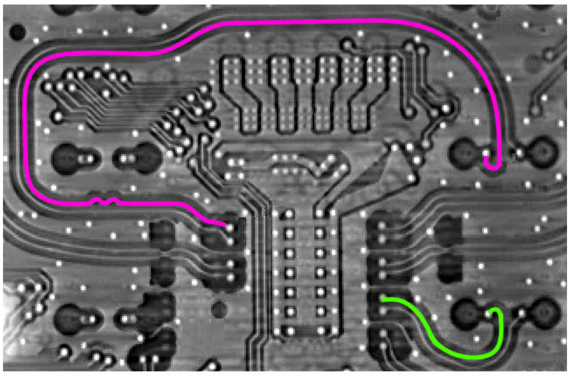

Figure 7.18 Different length in signal routing of two different high-speed pins.

different "groups" (Fig. 7.17, green, blue and orange/pink waveforms). Equal groups apply for negative polarity. The groups show different reflections in the rising edge of the pulses. Through 3D X-ray analysis of the package, this was identified to be related to different trace lengths in signal routing (Fig. 7.18). A longer trace (Fig. 7.18, e.g. pink line with respect to green line) resulted in an increased duration of the current plateau within the rising edge of the transient measured by CDM and CC-TLP (Fig. 7.17, orange/pink waveforms with respect to green waveforms). However, there was no difference of the peak current failure threshold between the different pins or waveform groups. Based on the simulations in Section 7.2.2 [5], this indicates that the stress current seen by the gate oxides is mostly independent of the length of the feeding transmission lines.

CC-TLP pulse width

The shape of the CDM waveform is mainly determined by the capacitance of the package, whereas the CC-TLP waveform can be tuned in different ways (Section 4.4). The first step was to adjust the incident voltage pulse width by varying the charged TL of the (VF-)TLP pulse generator. Although similar in the Full Width Half Maximum (FWHM), the unipolar widths of the stress currents in CC-TLP are, with 1.2 ns, about twice the 0.7 ns CDM pulse widths before polarity changes (Fig. 7.17). Thus, the incident CC-TLP voltage pulse width $t_{\mathrm{d,inc}}$ was reduced from 1.0 ns to 0.5 ns by applying a fully customized, ultra-fast home build (VF-)TLP pulse generator. As a result, the CDM pulse (Fig. 7.19, black curve) and CC-TLP pulse (Fig. 7.19, red curve) almost match. Although the CC-TLP waveform matched the

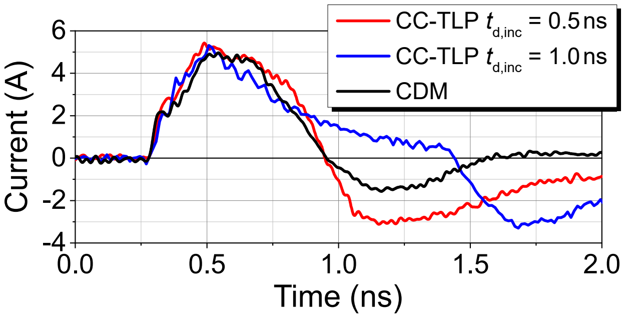

Figure 7.19 CDM and CC-TLP waveforms of a high-speed pin with different pulse widths.

CDM waveform almost perfectly, the difference in failure threshold could not be eliminated. Even the pulse width variation of the incident pulse from 300 ps up to 100 ns had no significant influence on the peak current failure threshold of CC-TLP. In order to further tailor the CC-TLP waveform to the one of CDM, remaining, slight differences in the falling edges of the CDM and CC-TLP waveform are investigated and minimized in the following step.

Source impedance

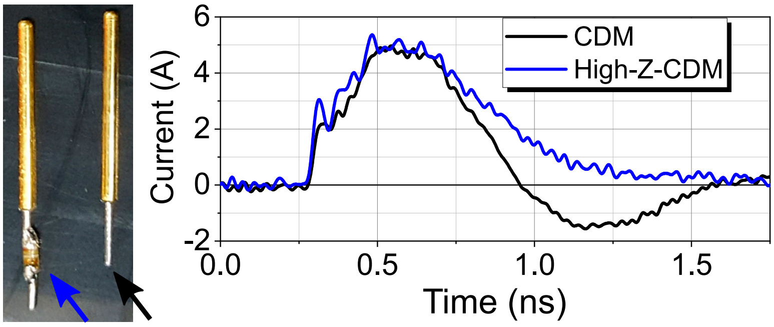

Figure 7.20 CDM testing on high-speed pins with default (right, black waveform) and high-Z pogo pin (left, blue waveform).

In contrast to CC-TLP's 50 Ω system, the CDM testing impedance is mainly given by the spark resistance in nitrogen atmosphere ($R_{S,CDM} \approx 28\,\Omega$ [59]). The generic simulation study (without consideration of the specific dynamic of the protection element) in Section 8.2 will be demonstrated that, despite their difference in source impedance, only a large gate oxide capacitance without ESD protection could cause miscorrelation between CDM and CC-TLP [21]. In order to experimentally investigate the impact of the source impedance on the current failure threshold for the DUT, a cylindrical resistor of 25 Ω was soldered on the pogo pin (Fig. 7.20, left picture). This CDM testing modification is hereinafter referred to as High Impedance CDM (high-Z CDM) testing. As theoretically predicted, high-Z CDM testing did not change the peak current failure threshold. Thus, the impedance difference seems to only have an influence on the (RC-) decay time of the stress current (Fig. 7.20, right graph) and is not likely to be a critical stress factor of the DUT.

Capacitive coupling to GP

A remaining difference between CDM and CC-TLP is the capacitive coupling between the GP and the DUT. Differences in capacitive coupling could lead to different charge distributions and stress differences of distinct charge/discharge paths. As brought out in Section 4.4, one can vary the transient decay of the stress current (RC-constant) by varying the heights of the GP above the DUT. For the CC-TLP tests, the GP was positioned directly above the DUT at a distance of $h_{\mathrm{GP}} = 0.5\,\mathrm{mm}$ by default (Fig. 4.1). The CDM set-up shows a higher distance between the GP and the DUT, due to the length of the pogo pin ($\sim 3.5\,\mathrm{mm}$). In CDM, the main coupling is built up via the FCP below the DUT ($C_{\mathrm{FCP\text{-}DUT}}$, Fig. 2.2), which forms a capacitance with the GP ($C_{\mathrm{FCP\text{-}GP}}$, Fig. 2.2) [37]. In contrast to the studies in Section 7.2 (Fig. 7.7), a variation of the capacitive coupling to the GP ($C_{\mathrm{DUT\text{-}GP}}$, Fig. 2.2) by changing the separation height h_{GP} between DUT and GP has almost no influence on the CC-TLP waveform (Fig. 7.21). This indicates that even for CC-TLP, this DUT, lying on its metal lid, mainly couples with the FCP below. Hence, in order to decrease the capacitive coupling between DUT and FCP, the distance between DUT and FCP h_{DUT} was increased by means of small PVC sheets (Fig. 7.22). The reduced RC-constant results in a shorter CC-TLP pulse width. A similar effect was achieved

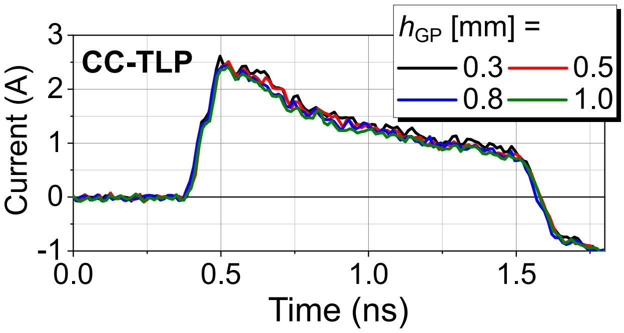

Figure 7.21 CC-TLP current waveforms of a high-speed pin for a defined TLP voltage and different separation heights h_{GP} between GP and DUT (Fig. 4.1). A variation of h_{GP} has almost no influence on the CC-TLP waveform.

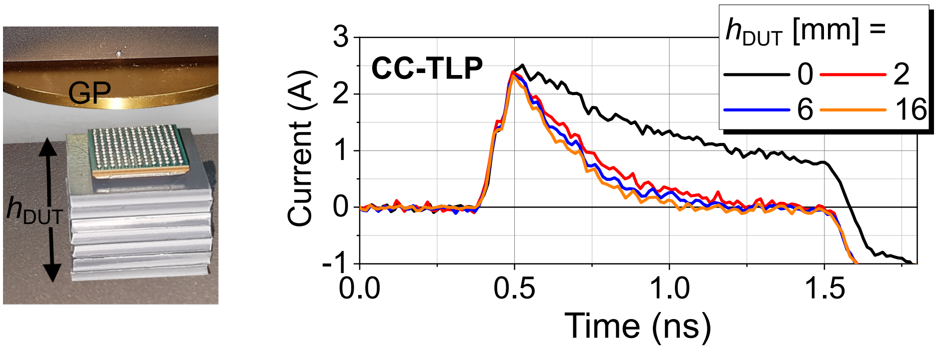

Figure 7.22 CC-TLP current waveforms for different heights h_{DUT} of the DUT above the FCP. An increase of h_{DUT} results in a reduced RC-decay of the CC-TLP waveform.

by removing the metal lid of the package, which acts as a heat spreader for the flip chip underneath, during testing. However, neither a change of the DUT/GP or FCP/GP coupling nor ESD testing without metal lid changed the failure threshold peak current. Thus, the capacitive coupling as well as the floating metal lid can be excluded to be the root cause for CDM addressing lower current failures ($I_\mathrm{p} \sim 2.5\,\mathrm{A}$) in comparison to CC-TLP.

The pogo pin capacitance

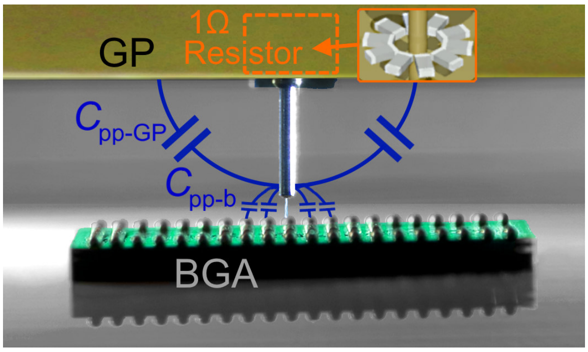

Figure 7.23 Schematic artwork of the CDM discharge. An initial, not directly measurable current flow stresses the device by charging/discharging the capacitance between pogo pin's plunger and GP ($C_\text{pp-GP}$) and the capacitances between pogo pin's plunger and the balls of the BGA ($C_\text{pp-b}$).

In analogy to the fast and high initial peak of air discharge system level tests (Section A.2), a potential effect of the local capacitance of the pogo pin's plunger in the CDM test is investigated on the devices [81]. The initial discharge of locally stored mobile charge into the effective capacitance between plunger and its surrounding (Fig. 7.23) results in an ultra-fast rising current pulse felt by the device but by-passing the 1 Ω current sensor resistor. As a consequence, it cannot be measured even by means of an ideal fast CDM metrology. This could be a possible explanation for the low current CDM failures. The first approach to investigate the potential impact of this effect on the DUT was to lower the pogo pin capacitance by reducing the diameter of the plunger (Fig. 7.24, left picture). If the initial discharge into the pogo pin capacitance is a critical stress parameter for the devices, a reduced pogo pin capacitance should decrease the initial CDM stress and consequently result in a higher CDM peak current failure threshold. Despite the increased inductance and a potential effect of the pogo pin geometry on the CDM discharge, the thinner plungers still provide low current failures within the peak current failure distribu-

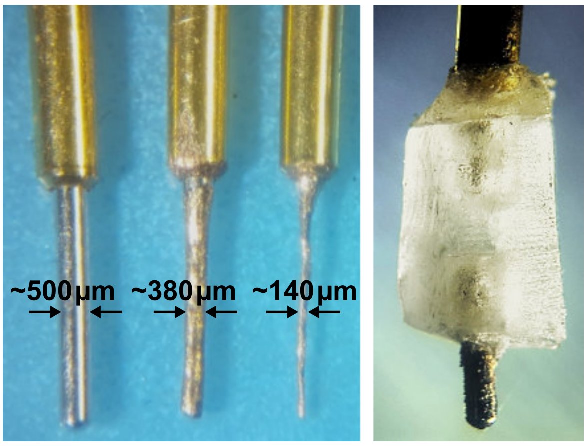

Figure 7.24 Pogo pins of different pin diameter (left) and electrically isolated tip of pogo pin (right).

tion measured with the default pogo pin (Fig. 7.16). Therefore, this first approach did not identify the pogo pin capacitance as a critical stress parameter of the DUT.

In a second approach, nearly the entire part of the spring-loaded plunger, which is located outside the barrel, was clipped. With a small poly acryl joint, an isolated tip of the pogo pin was established (Fig. 7.24, right picture). This setup enables to emulate only the initial discharge of the DUT into the pogo pin capacitance under real CDM conditions. An indicative low displacement current pulse passing through the series capacitance of the split plunger confirms the occurrence of the local discharge. The floating tip was grounded before each contact with the DUT. Assuming that the initial discharge into the effective capacitance of the tip of the pogo pin is responsible for CDM's low current failures, I/O failures should still be addressable. However, in order to create failures on the I/O pins, now a CDM test condition around TC 1000 was necessary in comparison with TC 250 ($I_\mathrm{p} \sim 2.5\,\mathrm{A}$) for the standard configuration. Consequently, the local discharge into the effective capacitance of the tip of the pogo pin is not a critical stress parameter for the investigated high-speed ICs.

The current slew rate

One key factor for the ESD susceptibility is the triggering behavior of the protection element (Section 8.3). This is related to the stress current slew rate SR, which is indirectly proportional to the rise time t_r (Eq. (6.4)) and was identified as the critical stress parameter for the small packaged IC in Section 7.3 [20]. In the studies to find the root cause of the increased yield loss, the rise times of the real world discharges, which occur during the placement of the through-hole connectors on the populated PCBs, were measured to be only few tens of picoseconds [79]. In the laboratory study, the current rise times of the first rising edges t_r1 were measured to be around 30 ps for CDM and around 45 ps for CC-TLP (Fig. 7.17). According to Equation (6.1), this roughly relates to a signal bandwidth of around 15 GHz for CDM and 11 GHz for CC-TLP. By inserting the measured bandwidths of all the single components used in the CDM and CC-TLP setup (Section 6.1.2) into Equation (6.2), the total bandwidth BW_System can be estimated to be around 16 GHz for the CDM system and around 11 GHz for the CC-TLP system. Hence, the bandwidths of the impulses are on the limit of the system bandwidths. For an absolute peak current of $\sim 5\,\mathrm{A}$ (Fig. 7.17), the corresponding slew rates of the first rising edge SR_1 were measured to be around 65 A/ns for CDM and around 45 A/ns for CC-TLP. To investigate the effect of a higher current slew rate, the bandwidth of the CC-TLP setup was increased. This required the modification of the CC-TLP stress path or the pulse generator.

Modification of the CC-TLP stress path

The simulation study in Section 8.3 will demonstrate that, if the specific dynamic of the protection element is considered, a shorter rise time (higher slew rate) will induce an increased stress across a gate oxide capacitance. To demonstrate the effect of a higher CC-TLP slew rate experimentally, the pick-off tee was removed and the pulse generator, i.e. the charged TL and its relay, was positioned directly in front of the CC-TLP probe (Fig. 7.25). The removal of the pick-off tee and with it the metrology path disables the in-situ measurement of the CC-TLP current I_{TLP}. Therefore, the peak current based had to be reconstructed on existing waveforms with the same (VF-)TLP charging voltage after reconfirming the excellent pulse repeatability. In contrast to the pass/fail distribution of default CC-TLP testing (Fig. 7.16), the resulting CC-TLP pass/fail distribution with the modified CC-TLP setup has a very sharp peak current failure threshold at around 2 A (Fig. 7.26) reaching the low current failures of CDM. The hard limit between pass and fail of the new CC-TLP failure current distribution is remarkable, in particular in view of the variation of breakdown voltages of gate oxides expected in this advanced technology node [82, pp. 5–14]. It

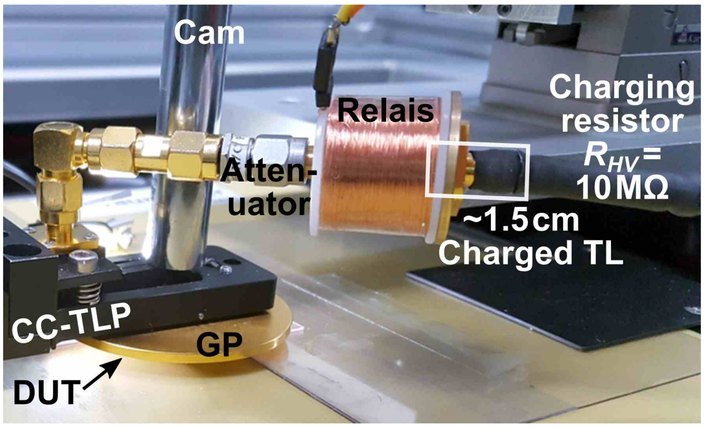

Figure 7.25 Modified CC-TLP probing set up to generate stress pulses with ultra-short rise times and very high current slew rates. A 6 dB or 10 dB attenuator behind the (VF-)TLP source is used to reduce multiple reflections.

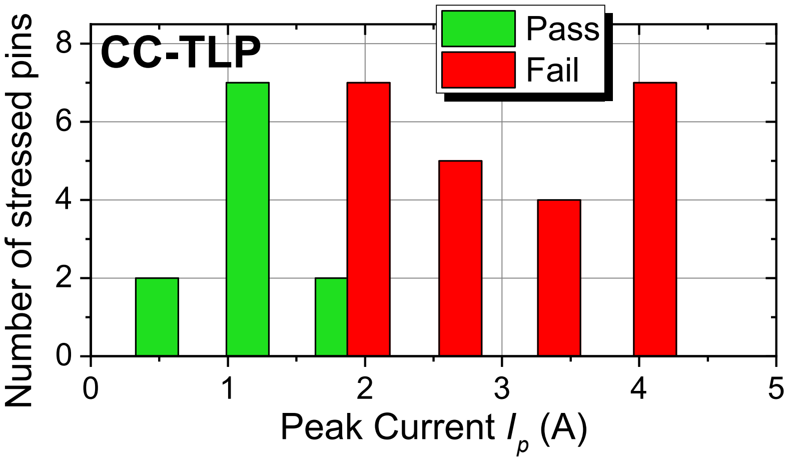

Figure 7.26 CC-TLP peak current failure distribution when stressing the IC with the modified CC-TLP probing setup, i.e. without pick-off and cables as shown in Figure 7.25.

clearly demonstrates the high reproducibility of CC-TLP. The new failure current distribution indicates that if the peak current exceeds a critical value of about 2 A, the current slew rate of the first rising edge determines the actual threshold at which the device fails.

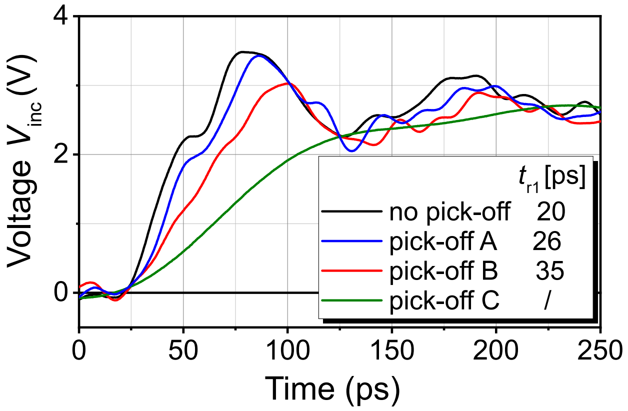

Figure 7.27 Exemplary low voltage pulses V_{inc} from the (VF-)TLP generator, propagating directly (black) or through the stress path of different pick-off tees (blue, red, green) into a 63 GHz oscilloscope with 160 GSa/s sampling rate.

To emphasize this assumption, the influence of the different pick-off tees on the rise time was evaluated. Since the real CC-TLP current cannot be recorded without metrology chain (Fig. 4.1), the incident voltage pulse $V_{\mathrm{inc}}(t)$ was analyzed by means of a 63 GHz single shot oscilloscope channel with a sampling rate of 160 GSa/s (Fig. 7.27). The higher sampling rate corresponds to one real measurement point approximately every 6 ps and is necessary for the evaluation of the fast rising edges of the pulses. The typical overshoot of the incident rectangular voltage pulse V_{inc} is based on the distinct capacitive behavior of the movable blade of the reed relay in the pulse generator, which was investigated and further improved in course of this dissertation (Section 6.1.2). The small plateau within the initial fast rising peak of the incident voltage pulse (~ 2 V) determines the first rising edge of the stress current (Fig. 7.17). In the domain of few tens of picoseconds, the limits of the measurement technology becomes apparent even for CC-TLP. However, subtle differences of some few picoseconds in the rise times t_{r1} with and without pick-off can be revealed, which, for a given peak current, translate to differences in the corresponding current slew rates (Eq. 6.4). This indicates that the slew rate SR_1 is the reason for the different pass/fail distributions between the default (Fig. 7.16) and the modified (Fig. 7.26) CC-TLP setup. The investigation further shows that the bandwidth of the stress path becomes especially important for ICs which are sensitive to the current slew rate. This effect could have a strong influence on very high-speed ICs in general.

Modification of the pulse generator

In the CC-TLP measurements with the home build (VF-)TLP pulse generator, the pick-off and with it, the metrology chain had to be removed from the setup in order to reach CDM's low current failures ($I_\mathrm{p} \sim 2.5\,\mathrm{A}$). At this point of the investigation, it was shown that this removal leads to a decrease of the current rise times of the first rising edges $t_{\mathrm{r}1}$ (Fig. 7.27) or — for a given peak current — to an increase of the current slew rate SR_1 of the incident voltage pulse. This indirectly justifies the hypothesis that the current slew rate is the critical stress parameter, which explains the initially measured peak current distributions.

The following approach allowed a direct verification of the hypothesis. By using an impedance controlled coaxial switch in ambient air [81] instead of the (VF-)TLP pulse generator, it was possible to achieve even higher slew rates, however at the expense of the excellent (VF-)TLP pulse reproducibility. This enabled the re-implementation of the removed components, i.e. the pick-off tee and cables and to measure the CC-TLP current I_TLP while simultaneously causing low current failures ($\sim 2\,\mathrm{A}$). An exemplary CC-TLP waveform generated by the coaxial switch leading to a failure of the IC before and after de-embedding of the pick-off metrology path is illustrated in Figure 4.5 (top right picture).

Figure 7.28 visualizes the absolute peak currents $|I_\mathrm{p}|$ and corresponding slew rates SR_1 measured by the CDM (●) and the default CC-TLP (▲) setup and also three data pairs of the CC-TLP setup with the modified pulse generator, which led to a failure of the IC (★).

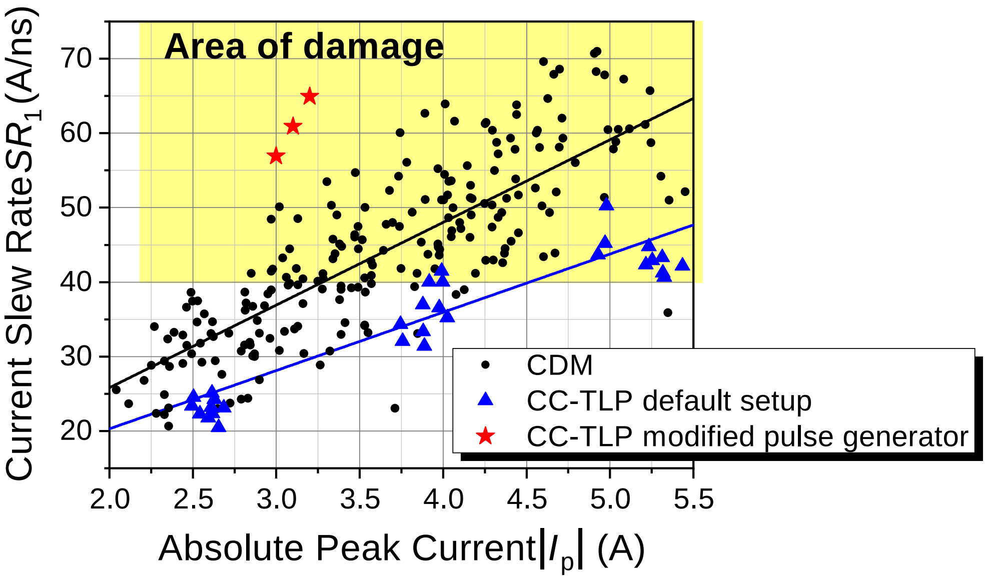

Figure 7.28 Absolute peak current - slew rate of the first rising edge SR_1 distribution of CDM (●) and default CC-TLP (▲) testing and CC-TLP testing with the modified pulse generator (★).

The yellow area ("Area of damage") marks the conditions for which failures of the high-speed devices are expected. Similar to the study in Section 7.3, this was chosen under the assumption that both a threshold current ($\sim 2\,\mathrm{A}$) and a threshold slew rate ($\sim 45\,\mathrm{A/ns}$) have to be exceeded in order to cause a failure. This is absolutely plausible given the naturally limited triggering speed of any ESD protection structure and will be verified by the simulations in Section 8.3. The threshold slew rate is partly exceeded by CDM (●) for peak currents slightly below 3.0 A, by default CC-TLP testing (▲) at around 5 A. This perfectly matches the results of the initially measured CDM and CC-TLP distribution of peak currents to failure (Fig. 7.16). The variation of the CC-TLP data points (▲) is mainly caused by the fact that it was not distinguished between different high-speed pins and corresponding waveform groups (Fig. 7.17). The huge slew rate variation of CDM data pairs (●), which is mainly caused by the air discharge [20, 21] (Fig. 7.14), is beyond the capability of the CDM metrology chain required in today's standards and explains the broader distribution and the wide pass/fail overlap in the CDM test (Fig. 7.16). From the CC-TLP measurements with the poorly reproducible coaxial switch, three data pairs, which show similar waveforms and led to a failure of the IC, were selected (★). These waveforms with a peak current amplitude around 3 A show huge slew rates of the first rising edge SR_1 of more than $\sim 55\,\mathrm{A/ns}$. This explains the appearance of first failures already around 2 A (Fig. 7.26). Overall, the initially measured miscorrelation between CDM and CC-TLP for low peak current failures ($I_\mathrm{p} \sim 2.5\,\mathrm{A}$) could be experimentally resolved through identifying the current slew rate to be a critical stress parameter for the tested high-speed devices.

7.4.6 Slew rate sensitivity of the Device under Test (DUT)

high-speed design requires impedance controlled interconnects with high electric bandwidths. This characteristic of ultra-high-speed chips, however, enables very fast ESD transients with ps-rise times to propagate with little attenuation or distortion from and to the sensitive chip. Based on the transit time of charge carriers, every ESD protection circuit has a limited triggering speed leading to a delayed response [25, p. 133]. If the response of the protection element is too slow with respect to the very fast ESD transient, a critical transient voltage overshoot occurs across the ESD protection element, which damages the gate oxide in parallel [26, 27, 71] (Section 2.1.2). This is a principal reason for the identified slew rate sensitivity of the tested ultra-high-speed device. The impact of this effect on the stress induced by CDM and CC-TLP is simulated in the parameter study in Section 8.3. Moreover, the study deals with the influence of a DC-blocking capacitor in series with the input path. This is required in many high-speed applications and is also contained in the tested high-speed devices [78].

7.4.7 Summary and conclusions

In this study, a high-speed IC was stressed by CDM and CC-TLP, initially yielding different overlapping distributions of peak currents to failure, suggesting a miscorrelation. In order to identify the root cause of this behavior, the following potentially critical stress parameters were investigated systematically:

- Differences in substrate routing
- Source impedance
- Capacitive coupling between DUT, GP and FCP
- Capacitive coupling between the plunger of the pogo pin and the GP
- Current slew rate

Only if the current slew rate is high enough, i.e. if the rise time of the initial edge of the incident pulse was reduced to some 20 ps, the CC-TLP peak failure currents displayed the favorable sharp pass/fail transition at the low tail ($I_\text{p} \sim 2.5\,\text{A}$) of the overlapping wide CDM failure current distribution. Today's limits to generate and measure pulses had to be challenged for this finding that may seriously impact the discussion on standardization of CDM and alternative stress test methods. This study employed a 33/63 GHz single shot oscilloscope, a CDM test head that exceeds a bandwidth of 18 GHz and different very-fast and ultra-fast CC-TLP setups with rise times down to some 20 ps. Although the setup will be further improved for a ps-in-situ measurement, the presented findings on rise time sensitivity directly affect the bandwidth requirements of today's CDM standards and questions the air discharge of CDM for qualification tests, even in some cases air discharge may generate the fastest possible impulses obtaining the lowest failure thresholds. The value of these exemplary findings grows in view of an increasing number of ultra-high-speed devices with impedance controlled interconnects and increasingly vulnerable gate oxides [83]. In this context, simulations will expose that the usage of a DC-blocking capacitor, which is required in many high-speed applications, could further increase the rise time or slew rate sensitivity of the device (Section 8.3.2). Given the variations of setups and number of device channels stressed in this study, consistent CC-TLP results have demonstrated that CC-TLP is a precise test method for ESD robustness analysis in the CDM domain with strong benefits for reliable and repeatable qualification tests even of critical devices.

Chapter 8

Simulation study

Completing by the results of the experimental correlation studies between CDM and CC-TLP (Section 7), the following parameter study investigates their correlation for a gate oxide failure theoretically. More specifically, it deals with the difference in peak voltages on ESD-protected elements leading to a gate oxide failure induced by CDM and CC-TLP. The simulations were performed by means of the Keysight (Agilent) ADS circuit simulation tool and mathematically verified by Wolfram Mathematica. Thereby, two parameters are of particular importance:

The first part of the study (Section 8.2) deals with the difference of the **source impedance** of CDM and CC-TLP. A widespread prejudice about CC-TLP is its incapability to reproduce CDM failures because of its higher source impedance of 50 Ω in comparison to CDM testing [17]. To produce the same stress as CDM would consequently request an adaption of the source impedance of the alternative contact-mode test method to CDM's spark resistance, as e.g. proposed by the alternative contact-mode test method, low-Z CCDM [60] (Section 4.5.2). One might speculate that a longer stress duration of the CC-TLP pulse based on its larger RC-constant can lead to a longer stress duration across the vulnerable gate oxide compared to CDM. As gate oxide structures can withstand higher voltages the shorter the stress pulses are [39], this could result in a reduced failure threshold of the gate oxide structure for CC-TLP in comparison to CDM. Nevertheless, all previous correlation studies [15–19, 71] and recent correlation studies on gate oxide failures, which have been performed in the course of this dissertation [20–22] (Section 7.3 and 7.4), demonstrated an excellent peak current threshold correlation between CDM and CC-TLP. This is particularly owed to the fact that the pulse width of the CC-TLP stress current $I_{\text{TLP}}(t)$ can be adapted by tuning the length of the charged TL in the (VF-)TLP pulse generator [18] (e.g. Fig. 2.4). Nonetheless, doubts remain because results of experimental correlation studies on some DUTs cannot be generalized for all available semiconductor devices. Besides the adaption of CC-TLP's pulse width to the stress current of CDM (Section 4.4), a CDM/CC-TLP correlation requires that both methods provide equal voltage drops across e.g. a vulnerable gate oxide structure. Therefore, a theoretical parameter study by means of generic simulation circuits was performed allowing for the explicit investigation of the impact of the source impedance on the peak voltage drop and the correlation between CDM and CC-TLP in a more general way.

The second part of the study (Section 8.3) deals with the **rise time** or **slew rate** of the stress pulse which may have an impact on the failure threshold, as already identified in the experimental correlation studies (Section 7.3 and 7.4). A high slew rate sensitivity of the DUT is mainly owed to the dynamic behavior of the ESD protection element, which cannot be simulated in a generic way. In order to still analyze the impact of the slew rate qualitatively, it was investigated exemplarily. While the slew rate of CC-TLP is highly reproducible and adaptable by implementing rise time filters into the stress path (Fig. 7.12), the slew rate of CDM shows a huge variation mainly caused by the air discharge (Fig. 7.14). Hence, the second part of the study does not deal with the conditions for a general correlation between CDM and CC-TLP, but rather with the consequences of transients with different rise times in the CDM-domain. Moreover, the study identifies the capacitance of the DC-blocking capacitor in series with the input path to be a critical factor that might lead to an increased slew rate sensitivity of the DUT.

8.1 Simulation model

8.1.1 Simulation model of the DUT

The object of investigation is the maximum voltage drop V_{IC} across an (internal) structure, which is represented by a capacitor C_{IC}, e.g. the capacitance of a gate oxide and an optional series impedance Z = R_{IC}. As depicted in Figure 8.1, it is protected by an ESD protection element D_{ESD} in parallel and enclosed by a background capacitor C_{Bg} (Fig. 2.1). In a first approximation, the ESD protection structure can be represented as a simple ohmic resistor R_{ESD}. In a more realistic model, this is replaced by an ESD protection diode D_{ESD} operating in forward-biased mode. At the port or I/O pad respectively, the stress pulse is injected.

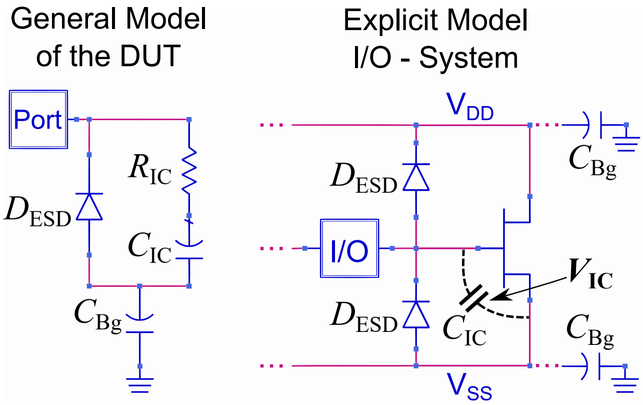
General Model
of the DUT
Port
R_{IC}
D_{ESD}
C_{IC}
C_{Bg}
Explicit Model
I/O - System
V_{DD}
D_{ESD}
C_{Bg}
I/O
V_{IC}
D_{ESD}
C_{IC}
C_{Bg}
V_{SS}

Figure 8.1 General (left) and specific (right) schematic of the system to be investigated in the simulations.

8.1.2 Simulation model of the CDM and CC-TLP tester

For the CC-TLP simulation, a stress voltage pulse with amplitude V_0, rise time t_r and pulse width t_d is injected by a voltage source with output impedance $R_{\text{S,CC-TLP}} = 50\,\Omega$. To enhance comparability, the CDM discharge is treated as a long voltage step $t_{\text{d,CDM}} \geq 30\,\text{ns}$ through an equivalent RLC model [37, 84] (Fig. 8.2).

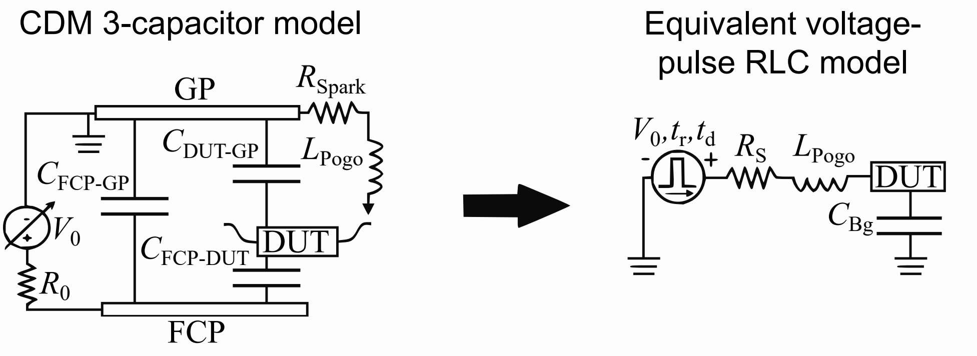
CDM 3-capacitor model
GP
R_{Spark}
$C_{\text{DUT-GP}}$
L_{Pogo}
$C_{\text{FCP-GP}}$
V_0
$C_{\text{FCP-DUT}}$
DUT
R_0
FCP
Equivalent voltage-
pulse RLC model
V_0, t_r, t_d
R_S
L_{Pogo}
DUT
C_{Bg}
-
+

Figure 8.2 The discharge of the CDM 3-capacitor model (left side) is replaced by a voltage pulse into the equivalent RLC-circuit (right side) in the simulations [37, 84].

The output impedance $R_{\mathrm{S,CDM}}$ of the CDM voltage source is mainly given by the spark resistance R_{Spark}. For an air discharge in a nitrogen atmosphere, $R_{\mathrm{S,CDM}}$ was chosen to be $28\,\Omega$ [59]. The inductance of the pogo pin L_{Pogo} is not represented through a lumped element in the simulation, since its corresponding effect can be set indirectly by the rise time t_{r} and the peak voltage V_0 of the pulse.

8.1.3 Combined simulation model

The combined schematics of CDM's and CC-TLP's simulations model, consisting of the pulse generator and the DUT introduced above, are illustrated in Fig. 8.3.

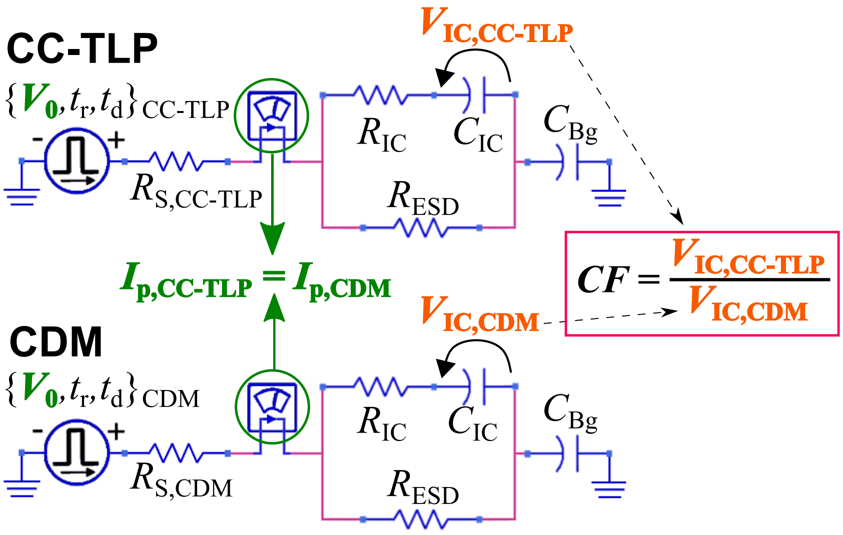
CC-TLP
$\{\boldsymbol{V_0}, t_{\mathrm{r}}, t_{\mathrm{d}}\}_{\mathrm{CC\text{-}TLP}}$
-
+
$R_{\mathrm{S,CC\text{-}TLP}}$
$\boldsymbol{V_{\mathrm{IC,CC\text{-}TLP}}}$
R_{IC}
C_{IC}
C_{Bg}
R_{ESD}
$\boldsymbol{I_{\mathrm{p,CC\text{-}TLP}}} = \boldsymbol{I_{\mathrm{p,CDM}}}$
$\boldsymbol{V_{\mathrm{IC,CDM}}}$
$\boldsymbol{CF} = \dfrac{\boldsymbol{V_{\mathrm{IC,CC\text{-}TLP}}}}{\boldsymbol{V_{\mathrm{IC,CDM}}}}$
CDM
$\{\boldsymbol{V_0}, t_{\mathrm{r}}, t_{\mathrm{d}}\}_{\mathrm{CDM}}$
-
+
$R_{\mathrm{S,CDM}}$
R_{IC}
C_{IC}
C_{Bg}
R_{ESD}

Figure 8.3 Schematics of CC-TLP (top) and CDM (bottom) simulation model.

Table 8.1 summarizes the parameters that are used in the simulation (Figure 8.3). The numbers in brackets denote the potential range of the parameter variation, the single bold numbers indicate the default values used in the simulation. A prerequisite for the comparison of the CDM/CC-TLP stress voltages induced across the gate oxide is that both methods provide the same peak current $\boldsymbol{I_{\mathrm{p}}}$ (Fig. 8.3, green). In real measurements, this criterion is fulfilled by calibrating the CC-TLP pulse voltage $\boldsymbol{V_{\mathrm{0,CC\text{-}TLP}}}$ with respect to the CDM stress. CDM's and CC-TLP's equivalent circuits differ according to their system impedances R_{S}, pulse lengths t_{d} and rise times t_{r} of their voltage pulses. Hence, with respect to a given CDM voltage $\boldsymbol{V_{\mathrm{0,CDM}}}$, a different pulse voltage $\boldsymbol{V_{\mathrm{0,CC\text{-}TLP}}}$ has to be set for CC-TLP to fulfill the calibration requirement ($\boldsymbol{I_{\mathrm{p,CC\text{-}TLP}}} \overset{!}{=} \boldsymbol{I_{\mathrm{p,CDM}}}$). In the simulation, this is done by means of an optimization routine that minimizes the peak current difference of CDM and CC-TLP for a given set of parameters before each measurement. In the case of a linear system, i.e. usage of resistances instead of protection diodes as protection elements, a post correction of the simulated voltage drops by means of the peak current is also possible.

The critical stress parameter is the resulting maximum voltage drop $\boldsymbol{V_{\mathrm{IC}}}$ across the capacitance C_{IC} (Fig. 8.3, orange). For equal peak currents ($\boldsymbol{I_{\mathrm{p,CC\text{-}TLP}} \overset{!}{=} I_{\mathrm{p,CDM}}}$), the quotient of CC-TLP's and CDM's peak voltage drop defines the factor of correlation:

$$\boldsymbol{CF} := \frac{V_{\mathrm{IC,CC\text{-}TLP}}}{V_{\mathrm{IC,CDM}}} \qquad (8.1)$$

Table 8.1 Parameters used in the simulation.

		(FI)CDM	**CC-TLP**
Discharge pulse-specific	$\boldsymbol{R_{\mathrm{S}}}$	(5 Ω - 80 Ω) **28 Ω**	**50 Ω**
	$\boldsymbol{t_{\mathrm{d}}}$	(≙ DC) $\gtrsim$ **30 ns**	30 ps - 20 ns
	$\boldsymbol{t_{\mathrm{r}}}$	(10 ps - 200 ps) **100 ps**	
	$\boldsymbol{V_0}$	arbitrary value	voltage that creates a peak current equal to CDM
		$I_{\mathrm{p,CC\text{-}TLP}} \overset{!}{=} I_{\mathrm{p,CDM}}$	
DUT-specific	$\boldsymbol{C_{\mathrm{Bg}}}$	(0.5 pF - 5000.0 pF) **20.0 pF**	
	$\boldsymbol{R_{\mathrm{IC}}}$	**0 Ω**	
	$\boldsymbol{C_{\mathrm{IC}}}$	(1.0 fF - 5 pF) **1.0 pF**	
	$\boldsymbol{R_{\mathrm{ESD}}}$	100 mΩ - 100 kΩ	

A correlation of both methods is given, if *CF* lies within a range of ±3% around 1.00, i.e. the simulation denotes a voltage understress of CC-TLP with respect to CDM for $CF < 0.97$ and a CC-TLP voltage overstress with respect to CDM for $CF > 1.03$.

8.2 Generic analysis of the CDM/CC-TLP correlation

The subject to be analyzed concerns possible CC-TLP overvoltages across vulnerable gate oxides caused by the larger RC-constant of the CC-TLP stress pulses 50 Ω [17]. To resolve this matter, the correlation factor *CF* for different parameter configurations was examined. The color-coded graphs in Figure 8.4 depict, as a representative example, the correlation factor *CF* in dependence on the CC-TLP pulse width $\boldsymbol{t_{\mathrm{d,CC\text{-}TLP}}}$ and the resistance $\boldsymbol{R_{\mathrm{ESD}}}$ of the ESD-protection element for two different capacitances $\boldsymbol{C_{\mathrm{IC}}}$. The dashed lines in Figure 8.4 distinguish the regions for a functional ESD-protection (region R2: $R_{\mathrm{ESD}} < 10\,\Omega$) from the regions with a "high ohmic ESD-protection" (region R1: $R_{\mathrm{ESD}} > 10\,\Omega$). A "high ohmic ESD-protection" can be interpreted as the lack of a functional protection element or as a protection structure with a too slow triggering speed. Figure 8.4 shows the influence of the

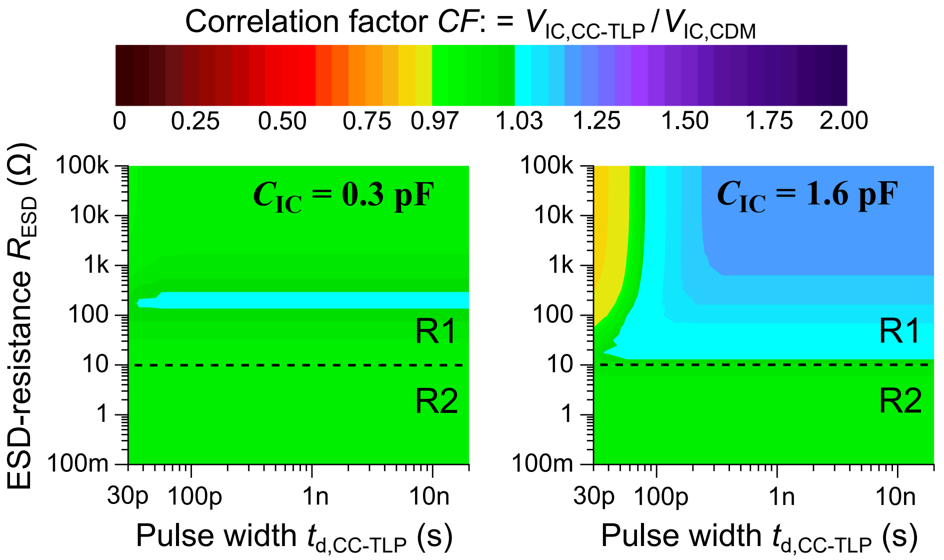

Figure 8.4 Color-coded correlation factor *CF* for two different capacitances C_{IC}. All the other variables are set to their default values given in Table 8.1 (single bold numbers).

source impedance with respect to gate oxide failures. Setting all the other parameters to their default values given in Table 8.1, the following applies:

The maximum voltage drops of CDM testing and CC-TLP across the capacitor C_{IC}, e.g. across a gate oxide capacitance, will **only miscorrelate** ($CF < 0.97$ or $CF > 1.03$), if the capacitance of the stressed structure is very high ($\boldsymbol{C_{\mathrm{IC}} \gtrsim 1\,\mathrm{pF}}$) **and** if there is no useful protection element (region R1: $\boldsymbol{R_{\mathrm{ESD}} \gtrsim 10\,\Omega}$). This confirms what had been experimentally demonstrated in all previous CDM/CC-TLP correlation studies on gate oxide failures so far [20–22, 15–18, 71](Section 7.3 and 7.4): Even though CC-TLP is based on a 50 Ω impedance, its peak current failure threshold correlates with the one of CDM except in exceptional circumstances. The general validity of this statement was checked by examining the influence of all the other variables within the listed ranges (brackets in Table 8.1):

Taking into account the air discharge, the CDM spark resistance and in turn the CDM source impedance $\boldsymbol{R_{\mathrm{S,CDM}}}$ may vary for each pulse. A smaller resistance $R_{\mathrm{S,CDM}}$ than the chosen default value of 28 Ω increases an existing overvoltage of CC-TLP with respect to CDM for large C_{IC} in region R1 (Fig. 8.4). For larger spark resistances, up to 50 Ω, the CC-TLP overvoltage decreases and even becomes an undervoltage for values larger than 50 Ω.

In general, the background capacitance $\boldsymbol{C_{\mathrm{Bg}}}$ shows nearly no influence on the simulation results. For very small background capacitances of only a few picofarad, the overvoltage in region R1 disappears (Fig. 8.4).

Since the variation of the resistor $\boldsymbol{R_{\mathrm{IC}}}$ that is connected in series with capacitor C_{IC} shows only a slight increase or decrease of the correlation factor *CF*, it was set to 0 Ω.

8.3 Rise time (slew rate) sensitivity of the DUT

An interesting quantity within this simulation is the rise time $\boldsymbol{t_\mathrm{r}}$ or the slew rate $\boldsymbol{SR}$ respectively of the CDM and CC-TLP stress pulses. As identified in the experimental correlation studies (Section 7.3 and 7.4), they may have an impact on the failure threshold. How this behavior can be interpreted according to the results of the simulation is discussed in the following.

8.3.1 Rise time t_r and the ESD protection element

The impact of the rise time on the peak voltage V_IC in the simulation depends on the ESD protection structure.

Simplified ESD protection element model

According to Section 8.2, for a functional ESD protection element represented by a low ohmic resistor R_ESD, the simulations shows an excellent CDM to CC-TLP-correlation ($CF \approx 1$) independent on the rise times of CDM and CC-TLP (Fig. 8.4, region R2). In absence of a functional protection element, represented by a resistor $R_\mathrm{ESD} > 10\,\Omega$ (Fig. 8.4, region R1), stress pulse with a shorter rise time would tend to result in a smaller peak voltage across the capacitor C_IC (Fig. 8.5). This, at a first glance rather counterintuitive relationship was extensively derived in [21]. The behavior can be explained as follows:

During charging of a capacitor with a trapezoidal stress pulse (a rectangular pulse with a rising and a falling edge), the peak charging current increases if the pulse rise time is reduced (Fig. 8.6).

If, for example, the rise time of the CC-TLP stress pulse is shorter than for CDM ($t_\mathrm{r,CC\text{-}TLP} < t_\mathrm{r,CDM}$), then CC-TLP would show an increased peak current with respect to CDM ($I_\mathrm{p,CC\text{-}TLP} > I_\mathrm{p,CDM}$). In order to match

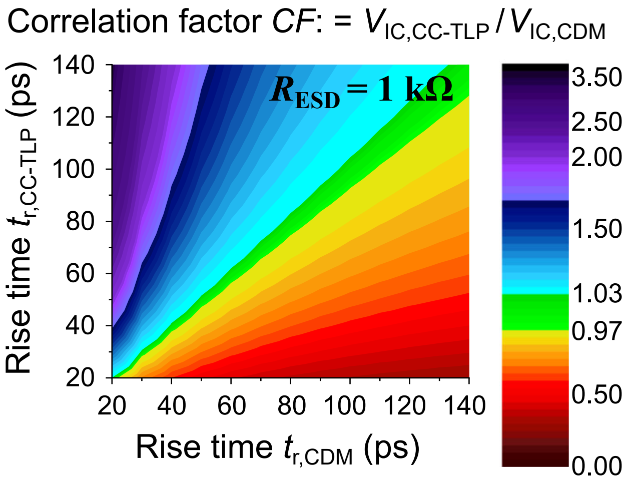

Figure 8.5 Correlation factor CF in dependence on the rise time of CDM and CC-TLP for a transient voltage drop across a capacitor $C_\mathrm{IC} = 0.1\,\mathrm{pF}$ without functional protection element (high ohmic resistor $R_\mathrm{ESD} = 1\,\mathrm{k\Omega}$). The pulse width of the CC-TLP stress pulse was set to $t_\mathrm{d,CC\text{-}TLP} = 3\,\mathrm{ns}$. All the other variables are set to their default values given in Table 8.1 (single bold numbers).

the peak currents of CDM and CC-TLP ($I_{\text{p,CC-TLP}} \overset{!}{=} I_{\text{p,CDM}}$), it would be necessary to compensate for the increased peak current $I_{\text{p,CC-TLP}}$[1] by reducing the pulse voltage $V_{0,\text{CC-TLP}}$. However, since the peak voltage drop V_{IC} across the capacitor C_{IC} primarily depends on the pulse voltage $V_{0,\text{CC-TLP}}$ and on the resistance of the high ohmic ESD element R_{ESD} in parallel, this would eventually lead to a reduced peak voltage of CC-TLP across the capacitor C_{IC} (Fig. 8.5). This rise time to stress behavior changes by using a more realistic model for the ESD protection element as described in the following.

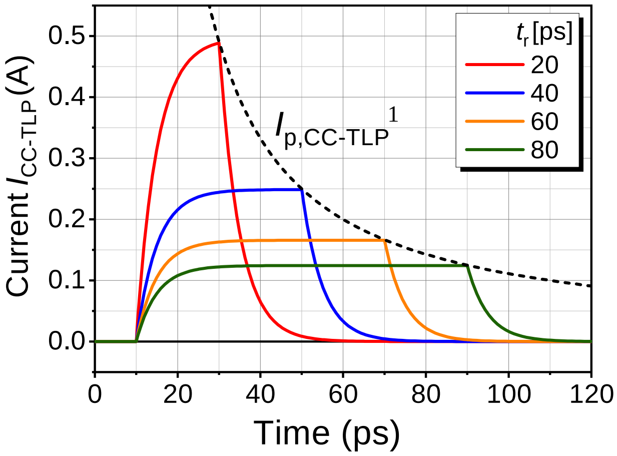

Figure 8.6 Charging of a capacitor ($C_{\text{IC}} = 0.1\,\text{pF}$) in dependence on the rise time t_r of the trapezoidal CC-TLP stress pulse ($R_S = 50\,\Omega$).

Non-linear ESD protection element model

For a more realistic model of the ESD protection element, the interaction of the transient's rise time with the ESD protection structure regarding its dynamic behavior has to be considered. The decisive factor is the limited triggering speed of every ESD protection element, which is already given by the transit time of charge carriers [25, p. 133]. Depending on the transient's rise time, the delayed response of the protection element results in a transient voltage overshoot that occurs across the ESD protection element [26, 27, 71]. The turn-on behavior under CDM-like ESD conditions is a specific characteristic of every ESD protection element and thus cannot be simulated in a generic way.

In order to analyze this effect qualitatively, it was investigated exemplarily by replacing the simple ohmic resistor R_{ESD} by an ESD diode $\boldsymbol{D}_{\text{ESD}}$ operating in forward-biased mode (Fig. 8.1). The shorter the pulse rise time, the higher the transient voltage overshoot across the ESD protection element. This in total leads to an increased voltage drop across C_{IC} as demonstrated in Figure 8.7. This relationship between rise time and peak voltage is opposite to the simulation results with the simplified ESD protection element R_{ESD} (Section 8.3.1). The quantity of *CF* (Fig. 8.7) strongly depends on the specific transient characteristic of the protection diode, which was arbitrary chosen in this simulation to illustrate this effect. The small deviation of the correlation zone ($0.97 < CF < 1.03$, green area) from the dashed line through the origin with a slope of 1 is owed to the difference of CDM's and CC-TLP's source impedance. In accordance with the experimental correlation studies (Section 7.3 and 7.4), the simulations with the protection Diode D_{ESD} confirm the increasing failure rates for stress pulses with higher slew rates. Nevertheless, as the rise time (slew rate) in CC-TLP is adaptable (Section 4.4) and can be tuned to the one of CDM, a correlation between CDM and CC-TLP should always be possible as experimentally demonstrated in Section 7.4.5.

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[1] $I_{\text{p,CC-TLP}} = I_{\text{CC-TLP}}(t_r) = \frac{2U_0C_{\text{IC}}}{t_r}\left(1-\exp\left(-\frac{t_r}{R_SC_{\text{IC}}}\right)\right)$

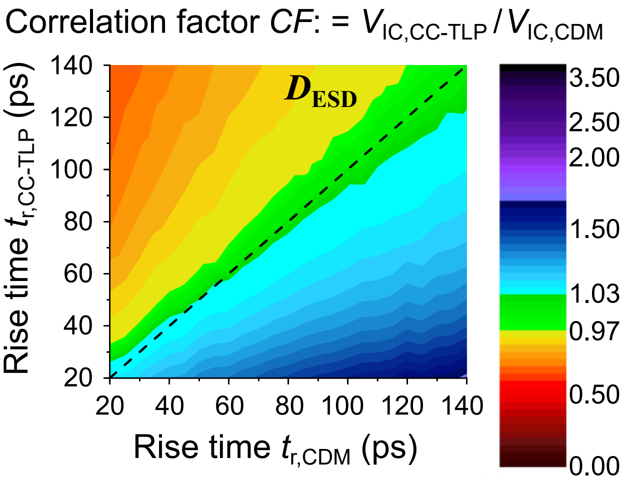

Figure 8.7 Correlation factor CF in dependence on the rise time of CDM and CC-TLP for the transient voltage drop across a capacitor $C_{\mathrm{IC}} = 0.1\,\mathrm{pF}$, which is protected by a diode D_{ESD} in forward-biased mode with a delayed turn-on behavior. The pulse width of the CC-TLP stress pulse was set to $t_{\mathrm{d,CC\text{-}TLP}} = 3\,\mathrm{ns}$. All the other variables are set to their default values given in Table 8.1 (single bold numbers).

8.3.2 Impact of the DC-blocking capacitor on the slew rate sensitivity

After having investigated the dynamic behavior of the protection element, this section deals with additional factors that affect the sensitivity of a DUT towards the slew rate of incoming stress pulses. The implementation of impedance controlled interconnects with high electric bandwidths is a characteristic of ultra-high-speed chips. However, they allow very fast ESD transients to propagate with little attenuation or distortion from and to the sensitive chip which might lead to an increased slew rate sensitivity of the DUT as experimentally identified in Section 7.4. Besides that, DC-blocking capacitors in series with the input paths are often required in many high-speed applications [78]. The following simulation analyzes the influence of these a DC-blocking capacitors on the slew rate sensitivity of the DUT.

In the underlying simulation, generic voltage pulses with variable rise times $\boldsymbol{t_r}$ were generated to propagate across a DC-blocking capacitor with a capacitance $\boldsymbol{C_{\mathrm{DC}}}$ into a **RC element**, which represents the effective resistance and background capacitance of the DUT.

Thereby, the peak current of the pulse that has passed the DC-blocking capacitor $\boldsymbol{I}_\mathbf{p}$ as well as the peak current of the pulse if no DC-blocking capacitor is implemented $\boldsymbol{I}_\mathbf{0}$ was determined. The quantity $\boldsymbol{\xi}_\mathbf{DC} = \boldsymbol{I}_\mathbf{p}/\boldsymbol{I}_\mathbf{0}$ describes the ratio between the peak current with and without a DC-blocking capacitor and thus represents the influence of the DC-blocking capacitor on the peak current. The top, color-coded diagram in Figure 8.8 illustrates ξ_DC in dependence on the initial rise time t_r of the stress pulse and the capacitance of the DC-blocking capacitor C_DC.

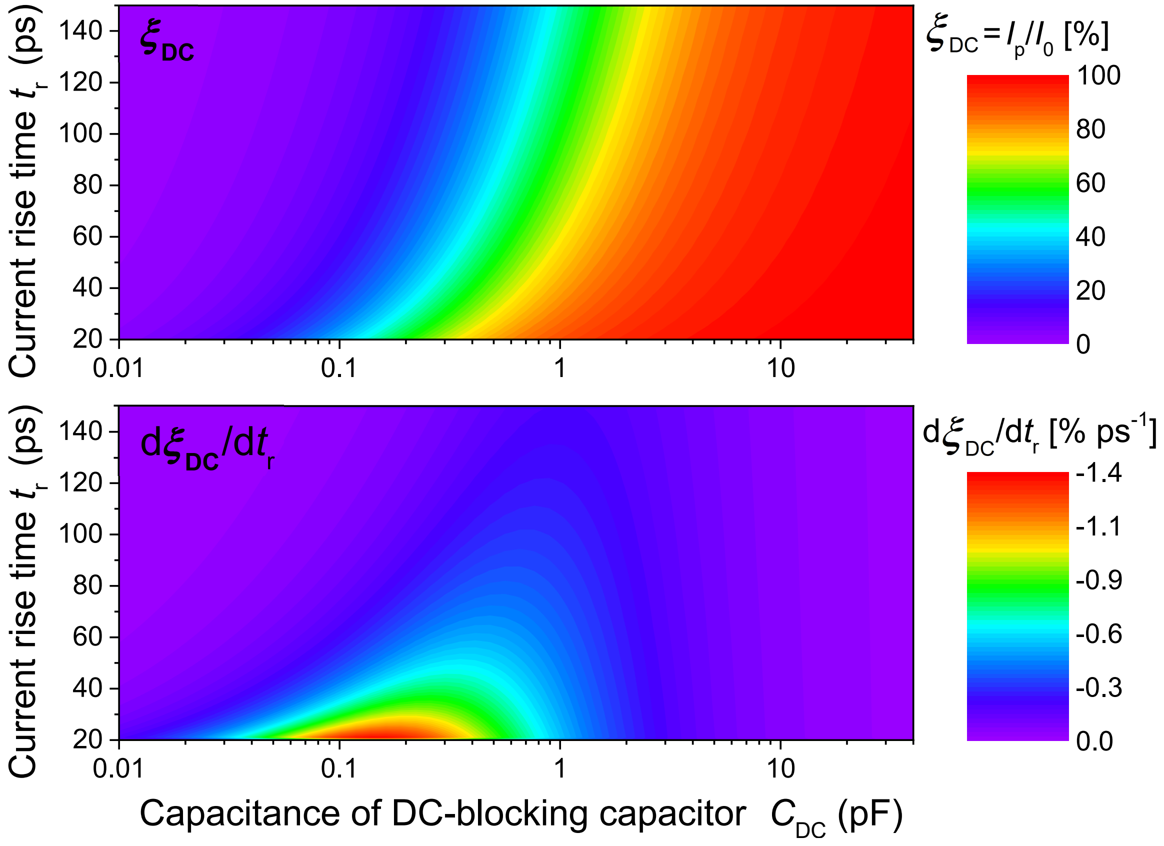

Figure 8.8 Peak current preservation $\xi_\mathrm{DC} = I_\mathrm{p}/I_0$ after a DC-blocking capacitor with capacitance C_DC in dependence on the initial rise time t_r (top) and corresponding variation with respect to an initial rise time variation $\mathrm{d}\xi_\mathrm{DC}/\mathrm{d}t_\mathrm{r}$ (bottom).

While, as expected, a high capacitance has less influence on the transient, a low capacitance is able to diminish the incoming pulse completely. Based on the functionality of a DC-blocking capacitor, pulses with higher rise times generally show a stronger decrease in their peak current than pulses with lower rise times. Thus, ξ_DC can be interpreted as the percentage preservation of the peak current after passing the DC-blocking capacitor. As already indicated by an increased density of contour lines (Fig. 8.8, top plot), the change of ξ_DC with respect to a variation of the rise time is particularly strong for capacitances between 0.1 pF and 1 pF.

To visualize this relationship more clearly, the derivative of the peak current preservation with respect to a rise time variation $\mathbf{d}\boldsymbol{\xi}_{\mathbf{DC}}/\mathbf{d}\boldsymbol{t}_{\mathbf{r}}$ is plotted (Figure 8.8, bottom plot). The plot illustrates that the impact of a rise time variation $\mathrm{d}t_{\mathrm{r}}$ on the peak current preservation after the DC-blocking capacitor ξ_{DC} is strongly dependent on the capacitance C_{DC} and has a maximum between 0.1 pF and 1 pF. Consequently, a DC-blocking capacitor with a capacitance within this range would rather cause a miscorrelation between stress pulses with equal amplitude but slightly different rise times or slew rates. Hence, in addition to the dynamic behavior of the protection diodes and the impedance controlled interconnects with high electric bandwidths, the capacitance of the DC-blocking capacitor could be another reason for the significant slew rate or rise time sensitivity of the tested high-speed ICs in Section 7.4.

8.4 Summary and conclusions

The variation of all the parameters considered in the simulation verified that a voltage drop miscorrelation between CDM and CC-TLP on an (internal) structure C_{IC} (e.g. a gate oxide) is primarily only expectable for extremely large structures ($C_{\mathrm{IC}} \gtrsim 1\,\mathrm{pF}$) without functional ESD protection element (Fig. 8.4, region R1: $R_{\mathrm{ESD}} \gtrsim 10\,\Omega$). Even though CC-TLP is based on an impedance of $50\,\Omega$, the simulation results confirm a general correlation between CDM and CC-TLP. This complies with the results that have been gathered experimentally in all the CDM to CC-TLP-correlation studies on gate oxide damages so far [20–22, 15–19, 71] (Section 7.3 and 7.4). Thus, an adaption to CDM's spark resistance, as e.g. proposed by the alternative contact-mode test method, low-Z CCDM [60] (Section 4.5.2), seems not to be required.

If the DUT has a high slew rate (rise time) sensitivity, which means that the peak current threshold of a DUT is reduced for faster stress pulses, transients with different rise times in the CDM-domain could result in a miscorrelation (Fig. 8.7). Depending on the dynamic behavior of the protection element, a slower rise time (higher slew rate) would thereby lead to an overstress (Fig. 8.7). This is consistent with the results of the experimental correlation studies (Section 7.3 and 7.4). However, a CDM/CC-TLP miscorrelation can be prevented by tuning the rise time of CC-TLP with respect to CDM (Section 7.4.5). Moreover, it was demonstrated that a DC-blocking capacitor in series with the input path with a capacitance C_{DC} between 0.1 pF and 1 pF might further contribute to an increased slew rate sensitivity of the DUT.

Chapter 9

Conclusion

Starting with a comprehensive overview of different ESD phenomena and prevalent ESD test methods and summarizing the current state-of-the-art and research, this thesis introduces the reader into the field of ESD (Chapter 1 and 2). It indicates a fundamental problem concerning ESD qualification at device level, namely the very limited reproducibility and repeatability of the standardized Charged Device Model (CDM) testing method, caused by the hardly controllable air discharge variation. Prevailing circumstances, such as technology scaling towards the single-digit nanometer scale or the enormous increase of data rates of high-speed ICs result in a growing need for an improved CDM test precision and monitoring (Chapter 3). This fact in combination with the deficiencies of the CDM test method to fulfill present-day and upcoming ESD requirements have aroused the development of an alternative, contact-mode test method called Capacitively Coupled Transmission-Line Pulsing (CC-TLP) [13, 14] (Chapter 4). In order to verify the ability of CC-TLP to replicate real world CDM events, which was a main objective of this thesis, correlation studies between CDM and CC-TLP for different technologies have been conducted. This thesis extends the previously, successfully demonstrated CDM/CC-TLP correlations for gate oxide failures of less advanced technologies [15–19] through profound investigations on more advanced technologies, i.e. a large Chip-on-Flex (COF) assembly (Section 7.2), a tiny packaged IC in a 0.25 µm BCD technology (Section 7.3) and an ultra-high-speed CMOS IC for network applications (25 Gbps) (Section 7.4), which do not show a simple correlation regarding the peak current. One of the main findings of these studies is that dealing only with peak currents as failure thresholds may not be sufficient, as there might exist additional critical stress parameters, e.g. the current slew rate, impulse shape, energy content or the number of stress pulses. Despite decades of application, there is still a significant lack of understanding about these influences, particularly because the investigation of these parameters is not directly addressable by the poorly reproducible CDM test method. Thanks to the high reproducibility of CC-TLP, its wafer level capabilities and the possibility to control parameters like the rise time, the pulse width or the capacitive coupling of the Device under Test (DUT), this thesis is one of the first to directly reveal and analyze these potential critical stress parameters for advanced semiconductor technologies at device and wafer level. This seems to be the key to significantly improve CDM qualification procedures for classifying CDM sensitivities in the future.

As a result, this work contains the first CC-TLP analysis of a pn-junction failure and thereby demonstrates a correlation that is more closely related to the dissipated energy or the number of stress pulses than to peak current (Section 7.2). For this, issues like the feasibility of CDM and CC-TLP stress tests on a large COF assembly in which the Ground Plane (GP) does not even overlap the sensitive chip, or the influence of capacitive and inductive coupled traces to the chip had to be considered and investigated. The analysis of data showed that the, according to current CDM standards [10, 34–36] relatively freely selectable, number of CDM pulses per pin and voltage level had a direct influence on the degradation and ultimately on the failure threshold of the DUT. This led to the question about the appropriate number of CDM multizaps that are commonly used to reduce sensitivity towards outliers that do not reach the nominal peak current level. Despite years of conflicts between reproducibility and test time reduction, this thesis is to the knowledge of the author the first to quantify the benefit of multizaps for CDM statistically.

The second CDM/CC-TLP correlation study of this thesis investigates a tiny packaged IC in a 0.25 µm BCD technology and demonstrates exemplarily how CC-TLP test results can resolve discrepancies that occurred during qualification tests employing three different CDM testers (Section 7.3). Thereby, the current slew rate firstly appeared as a critical stress parameter which means that both, a threshold current and a threshold slew rate have to be exceeded in order to cause a failure.

An identical relation was revealed for the ultra-high-speed CMOS IC (25 Gbps) for today's data transmission (Section 7.4). By entering the single-digit picosecond domain, today's limits to generate, propagate and measure pulses had to be challenged for this finding. Only careful de-embedding of the pulses after analysis of the transfer function of the metrology setup provided access to this domain. Circuit simulation of a simplified generic high-speed input varying the capacitance of the DC-blocking capacitor strongly indicates a relationship between the rise time sensitivity and the capacitance. Increasing the source impedance of CDM to the 50 Ω of the CC-TLP by means of adding resistance to the pogo pin did not change the failure threshold, particularly because the pulse width of CC-TLP can be adjusted to match the CDM pulse width. The generality of this statement was verified by a parameter simulation study, which investigates the CDM/CC-TLP correlation from a theoretical point of view (Chapter 8). This is an essential message as it substantiates that an adaption to CDM's spark resistance, as proposed by the alternative contact-mode test method low-Z CCDM [60] (Section 4.5.2), is not required.

All studies so far demonstrated an excellent correlation between CDM with precisely in-situ monitored discharge currents and the CC-TLP method. In some cases, related to the complex interaction between the tester and the DUT, stress parameters beyond the peak discharge current were identified to have a critical influence on the failure threshold. In today's CDM tests according to the standard, these influences are obfuscated by the variability of the air discharge and the limitations of metrology. If at all, they surface as unusual distributions of failure thresholds between tests and CDM-testers. Apart from that, this thesis illustrates how the high reproducibility of CC-TLP can be used to identify different types of ground nets of an IC. Moreover, it introduces an innovative method of scanning the electrostatic surface potential across DUTs in order to gain a deeper insight into the electrostatic behavior of the DUT providing required information for ESD-relevant countermeasures.

In the ps-domain, the limits of today's measurement technology become apparent even for CC-TLP (Section 7.4). In order to be prepared for ultra-high-speed devices of future generations, a further improvement of the bandwidths of all components, especially the CC-TLP pick-off, will be necessary. For future work, it might also be worth to put a deeper focus on the unique wafer level capability of CC-TLP and to exhaust its limits through further correlation studies of high-end technologies at wafer level and bare dies.

This thesis has addressed major challenges involved with device and wafer testing in the CDM domain. All the findings of this thesis demonstrate the tremendous potential of CC-TLP. Its high reproducibility and repeatability, its additional wafer level capability and its ability to control and tune parameters like pulse width, rise time and capacitive coupling are strong benefits for reliable and repeatable qualification tests in the CDM domain. Considering previous work [15–19] in addition to the findings of this thesis and underlying publications [5, 20–22, 12], CC-TLP has reached a level of maturity that demands for standardized CDM stress testing to be complemented or even replaced by corresponding CC-TLP tests. This thesis should impact the discussions on ESD testing of future technologies and the standardization of CDM and alternative stress test methods.

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Appendix A

Prevalent ESD models and test methods

The following table provides a brief overview of all prevalent ESD test methods.

Table A.1 Overview of ESD test methods. Click on test method for description.

ESD model/ test method	**App. level**	**Regulation**	**Type and characteristics**
	w: wafer d: device s: system	s: standardized stm: stand. test method sp: stand. practice x: no guidelines	
HBM	d	s [85]	Human discharge through DUT to ground
HMM	d	sp [86]	IC evaluation with regard to system level stress
CDM	d	s [10, 34–36]	Fast, high current discharge of charged DUT
CC-TLP	w/d	sp in progress	Alternative contact-mode test method in CDM domain
low-Z CCDM	d	sp in progress	Alternative contact-mode test method in CDM domain
TLP	w/d	stm [87]	Long pulse ($\sim 100\,\mathrm{ns}$) characterization of ESD protection structures
VF-TLP	w/d	stm [87]	Short pulse ($\sim 1\,\mathrm{ns}$) characterization of ESD protection structures
IEC 61000-4-2	s	s [88]	Human with a small piece of metal discharge through DUT to ground
TLU	s	sp [89]	Transient turn-on of parasitic npnp-structures during operation
CDE	s	x (broad cable variety)	Connecting of a charged cable into a connector during operation
CBM	s	x (broad board variety)	Discharge of entire PCB capacitance to ground

An introduction of prevalent ESD test methods aims to raise awareness of the existence of different failure mechanisms and critical stress parameters, which play a major role in the course of this thesis. This thesis focuses on CDM testing (Section 2.1.1) and alternative contact-mode test methods like CC-TLP (Chapter 4 and onwards) and low-Z CCDM (Section 4.5.2), which are based on the concept of (VF-)TLP (Section 2.2). The HBM as well as several test methods at system level are not subjects of this thesis. Nevertheless, to provide an entire overview of all existing ESD test methods, they are briefly introduced in the following appendix.

A.1 The Human Body Model (HBM)

By means of the triboelectric effect, e.g. by walking across a carpeted floor or wearing nylon clothes, the human body capacitance is able to charge up to some 10 kV with respect to ground [4, p. 10]. An interesting fact is that, when touching a metal object after being charged, one is only able to "feel" an ESD discharge if the potential difference to the object was at least 2.5 kV [3, p. 2]. If the metal object is a pin or pad of a grounded IC, however, voltages below 100 V can already be enough to induce an ESD damage [46]. This kind of ESD-phenomena is described by the Human Body Model (HBM). First approaches towards the HBM can be found in the mining industry in the 1950s [90], where explosions of gas mixtures detonated by ESD have been investigated. Around thirty year later, the first HBM standard was defined by the US military [91]. A HBM event involves at least two pins, whereby the capacitance of the charged person discharges into a pin of the device, via a specified path through the IC and via the grounded pins to ground (Fig. A.1). Pulse widths of the HBM stress current waveforms I_{HBM} are typically around 100 ns and typically lead to a thermal damage and power driven failure in the pn-junctions of e.g. protection devices [4]. As precaution of HBM events,

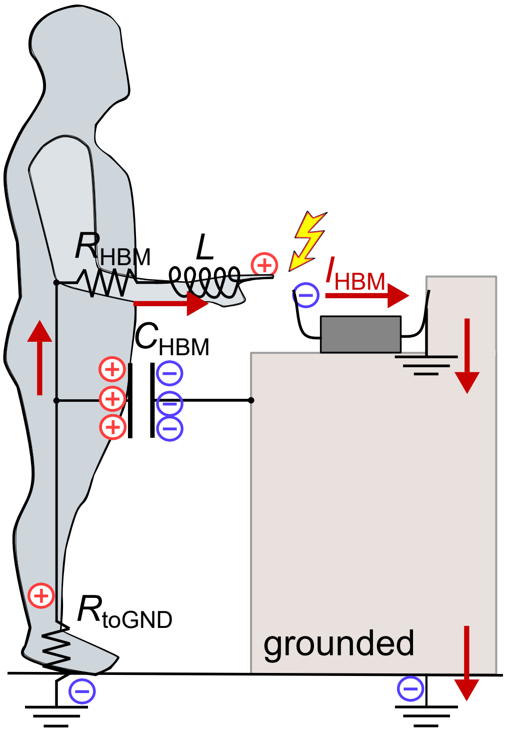

Figure A.1 Discharge according to the HBM. The circuit diagram within the schematic illustrates the principle of HBM testing.

the person to ground resistance R_{toGND} has to be less than 40 MΩ in order to limit the body voltage to less than 100 V [46]. For this purpose, e.g. ESD shoes or ESD grounding straps on the wrist are used in order to prevent the human from charging during manual handling of semiconductor devices and ESD control measures at the factory level are employed.

Human Body Model (HBM) testing

The HBM event can be modeled by an equivalent RC circuit shown in Figure A.1. The standardized capacitance $C_{\mathrm{HBM}} = 100\,\mathrm{pF}$ [85], representing the capacitance of the human body, is charged up to a specific voltage. A switch simulates the touching of the device's pin or pad by triggering the discharge via a resistance $R_{\mathrm{HBM}} = 1.5\,\mathrm{k\Omega}$, imitating the resistance of the human body. The charge flows via an input pin along a specific path through at least one output pin of the DUT to ground. The HBM network provides damped double-exponential waveforms of single polarity [92, p. 77] with a characteristic decay time that is given by $\tau_{\mathrm{HBM}} = R_{\mathrm{HBM}} C_{\mathrm{HBM}}$ and is typically around 150 ns. HBM testers typically provide an automated relay matrix to stress all pin combinations of the major HBM current paths. In principle, HBM can occur between each pair of two pins. However, testing each pair of two pins individually would result in a quite long testing time (>1 h for a package with 64 pins, assuming one zap per second). In most cases, it is sufficient to only stress those pin combinations, which will provide the worst-case conditions. Thus, in order to save test time and to reduce potential overstress, all the pins have to be classified as supply pins or non-supply pins (e.g. I/O pins, clock, etc.) and no connects, and are partitioned into different groups. Then they are HBM stressed in specific pin combinations following specific rules [85]. While for instance each I/O pin had to be HBM stressed with respect to each independent supply pin in the HBM standard of 2010, the later version of the standard [85] requires each IO pin to be stressed only with respect to the supply pins that are directly associated with that IO pin to further reduce the test time. A device has failed the HBM stress, if it does not meet the data sheet parameters using parametric and functional testing after the HBM test. Depending on the end customer applications, the DUT has to meet a HBM robustness level of several Kilovolts.

A.2 System level ESD stress models and test methods

After having ensured an adequate ESD protection in manufacturing by means of CDM and HBM tests on device level, the ESD vulnerability of electronic products in powered state and during operation under real-world ESD stress conditions in the system end-user environment has to be investigated. In contrary to the ESD controlled environment in manufacturing, no ESD stress precautions can be expected in the uncontrolled end-user environment. As the number of portable, i.e. not grounded, devices steadily increases worldwide [47] (e.g. handheld mobile devices, laptops, etc.), system level ESD testing has gained considerable interest.

IEC 61000-4-2

On system level, several possible ESD scenarios are conceivable. For instance, a charged human could touch an exposed port, e.g. an I/O connector pin, with his finger or even by means of a metallic tool, e.g. a screwdriver and discharges directly into the system's electrical circuits. The discharging of a charged person holding a metal object into a system is replicated by the system level IEC standard 61000-4-2 [88] or ISO 10605 for automotive electronics. It is the typical test method used to determine the immunity of systems to ESD events during operation [93]. It is commonly used to certify commercial electronic equipment such as mobile phones or computers and is a required test to attain a CE Mark. The IEC 61000-4-2 specifies the waveform parameters that should be delivered by the ESD tester as well as the procedures and stress points for executing ESD tests on system level. In principle, the system has to be stressed under powered conditions by an ESD discharge simulator (hand held ESD gun). Two different stress methodologies are possible, either directly contacting the stress point or performing an air discharge by approaching the stress point, whereby contact discharge is the preferred test method according to the standard [94]. Besides the ESD event itself, air discharge testing generates EMI, which is either shielded by the system or may induce voltage across TLs of the PCB. The IEC

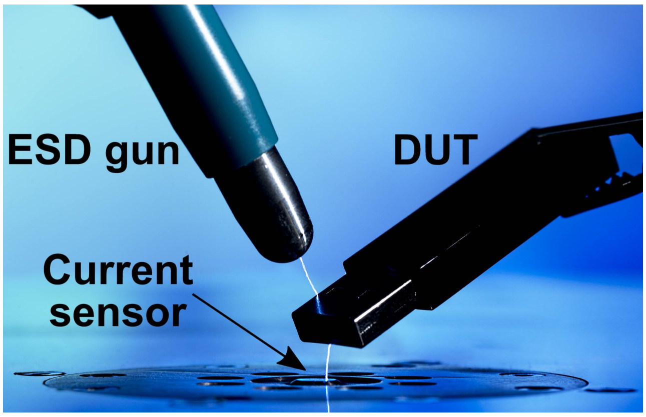

Figure A.2 System level ESD testing including primary and secondary air discharge.

stress waveform is a double-peak discharge waveform [95], containing an initial fast rising peak produced by the discharge of the local capacitance at the tip of the ESD gun and a lower second peak during the discharge of the remaining RC network of the gun. Since user applications can be subjected to many ESD strikes during their lifetime, a minimum of 10 positive and 10 negative strikes is recommended. Along with the failure mode of a physical destructive hard failure, a powered system can also suffer functional soft (reversible) failures, which can for example be restored by performing a reset.

In addition to the controlled primary stress pulse from the hand held ESD gun that charges up the investigated product, a secondary discharge event (Fig. A.2) from a non-grounded metallic part of the product to ground may occur [96]. The secondary ESD discharge was identified to be particularly harmful for the system under test and may lead to soft and hard failures [97]. It is important to emphasize here, that system level testing according to IEC 61000-4-2 does not correlate with device level testing (HBM and CDM) [93].

The Human Metal Model (HMM)

In order to emulate the system level ESD stress at component level, the standard practice Human Metal Model (HMM)[86] was developed and published in 2010. It defines device testing of external pins of individual ICs that are exposed to the outside world. Its intention is the evaluation of ICs with regard to an ESD stress pulse which it would be exposed to on system level. The waveform of the HMM pulse is the same as specified in the IEC 61000-4-2 document. Similar to HBM, HMM is a 2 pin test method but emulates much larger currents and faster rise times because it assumes a discharge which originates from a small piece of metal rather than from the human skin. In addition to the ESD stress, the DUT is exposed to the electric and magnetic fields radiated from the gun tip, which are caused by the rapidly changing currents at the stress point. In order to reduce the influence of the Electromagnetic (EM) radiation on the DUT, it is also possible to stress the DUT from behind through a hole in the test plane, serving as a shield, or to replace the usage of the poorly reproducible gun by the connection to a 50 Ω transmission line pulser [93]. This increases the reliability and reproducibility of the setup. For thermal related failures, a correlation between the power driven failure levels obtained by HMM and TLP have been reported in the literature [98–100]. However, an interlaboratory round robin test including 8 different operators located at different locations revealed that the current HMM method is not capable of determining a failure level with the IEC 61000-4-2 [95]. Results showed that while being relatively repeatable within a single lab, HMM measurements lack reproducibility across different labs.

Transient Latch-up (TLU)

Another stress mechanism which addresses stresses that occur beyond handling in the factory is Transient Latch-up (TLU). In this phenomenon, a fast transient turns-on a parasitic npnp-structures, e.g. a parasitic SCR of a CMOS IC, leading to a low-impedance path from VDD to VSS, producing either malfunction like an increased power consumption and/or irreversible damage. A TLU event can only occur if the device is powered on. Transient stress has been shown to be a more effective stimuli for latch-up events than static stress [101]. Besides ESD, TLU can be triggered by several real-world events reaching from a rapid rise or transient spikes of the power supply voltage through overshoots/undershoots during turn-on or turn-off to high-power microwave interference and ionizing radiation [102]. The latter case is particularly relevant for aerospace applications.

Cable Discharge Event (CDE)

Cable Discharge Event (CDE) arises when charged cables or peripheral devices are plugged in or out of a device port or when an uncharged cable is connected to the port of a charged device [103]. The CDE plays an important role in today's environment of mobile devices like cell phones or laptops, particularly in cases of "hot swapping" or "hot plugging", i.e. connecting or disconnecting cables into a connector with the system powered on. Recent studies deal for example with CDE on Ethernet or USB interfaces [103–105]. The cable can be charged triboelectrically or by induction [106, p. 383] and can build up hundreds of volts during flexing [93]. When approaching a system-level input, an air discharge takes place. A cable is able to store electrical charges proportional to its length and discharges similar to a TL with an initial high current spike [105]. Experiments indicated that, depending on humidity and isolation, a long charged cable needs more than 30 minutes until most of its charge is decayed through the air [107]. During this time, the potential risk of a CDE is present. The severity of the induced CDE strongly depends on the length and impedance of the cable and on the construction of the interface, e.g. which pin contacts first [103]. CDE typically lead to energy related damages or malfunctions resulting from (transient) Latch-up (LU) [105],[106, p. 383].

Charged Board Model (CBM)

Beyond CDM discharges in the manufacturing environment, the Charged Board Model (CBM) depicts an ESD hazard at the board-level. Being assembled onto a PCB which charges up, the device can be stressed by the discharge of the entire populated PCB upon contact with a conductive object. The significantly greater capacitance of the PCB leads to higher discharge current amplitudes through the device. This typically results in more severe ESD damages compared to HBM or CDM and can be easily mistaken for EOS damage [108]. In comparison to the single-pin discharge of CDM, various discharge paths inside the IC can be present at the same time. This makes the event much more complex and a high HBM and CDM robustness at component level can generally not be translated into a low susceptibility to CBM at the board-level [109]. In the CBM test procedure, an arbitrary stress point on the initially charged PCB is grounded. This offers additional testing opportunities and provides more discharge information for instance with respect to CDM, where only the package signal pins can be contacted or with respect to HMM, where only external ports can be addressed [24, p. 47]. Both, CBM and CDE are not standardized because of the broad variety of cables and boards.

List of publications

First-author publications

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