COPPER PILLAR BUMPS
as
SPACE-SAVING INTERCONNECTION TECHNOLOGY
on
THIN FILM ACOUSTIC PACKAGES
for
SURFACE ACOUSTIC WAVE RF-FILTERS

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ABSTRACT

Wireless data transmission is already a part in almost every area of daily life. Portable user devices like laptops, smartphones, smartwatches, headphones and many other devices use cellular networks, Wi-Fi, Bluetooth, and other standards to wirelessly transmit and receive data. Micro-acoustic radio frequency filters (RF-filters) are the key components to empower the frequency-related wireless communication as they provide good filter performance at reasonable component size. Just as in the entire semiconductor industry, there is also a demand for the further miniaturization of surface acoustic wave (SAW) and bulk acoustic wave (BAW) RF-filters. The miniaturization of components, which are manufactured at wafer-level reduces the costs and increases the functional density. The RF-filter size, the electrical performance, and the costs are key to commercially succeed on the market.

A package protects the sensitive micro-acoustic structures on RF-filters against environmental impacts. One of the thinnest commercially available SAW and BAW RF-filter components use the wafer-level manufactured Qualcomm TFAP™ * (Thin Film Acoustic Package). Solder bumps (SBs) on the TFAP ensure the mechanical and electrical joint to the printed circuit board (PCB) after component assembly and solder reflow. The SBs with a diameter of 140 µm consume a lot of valuable space on the small components. A simple reduction of the SB size is limited because the remaining gap (stand-off) between the soldered RF-filter component and the PCB would get too small to apply an underfiller in the gap during the final encapsulation process. The encapsulation additionally protects the components.

In this thesis the actual SBs on RF-filter components with TFAPs were successfully replaced by the space saving copper pillar bump (CPB) interconnection technology. CPBs are built of a cylindrical copper base with a spherical solder cap on top. In contrast to SBs, the height of CPBs and therefore also the remaining stand-off, can be broadly adjusted independently from the CPB diameter. The CPBs on TFAPs have a height of 75 µm and a diameter of 65 µm. Depending on the RF-filter component size

* Qualcomm TFAP is a product of Qualcomm Technologies, Inc. and/or its subsidiaries.

and the number of CPBs up to 26 % of additional free space is gained using CPBs instead of SBs on one component under current design rules. This allows a component miniaturization, the increase of functional density, novel design approaches (e.g. heat sinks, reduction of redistribution layers, combination of various CPB sizes and shapes), and a significant reduction in costs. The CPBs were manufactured with commercial tools by thin-film metal deposition, lithography, wet and dry etching, electroplating, and wafer singularization.

For component reliability testing a solder paste was stencil printed on the test PCBs prior the RF-filter assembly and soldering process. The reliability requirements of damp heat steady state (DHSS), dry heat (DH), unbiased highly accelerated stress test (uHAST), and temperature cycling (TC) on the CPB interconnection were fulfilled. In addition, component shear tests confirmed a sufficient mechanical connection to the PCB by CPB interconnections. A detailed understanding of failure modes after prolonged reliability test durations and the formation of intermetallic compounds in the solder was gained by failure and component analyses.

This work proves, that the replacement of SBs by CPBs on micro-acoustic RF-filters with a TFAP allows a significant component miniaturization and a reduction in costs still fulfilling the performance and reliability requirements.

KURZFASSUNG

Mobile Datenübertragung ist ein fester Bestandteil von fast jedem Bereich des täglichen Lebens. Mobile Endverbrauchergeräte wie Laptops, smarte Mobiltelefone, smarte Armbanduhren, kabellose Kopfhörer und viele andere miteinander drahtlos vernetzte Geräte (IoT, Internet of Things) nutzen Mobilfunk, Wi-Fi, Bluetooth und andere Standards für das kabellose Empfangen und Senden von Daten. Mikroakustische Hochfrequenzfilter (HF-Filter) sind die elektrischen Schlüsselkomponenten für eine kabellose Datenkommunikation. Sie bieten eine gute elektrische Filterleistung bei kleiner Bauteilgröße. Wie in der gesamten Halbleiterindustrie, gibt es auch bei Oberflächenwellenfiltern (SAW-Filter, surface acoustic wave filters) und Volumenwellenfiltern (BAW-Filtern, bulk acoustic wave filters) die Notwendigkeit einer fortschreitenden Bauteilverkleinerung. Die Verkleinerung von auf Wafer-Ebene gefertigten Bauteilen senkt Kosten und erhöht die Integrationsdichte. Bauteilgröße, Filterleistung und Bauteilpreis sind auf dem kommerziellen Markt für einen Erfolg entscheidend.

Ein Gehäuse („Package“) schützt die empfindlichen mikroakustischen Strukturen von HF-Filtern vor äußeren Einflüssen. Die dünnsten kommerziell erhältlichen SAW und BAW HF-Filter haben das auf Wafer-Ebene gefertigte Qualcomm TFAP™† (Thin Film Acoustic Package). Derzeit gewährleisten Lotkugeln (solder bumps, SBs) auf den TFAPs eine elektrische und mechanische Verbindung der HF-Filterbauteile zur Leiterplatte nach dem Bestück- und Verlötprozess. Die 140 µm großen Lotkugeln beanspruchen viel wertvollen Platz auf den HF-Filterbauteilen. Ein weiteres Verkleinern der Lotkugeln ist limitiert, da zwischen dem verlöteten Bauteil und der Leiterplatte eine definierte Spalthöhe (stand-off) gewährleistet sein muss, um auch den Spalt mit einer Moldmasse füllen zu können. Die Moldmasse schützt die final eingekapselten Bauteile zusätzlich.

In dieser Dissertation wurde die bestehende Lotkugel-Verbindungstechnik für mikroakustische SAW HF-Filter mit TFAPs durch eine platzsparende copper pillar

† Qualcomm TFAP is a product of Qualcomm Technologies, Inc. and/or its subsidiaries.

bump Verbindungstechnik (CPB-Verbindungstechnik) ersetzt. Die CPBs bestehen aus einer zylinderförmigen Kupfersäule auf der sich eine halbrunde Lotkappe befindet. Im Gegensatz zu Lotkugeln, kann die Höhe der CPBs und damit auch der Spalt zwischen dem Bauteil und der Leiterplatte über einen sehr weiten Bereich unabhängig vom Durchmesser der CPBs eingestellt werden. Die CPBs haben eine Höhe von 75 µm und einen Durchmesser von 65 µm. Abhängig von der Komponentengröße und der Anzahl der benötigen Verbindungen, können unter der Berücksichtigung von geltenden Entwurfsregeln der HF-Filter durch den Einsatz von CPBs statt SBs bis zu 26 % zusätzliche funktionale Fläche auf den Bauteilen gewonnen werden. Das ermöglicht eine Bauteilverkleinerung, eine Erhöhung der Funktionsdichte, neuartige Gestaltungsansätze (z.B. zusätzliche Wärmeableitung, Vermeiden von elektrischen Umverteilungen, Kombination von verschiedenen Formen und Größen der CPBs) und eine signifikante Kosteneinsparung je Bauteil. Die CPBs wurden an kommerziellen Anlagen mittels Dünnschicht-Metallabscheidung, Lithographie, Nass- und Trockenätzen, Galvanik und Wafervereinzelung gefertigt.

Die HF-Filterbauteile mit CPBs wurden auf mit Lotpaste bedruckte Testleiterplatten bestückt und verlötet, um anschließend die Bauteilzuverlässigkeit zu prüfen. Die Zuverlässigkeitsanforderungen von damp heat steady state (DHSS), dry heat (DH), unbiased highly accelerated stress test (uHAST) und temperature cycling (TC) an die CPB-Verbindungstechnik wurden erfüllt. Zusätzlich bestätigten Scherversuche an aufgelöteten HF-Filterbauteilen mit CPBs eine gute mechanische Verbindung zur Leiterplatte. Ein detailliertes Verständnis der auftretenden Fehlermodi nach verlängerten Zuverlässigkeitstests und die Charakterisierung der gebildeten intermetallischen Phasen im Lot wurden durch Bauteil- und Fehleranalysen gewonnen.

Diese Dissertation zeigt, dass durch den Austausch von Lotkugeln durch CPBs eine signifikante Bauteilverkleinerung und eine deutliche Kostenreduktion für mikroakustische HF-Filter erreicht wird, wobei die Anforderungen an Filterleistung und Bauteilzuverlässigkeit weiterhin eingehalten werden.

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1 Introduction & Fundamentals

In the last two decades wireless data transfer using mobile devices has changed our world in a radical way. Nowadays, mobile communication is available to almost everyone and it is present everywhere in our daily life. Mobile devices allow us to organize our day, gather information, get entertained, and to communicate to others independent of the current location. This has a massive impact on the evolution of our current society in all parts of the world. [1–5] Consumer devices like smartphones, computers, cars, household appliances, and many more are connected to each other utilizing mobile data transfer and hence connecting devices and people together. The mobile data transfer volume has increased steadily since years. The transferred data volume between Q4 2019 and Q4 2023 increased by factor 3.8 with a global number of unique mobile subscribers of almost 8.5 billion in Q4 2023 [6]. Most people are not aware that the invention of micro-acoustic radio frequency (RF) filters facilitated this progress. In general, mobile data transfer is based on transmission and reception of modulated electromagnetic waves in defined frequency bands. The main components to filter specific frequency ranges in mobile devices are micro-acoustic RF-filters, which are split into two types, namely surface acoustic wave (SAW) and bulk acoustic wave (BAW) RF-filters. These components meet the tough requirements on electrical performance, low energy consumption, and small component size, which are crucial for mobile devices. So far, more than 40 micro-acoustic RF-filters are integrated in an average smartphone to ensure functionality in various frequency bands. However, there is no globally harmonized standard for the usage of specific frequency bands for

certain purposes. To ensure global device functionality, high data transfer rates, and long transfer distances each mobile device must support many different frequency bands, hence multiple filter functions are required. The typical area demand of such a RF-filter inside a mobile device is in the range of 0.5 mm^2 to 2 mm^2 with a component height of typically 0.2 mm to 0.5 mm including the electrical interconnections. The high demand for mobile devices as e.g. smartphones is additionally amplified by the short replacement cycles of roughly only 2 years [7]. Furthermore, the increasing complexity of existing mobile devices and the addition of new products mainly driven by IoT (Internet of Things) [8], which all use mobile data transfer, do additionally reinforce the requirement for a huge number of affordable high-performance RF-filters with a small component size.

In this work the high potential of RF-filter component miniaturization by the replacement of the common solder bump for electrical interconnection by CPB (copper pillar bumps) interconnection technology is presented.

1.1 Surface Acoustic Wave Radio Frequency Filters

SAW and BAW RF-filters are the main electrical components to facilitate mobile data communication by using modulated electromagnetic waves in defined frequency bands, as they provide good performance at reasonable small component size. In this work the focus was set on SAW RF-filters. However, interconnect technology developed in this work can be used for SAW and BAW based RF-filters. The package protects the micro-acoustic filter structures against environmental impacts and will be described in following chapters. In the last decades there has been intensive research on SAW RF-filters to achieve ever-improving performance, miniaturization, and cost reduction. The research included the understanding of wave formation and propagation, various materials, filter structures, package designs, and micro-acoustic simulations to name a few. However, the field of SAW (and BAW) RF-filters easily fills complete books, wherefore this chapter will only give a very brief and simplified

introduction to the functionality of SAW RF-filters. Further very well summarized and detailed information of SAWs can be found in [9–12].

SAW RF-filters are based on the piezoelectric effect, by transforming electrical signals into mechanical waves and back to an electrical signal. A piezoelectric material changes its shape, if an electric field is applied and vice versa, i.e. the relative position of the atoms chances. To apply an electrical field to a piezoelectric material, inter digital transducers (IDT) can be used. Simple IDTs consist of two electrically separated bus bars on the piezoelectric material with thin comb shaped metal electrodes which are alternatingly interlocked to each other. The IDT's electrodes are in a regular distance to each other. Thus, applying a voltage to the bus bars induces an electrical field between one opposed electrode pair and causes a shape change in the piezoelectric material. The IDTs usually consist of multiple electrode pairs; hence, the application of a voltage difference to the two bus bars creates a repetitive electrical field between the electrodes, which causes a corresponding wave shaped deformation of the piezoelectrical material. In Fig. 1 the simplified schematic of a SAW delay line is shown. The delay line consists of an input-IDT and an output-IDT on a piezoelectric substrate and enables a simple illustration of the SAW filter concept. An oscillating signal is fed to the input-IDT, which converts some of the electrical energy into SAWs with the approx. wavelength corresponding to the electrode distances from the same bus bar. The distance between two neighboring electrodes, which belong to the respective other bus bar, define approx. half the wavelength formed. The IDT is bidirectional, which means that the wave shaped deformation in the piezoelectric material induced by the repetitive electric field of the input-IDT will leave equally on both sides of the IDT as long as the input signal oscillates.

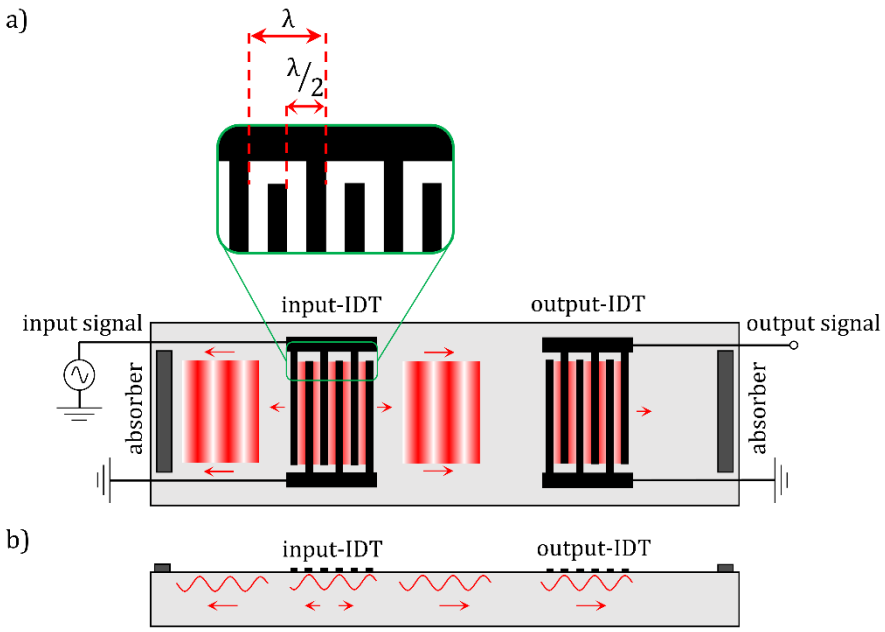


Fig. 1. Schematic of simplified SAW delay line. In a) the top view of piezoelectric substrate with the input inter digital transducer (IDT) for acoustic wave formation from an electrical signal and the output-IDT for transformation from an acoustic wave back into an electrical signal. The input-IDT is bidirectional, i.e. the formed wave travels in both directions. The absorber does absorb acoustic waves to minimize reflections and thereby caused unwanted superpositions and delayed signals. The distance between two opposed connected electrodes equals approx. half of the wavelength formed. The distance between two nearest electrodes of the same bus bar equals approx. the wavelength formed. In b) the schematic cross-section of a). The surface acoustic waves are illustrated only highly simplified.

If the voltage applied oscillates in a frequency enabling constructive superposition of the formed SAWs, continuous moving wave fronts with high amplitudes, which are parallel to the IDT's electrodes will exit on both ends of the input-IDT. To enable constructive superposition of the formed SAWs for a center frequency f_0 of interest the propagation velocity v of the SAWs inside the piezoelectric material needs to be considered to define the wavelength λ and thus the IDT's electrode distances by

$$\lambda = \frac{v}{f_0} \,. \tag{1.1}$$

In this work only the piezoelectric material lithium niobate (LN, $LiNbO_3$) in the 128° Y-X cut was used and for this material typically Rayleigh waves [13] are formed by the IDTs. A schematic Rayleigh wave in half-space is shown in Fig. 2. The propagating wave consists of a transversal and longitudinal part, which induces a

counterclockwise elliptical material movement in the material. The amplitude decreases with the depth of the material with the highest amplitude at the free surface.

In Fig. 1 the output-IDT is just on one side, hence only in one direction the propagating SAW will reach the output-IDT and will be transformed back into an electrical signal. The SAWs propagating in the other direction are absorbed in the absorber. The absorption minimizes unwanted wave reflections and wave coupling effects. In very simplified terms, all input frequencies except the ones close to the center frequency f_0 will experience a high attenuation because no constructive superposition takes place during wave formation. This results in a lower amplitude due to partly signal cancellation by destructive wave interference. Additionally, the transformation of the SAWs back into an electrical signal at the output-IDT will also result in a weaker signal.

The propagation velocity of SAWs in $LiNbO_3$ with a free surface, i.e. free of deposits like a metallization on the surface depends on the crystal orientation, the wave type, and the propagation direction of the waves [15, 16]. The crystal orientation of the $LiNbO_3$ substrate is defined by the cut, i.e. how the thin wafer is separated from the single crystal ingot. In this work $LiNbO_3$ with a 128° Y-X cut was used for all SAW RF-filter components, resulting in a wave propagation velocity v of approx. 3977 m/s

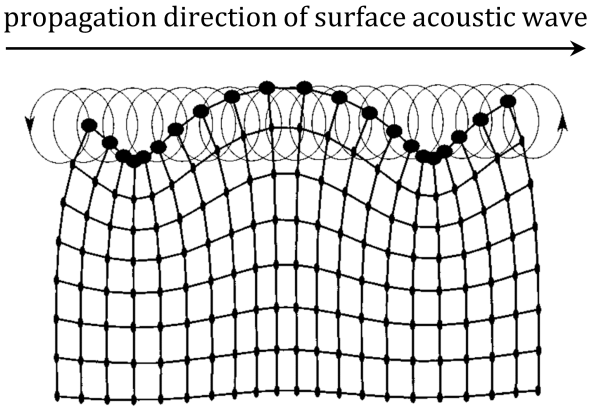


Fig. 2. Schematic half-space of particle motion in a Rayleigh wave. Elliptical motion of particles by a vertical and horizontal movement. Graphic adapted from [14].

for Rayleigh waves with a free surface and an electromechanical coupling coefficient K^2 of 0.057 (5.7%) [17]. The electromechanical coupling coefficient K^2 describes how much electrical energy is transformed into an acoustic wave. Because the electromechanical coupling coefficient for metallized surfaces (considering ideal thin metallization with no weight) and free surfaces are almost equal for Rayleigh waves, according to [9, 15, 18], K^2 can be calculated by

$$K^2 = \frac{v_{free}^2 - v_{metallized}^2}{v_{free}^2} \cong 2\,\frac{v_{free} - v_{metallized}}{v_{free}} \equiv 2\,\Delta v/v\,. \qquad (1.2)$$

The schematic crystal structure and an illustration of the $LiNbO_3$ cut used is shown in Fig. 3. The first letter (Y) in the notation of 128° Y-X-cut indicates that the wafer's surface is the normal of the y-axis in the cartesian coordinate system and the second letter (X) defines the acoustic wave propagation direction along the x-axis. The angle

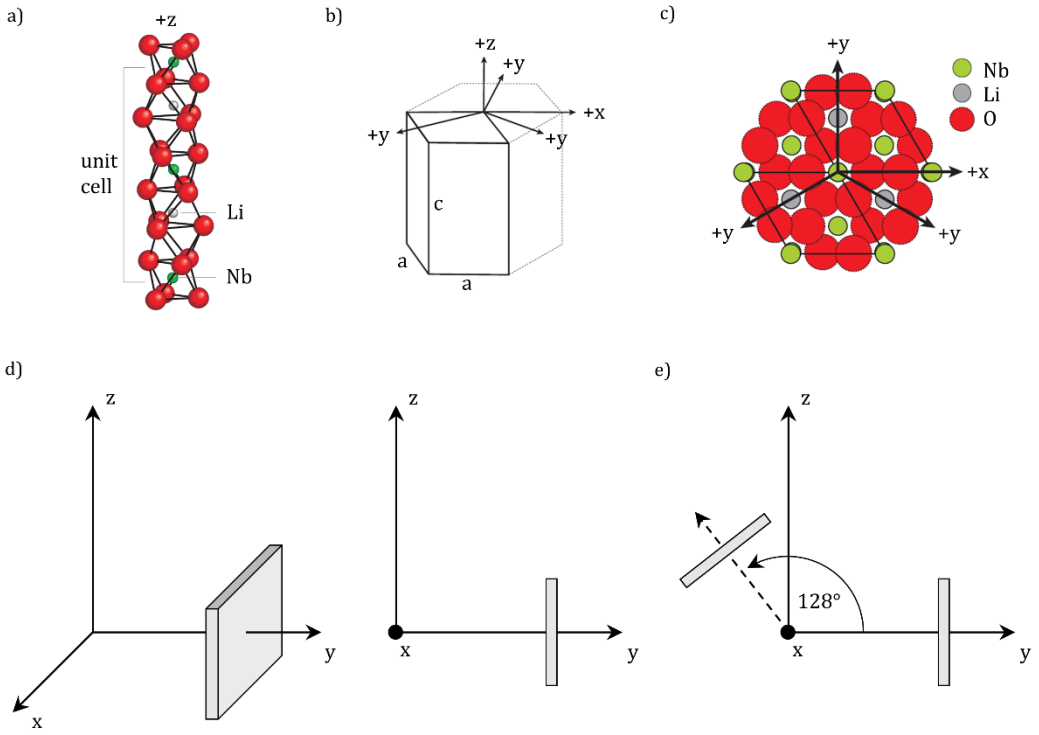


Fig. 3. Schematic crystal structure of $LiNbO_3$. In a) the unit cell of $LiNbO_3$. In b) the vectors of a hexagonal (c, a) and orthogonal (x, y, z) unit cell, where the unit cell lattice parameter c equals the z-axis and three y-axis are perpendicular to the z-axis. The y-axis are in the mirror planes of the unit cell and the corresponding x-axis are the cross-product of x=y × z. In c) top view of the unit cell along z-axis. In d) Y-X cut in cartesian coordinate system and in e) a 128° Y-X cut rotated over the x-axis. [20] Graphs adapted from [20, 21].

of 128° indicates the rotation of the surface plane over the x-axis. Further details about the $LiNbO_3$ material properties and manufacturing can be found in [19].

128° Y-X cut creates only little unwanted bulk waves in comparison to a Y-Z cut, which results in lower losses, but it shows a higher diffraction of the wave the farther away from the transducer, i.e. the wave become rather circular instead of parallel to the electrodes. The diffraction can be diminished by the filter's design. [16] As so often the case, the SAW RF-filter components used in mobile applications are much more complex in their design and function than a simplified introduction can explain, by even following physical descriptions that can be solved only numerically at the current time.

The SAW RF-filter duplexer used in this work have a high signal attenuation in the stop band region, i.e. in frequency regions which are not intended for data communication, and a very low attenuation in the pass band region, i.e. the frequency regions which are intended for data transfer. A duplexer uses the same path for transmitting and receiving via the antenna and it uses two very close but still separated frequency bands. In this work the SAW RF-filter duplexer can transmit and receive at the same time, which is also called full duplexing using frequency division duplexing (FDD). The delay line design used for the introduction to SAW RF-filters has high insertion losses due to the acoustic wave absorption at one side of the input-IDT. Further unwanted ripples in the pass band due to acoustic wave reflections at the electrodes limit their range of applications especially for mobile RF-devices.

However, low-loss bandpass filters can be realized by a combination of electrically connected SAW resonator structures. A simple SAW resonator structure can be achieved by one IDT sandwiched between two reflector structures, which reflect the SAWs. A simple schematic of such a SAW resonator is shown in Fig. 4 a). The SAW is trapped between both reflectors creating a resonant cavity. Gratings can be used as reflectors made of e.g. the same metal as the IDT's electrodes. The free surface between each grating and the grating's metal stripe width are both a quarter of the wavelength, which achieves a high reflectance, due to constructive superposition

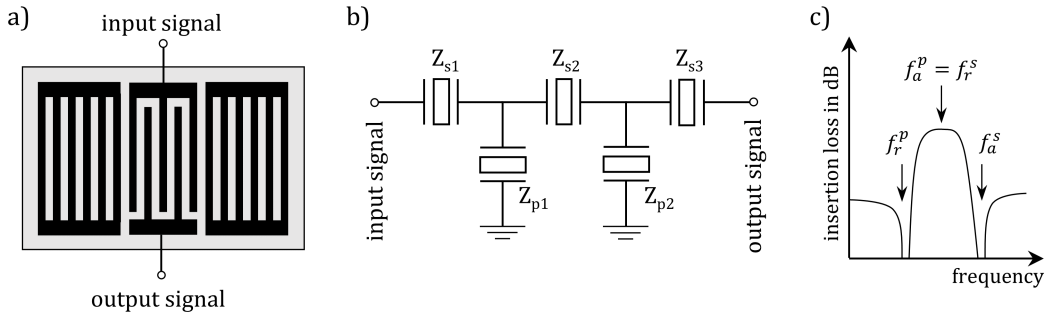


Fig. 4. SAW resonator. In a) the schematic top view of a SAW resonator with one IDT sandwiched between to reflector gratings. In b) an impedance element filter (IEF), which consist of a ladder type combination of SAW resonators. Z indicates the corresponding impedance of parallel and serial SAW resonators. In c) the schematic response of an IEF indicating the resonance and antiresonance frequencies of the serial and parallel SAW resonators. Graphs adapted from [9, 11].

(Bragg frequency) of the reflected SAWs. The distance between the gratings and the respective position of the IDT must also be chosen to fulfill constructive interference. The reflection's nature mainly relies on two effects. First, a mechanical effect, which is due to the discontinuity of the surface. Second, an electrical effect, because the metal grating is short-circuiting the piezoelectric surface, which disturbs the SAW propagation and leads to a reflection. Further, an electric field is induced from the propagating SAW to the metal reflectors passing the grating. This induced electric field is subsequently released which therefore also forms SAWs in both direction and hence creates a reflection. As the reflectance of one metal stripe is quite low gratings with numerous metal stripes are usually used. The thin metal stripes minimize the formation of bulk waves and reduce therefore signal losses. Different reflector types, structures, and various electrical connections to each other allow different reflection characteristics. These SAW resonators have a resonance frequency where the admittance is very high, i.e. the signal is passed through the filter with very low attenuation. However at the antiresonance frequency almost no acoustic coupling takes place and the SAW resonator has a very high impedance (low admittance), hence the signal is strongly attenuated at the output of the filter. [9, 11, 12]

For mobile RF applications low-loss pass band filters are required with a high-power compatibility and a relatively small size. These requirements are met by

an impedance element filter (IEF), which combines electrically connected SAW resonators as shown in Fig. 4 a) mostly on the same substrate in a ladder type by alternating between serial and parallel as illustrated in Fig. 4 b). The serial SAW resonators are designed that the frequency of interest fulfills the Bragg conditions, i.e. at this frequency the serial resonators have their resonance frequency f_r^s. Thus, for f_r^s the impedance is low and the admittance is high. Therefore, the input signal can pass through the serial SAW resonators with low attenuation. The parallel SAW resonators are designed to have their antiresonance frequency f_a^p equal to the resonance frequency f_r^s of the serial SAW resonators, thus no signal is lost to the ground because the impedance of the parallel SAW resonators is high. The impedance of the parallel SAW resonators gets very low for their resonance frequency f_r^p and thus the input signal goes to the ground, as the serial SAW resonators have a high impedance. For the antiresonance frequency f_a^s of the serial SAW resonators the impedance gets very high and hence no signal can pass through them. Outside the passband, which is between the resonance frequency f_r^p of the parallel SAW resonators and the antiresonance frequency f_a^s of the serial SAW resonators, there is only little acoustic coupling. Thus only little signal can pass due to the resonators' static capacitances. [9, 11] The choice of material, cut angle, the electrode design, and SAW filter approach including the formation of a specific wave types have a direct impact on the SAW RF-filter characteristics in terms of insertion loss, temperature stability, passband and stopband characteristics, and high-power compatibility. This has led to different approaches like the described IEF but also transversely coupled resonators (TCR), and longitudinal coupled resonators (LCR). However, these types are not explained here but further information can be found in [9, 11].

The required metal stripes for electrodes and grating to form a RF-filter are manufactured at wafer-level by photolithography and thin film metal deposition. The SAW resonators are sensible to environmental impacts if mass loading and corrosion effects are induced. Therefore, a special package needs to protect the filter structures, but must not interfere with the filter function. The provision of an air cavity above the filter structure by the micro-acoustic package is mandatory to ensure that the SAW

formation and propagation is not disturbed by the package. Packaging of micro-acoustic filters will be discussed in the next chapter.

Finally, for RF signal filtering various RF-filter components are commonly integrated into so called RF-modules together on a shared substrate with other electrical components like electrical switches, amplifiers, inductors, capacitors, among others. This allows to match the impedance for all integrated components to achieve the best electrical filter performance. RF-modules are normally encapsulated by a mold-material to enhance reliability. Typically, manufacturers of consumer products purchase customized RF-modules, which already meet all their requirements.

1.2 Component Miniaturization as a Driver

The customers of RF-filters which are, for example, the manufacturers of smartphones have a demand for increasingly smaller electronic components. There are different reasons for it, one is that the space inside mobile devices is very limited. Many different components are combined in such a device. Additionally, this situation is aggravated by the increasing number of components needed to achieve the high device functionality, which is essential to be successful on the consumer market. Thus, there is a high interest in miniaturized components including the large number of integrated RF-filters. At the same time not only component size but also electrical performance, component reliability and the costs are major decision-making criteria for RF-filter component costumers. However, the manufacturers of RF-filter components have also a great interest in further miniaturization of single components. Obviously, this is because of their costumers' requirements but also because the miniaturization may offer some benefits for the manufacturers themselves. The main driving force might be the potential manufacturing cost reduction. Typically, RF-filters are manufactured at wafer level, thus minimizing the component size on a wafer will allow a higher total number of components on a single wafer. This can decrease the manufacturing costs

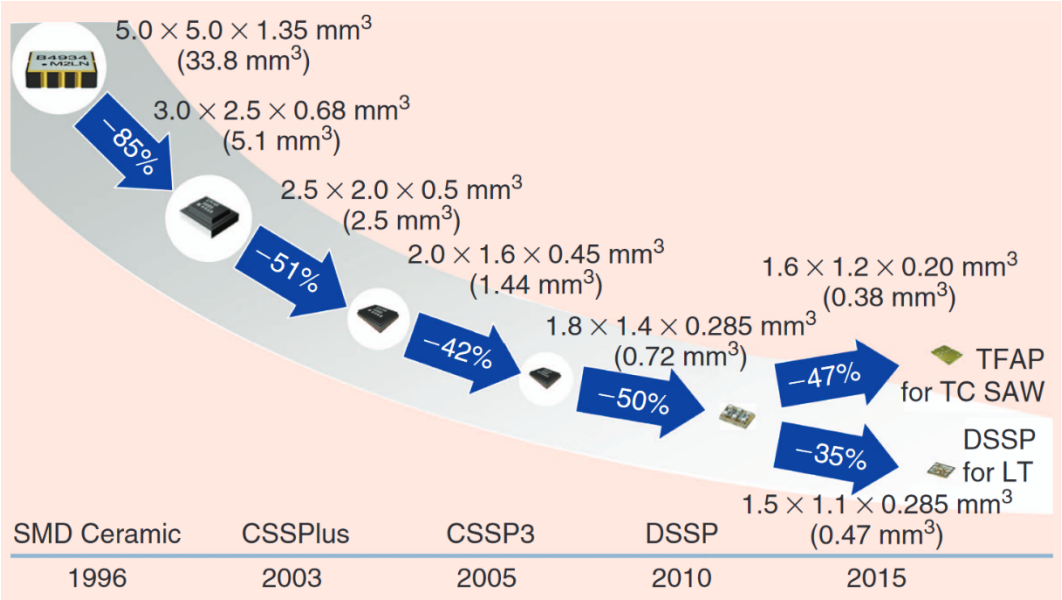


Fig. 5. Miniaturization of SAW RF-filter duplexers package technologies developed by RF360 Europe GmbH (former EPCOS). [22] © [2015] IEEE

per single component but only if the production costs generated by possible new processes which are necessary for miniaturization and a potential higher yield loss due to the new processes do not devour this advantage. The trend of miniaturization in the segment of RF-filters in the last two decades can be clearly seen in Fig. 5. Since the 90's package technologies for RF-filters changed which enabled a height reduction of approx. 85 % and a volume reduction of approx. 99 %. This significant component miniaturization facilitated today's consumer products in the first place.

This massive shrinkage was only achievable by developing new package technologies. Starting with the largest package technology as shown in Fig. 6 a) which is SMD (surface mounted device) Ceramic, where the SAW device is bonded into a ceramic box, electrically connected via wire bonding, and sealed with a lid. However, the bond wires limit the device's performance by their fluctuating impedances and additionally the wires consume valuable space. The technologies subsequently developed were three generations of CSSP (Chip Sized SAW Package), namely CSSP, CSSP 2 (CSSPlus), and CSSP 3. All three generations have the SAW chip soldered to a LTCC (low temperature cofired ceramic) or HTCC (high temperature cofired ceramic) as a substrate or interposer in common. To protect the sensible filter structures and

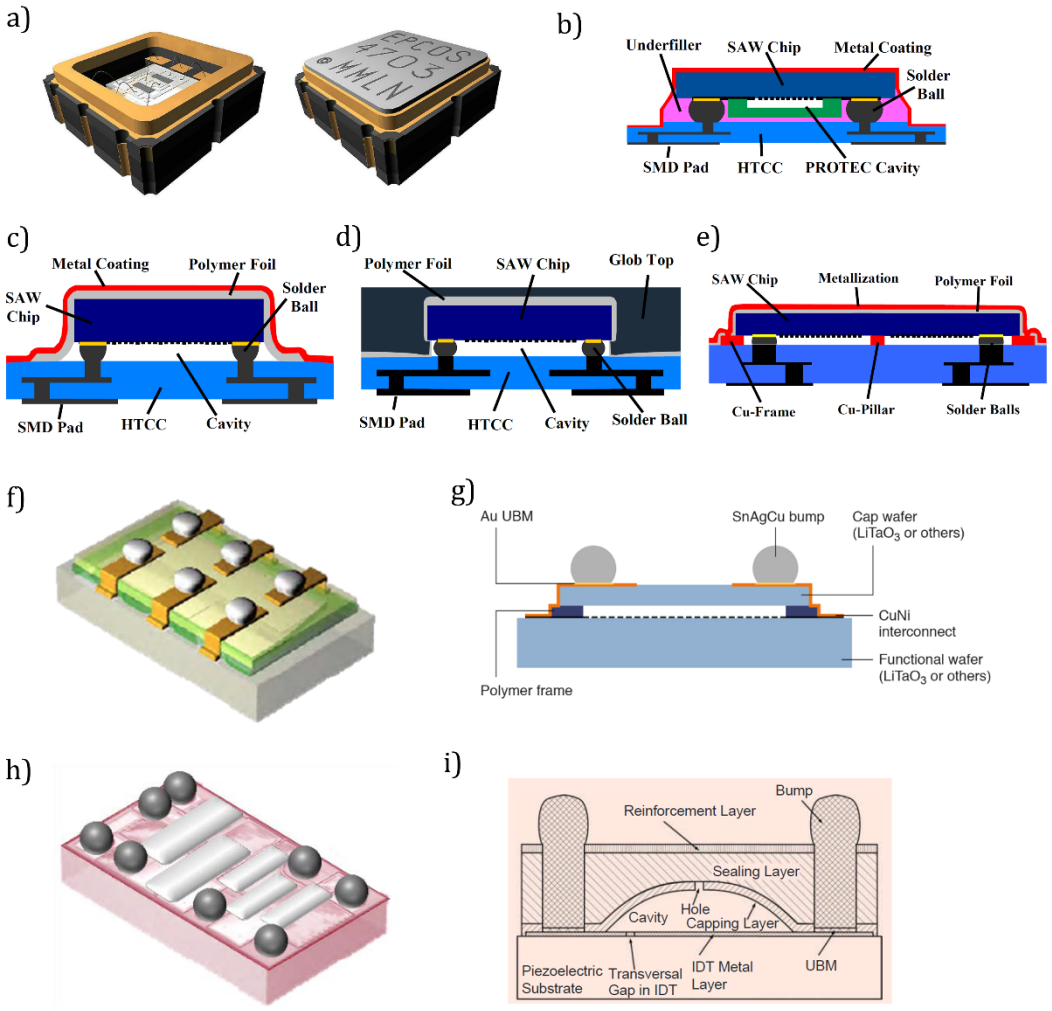


Fig. 6. Package evolution of RF360 Europe GmbH (former EPCOS) micro-acoustic RF-filters. In a) schematic of SMD Ceramic Package [24]. Schematic cross-sections of b) CSSP 1 [24], c) CSSP 2 (CSSPlus) [24], d) non-hermetic CSSP 3 [24], and e) hermetical CSSP 3 [24]. In f) a schematic of DSSP [23] with the schematic DSSP cross-section in g) [25]. In h) a schematic of TFAP for SAWs [23] with the schematic TFAP cross-section in i) [22].

to provide a cavity above these structures for CSSP 1 a small PROTEC cavity is created over the SAW structures. The SAW chip is then flip chip bonded on the ceramic substrate and an underfiller is applied. A deposited metal layer ensures sealing as shown in Fig. 6 b). For CSSP 2 and the non-hermetic CSSP 3, which are illustrated in Fig. 6 c) and Fig. 6 d), respectively, a polymer film is applied after flip chip placement on the ceramic substrate. Then a metal coating is applied for the CSSP 2 technology and a glop top foil for the non-hermetic CSSP 3 technology to seal the package. The

hermetic CSSP 3 uses a metal coating for the hermetic sealing instead of the glop top and is illustrated in Fig. 6 e). Further, the hermetic CSSP 3 technology withstands higher molding pressure due to a copper frame and mechanically supportive copper pillars in the center of the chip. The DSSP (Die Sized SAW Package) technology uses bonding of two wafers with a polymer frame as sealing to create a cavity. At least one wafer contains filter structures and another wafer is used as lid. DSSP is shown in Fig. 6 f) and Fig. 6 g). The latest technology is the so called TFAP and is illustrated in Fig. 6 h) and Fig. 6 i). Here the cavity is created by a stack of different materials using the sacrificial layer method creating a package with a height of only approx. 20 µm (substrate and electrical interconnections are not taken into account). [22–25]

1.3 Miniaturization of Thin Film Acoustic Packages

TFAPs can be used for SAW, BAW and TFSAW (Thin Film SAW) RF-filter technologies. Typically, BAW and TFSAW RF-filters are built on Si (silicon) substrates, which have an isotropic thermal expansion. On the other hand, SAW RF-filters are mostly built on LN or lithium tantalate (LT, $LiTaO_3$). These substrates have a rather strong anisotropic thermal expansion and show piezo- and pyroelectricity, which makes them prone to wafer fracture during manufacturing processes. Hence, process development for CPBs was focused on SAW RF-filters because processes developed for RF-filters with LN or LT substrates can be easily transferred to RF-filters with a Si substrate.

There are different miniaturization approaches for TFAPs. The one presented in this work is to minimize the space consumption of the electrical interconnections, which electrically and mechanically connect the chip to the PCB (printed circuit board). The standard TFAP technology uses spherical solder bumps (SB) as electrical interconnection. The SB interconnections, the package, and the filter structures are on the same chip side as shown in Fig. 6 h). Thus, SB interconnections consume valuable chip area. This consumed area cannot be used by packaging or filter structures. The shrinkage of the electrical interconnections allows to gain significant more active chip area which can be used for filter structures or chip miniaturization.

TFAP is one of the thinnest commercially available package solutions for RF-filters on the market and it has almost no impact on the filter characteristics [26]. Therefore, the further miniaturization of TFAP enhances its already high potential for RFFE (radio frequency front end) components. However, the simplest way of reducing the TFAP's spherical Sn-Ag-Cu alloy (SAC) SB interconnections is limited by the required stand-off between the soldered RF-filter and the PCB for the molded underfill after component assembly. This is because the further miniaturization of the spherical shaped SBs would result in a significant gap height reduction between chip and PCB, which is no longer sufficient to apply the molded underfill inside the gap, as shown in Fig. 7. The underfill is a composition of a particle filled epoxy resin to encapsulate the chip and to fill the gap between chip and PCB after assembly to the PCB. The underfill mechanically supports the chip and mechanical stress is not only induced into the electrical interconnections but distributed to the whole chip. The underfill's CTE (coefficient of thermal expansion) is adjusted to the PCB and the chip to minimize thermo-induced mechanical stress, which enhances the component reliability in the final RF-module.

In this work the miniaturization on TFAPs was performed by replacing the former SB by CPB interconnections [27]. In 2013 G. Fattinger et al. published a BAW RF-filter with CPBs for a wall-roof based package on a silicon substrate for the purpose of miniaturization [28]. In the case of TFAPs the replacement of SBs is also an effective strategy for minimizing the chip size of RF-filters by up to 26 % considering the standard design rules. A simple CPB consists of a cylindrical Cu base and a spherical solder cap on top. A Ni diffusion barrier is sandwiched between the Cu base and the solder cap. A schematic draw and a scanning electron microscopy (SEM) image of a CPB is shown in Fig. 7 d). The stand-off, i.e. the gap between chip and PCB after flip-chip assembly can easily be adjusted by the CPB's Cu base height, thus providing a sufficient gap height for the molded underfill. CPBs were already patented in 2001 by IBM [29]. Nowadays, CPBs are already implemented in several applications due to their benefits compared to other interconnection technologies and many outsourced semiconductor assembly and test manufacturing vendors like Amkor, APS, ASE, FCI, JCET, Nepes, PTI, SPIL, and UAT offer CPBs manufacturing solutions on Si based

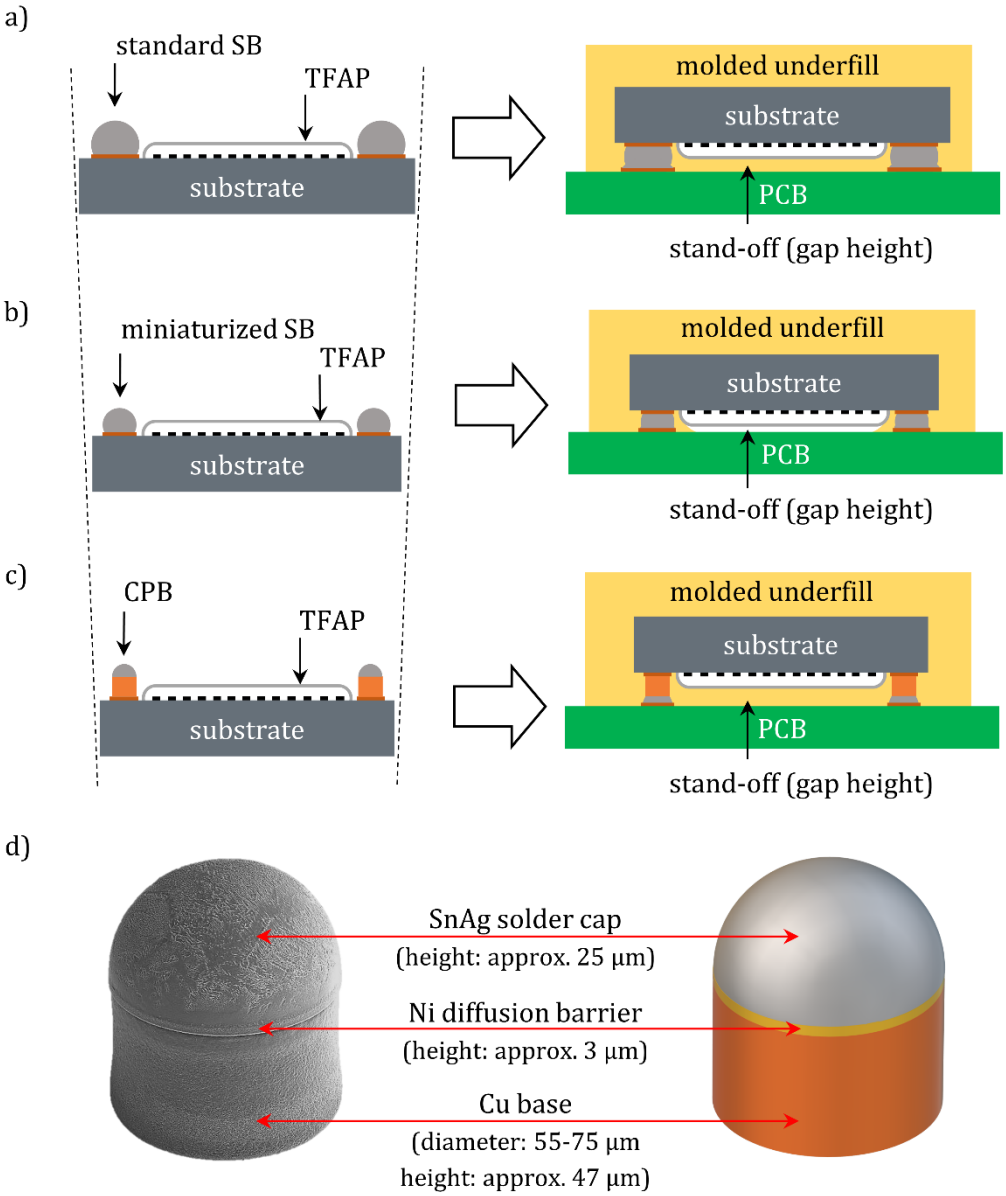


Fig. 7. Schematic cross sections of RF-filters with SBs and CPBs. a), b), and c) show schematic cross-sections of single RF-filters with a TFAP and the corresponding assembled RF-filter mounted on a PCB (green) and encapsulated by a molded underfill (yellow). a) illustrates the current TFAP technology available on the market with standard SB interconnections. The standard SB interconnection facilitates a sufficient gap height for the molded underfill after soldering to the PCB. b) shows a fictitious miniaturization of the SB interconnections resulting in an insufficient distribution of the molded underfill below the TFAP due to the too low gap height. c) illustrates the substitution of SBs by CPBs, which consume less chip space compared to SBs and easily facilitate a sufficient gap height by adjusting the copper base height. The dashed lines indicate the miniaturization potential. In d) the geometry and materials of a round CPB with a spherical solder cap are shown at a SEM image (left) and a 3d-schematic (right).

substrates without high topologies [30–39]. However, for RF360 Europe GmbH a Qualcomm company, micro-acoustic package technologies with CPBs as interconnection technology were not available on the market during this research. In this work manufacturing technics for CPBs on TFAPs were developed to produce very first RF-filter components, which were subsequently tested for their electrical performance and reliability.

The high miniaturization potential of TFAP components by replacing SBs with CPBs is shown in Fig. 8. The main reasons for the miniaturization are the smaller footprint of the CPB and the beneficial spacing rules, i.e. the space needed between the CPBs and the surrounding structures. The diameter of the conventional SB interconnection for TFAPs is in the range of 120-140 µm. The diameter of the CPBs is in the range of 55-75 µm or even less, thus significantly smaller. The manufacturing processes and the geometry of CPBs allow smaller pitches, i.e. the distance between

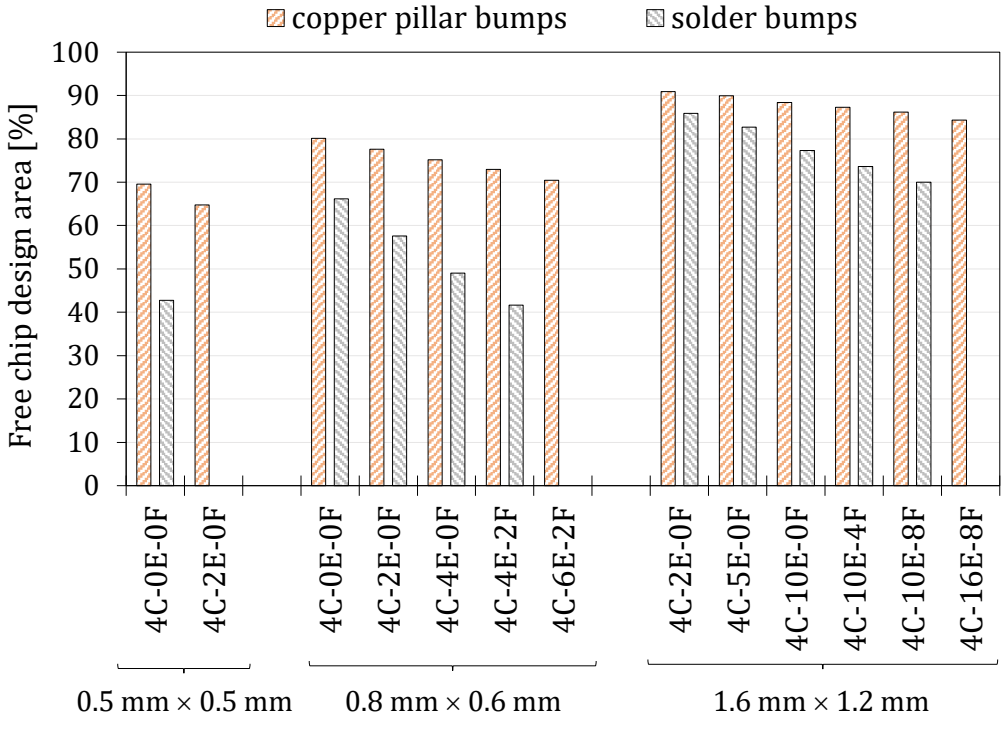


Fig. 8. Comparison of remaining free chip design area between SBs and CPBs on a TFAP following current design rules. The free chip design area can be used for package and filter structures. The values are calculated for three different chip sizes and different interconnection positions on each chip. The interconnection position is defined by C = corner position, E =edge position, and F = free/middle position on the chip. A missing column indicates a non-feasible combination due to space limitations on the chip.

two neighboring interconnections. In contrast, SBs tend to bridge between two interconnections at low pitches due to their spherical shape prior assembly and an even more with the squeezed shape after assembly to a PCB.

CPBs facilitate almost random interconnection positions on a component, which avoids unnecessary redistribution layers due to the smaller interconnection size and the smaller pitch. A further advantage is that the CPB's Cu base height is almost independent on a large scale from its diameter. With the design advantages of CPBs as interconnection technology, also the 3d package integration becomes more attractive. Additionally, there is a high potential for an increase of electrical performance, RF-filter functionality, and power durability through higher interconnection density and the selective placement of interconnection heat sinks with CPBs, which is not feasible with SB interconnections.

1.4 Main Achievements

The key achievements reached in the frame of this work are listed in the following. The manufacturing processes were developed and applied in a running manufacturing environment using common manufacturing tools. Therefore, overcoming organizational challenges by approving new materials and processes was also a part of this work. Unfortunately, due to confidentiality obligation some concepts developed and used in this work cannot be explained in every single detail. During development, the focus was always set on economic efficiency and feasibility for mass production of RF-filter components with a TFAP and CPBs as interconnections technology. The main achievements are:

- Creating a multi-design wafer layout including various designs and process control structures for TFAP SAW RF-filters by customizing the existing package technology in close cooperation with the RF360 Europe design team. This included the estimation of process biases and alignment concept adjustments for the fabrication of the new interconnection technology.

- Selection of process materials in compliance with local regulations including environmental compatibility, emission control and treatment (air and wastewater), occupational safety, material storage, equipment compatibility, processability, exclusion of contaminating effects to other processes, and material disposal in cooperation with RF360 Europe health, safety, and environmental department. This also required some modifications on the supply and disposal infrastructure to comply with the strict local regulations.
- Selection, modification, and development of manufacturing processes for CPBs on TFAPs in the fields of thin film metal deposition, electrochemical metal deposition, thick-film lithography, dry and wet etch processes, solder reflow, and lithium niobate wafer singularization. Further, the evaluation of the process suitability and possible interactions between them were considered.
- Coordination of taping selected designs into tape & reel in cooperation with RF360 technology (Wuxi, China).
- Design of test PCBs for daisy chain and functional components in cooperation with RF360 Europe reliability department.
- Implementation of small volume solder paste printing with stencil from Christian Koenen GmbH including the alignment concept and pick and place flip chip component assembly.
- Design of experiments and the evaluation of results for process and design optimizations.
- Reliability and mechanical testing using damp heat steady state, dry heat, unbiased highly accelerated stress test, temperature cycling, and mechanical shear testing with the corresponding statistical result evaluation.
- Failure analysis, process change impact analysis and material characterization by C-mode scanning acoustic microscope, scanning electron microscope, focused ion beam cutting, optical microscopy, mechanical cross-sectioning, shear testing, interferometry, and energy dispersive X-ray analysis.

- Approval of CPBs as new interconnection technology for RF-module integration with micro-acoustic SAW RF-filter demonstrator components by fulfilling the main reliability requirements.
- Publication of selected results at conference presentations and a peer reviewed journal after approval from project partners.

These achievements are explained and the results are discussed in the following chapters.

2 Copper Pillar Bump Manufacturing

The following subchapters start with a summarized overview of TFAP and CPB manufacturing processes for the RF-filter components. Multiple following subchapters are describing the developed manufacturing processes in more detail. Impacts of process parameter variations are also discussed in the following chapters.

2.1 Overview Qualcomm TFAP and CPB Manufacturing

The miniaturization of SAW RF-filters with a TFAP was achieved by replacing the standard SBs by CPBs interconnection technology. Therefore, CPB manufacturing processes were developed and specifically applied to TFAP. Generally, micro-acoustic RF-filter structures need an air cavity to allow undisturbed formation and propagation of acoustic waves in the piezoelectric material. In this work the cavity is provided by the Qualcomm TFAP. The successive SAW RF-filter manufacturing steps were all performed at wafer-level beginning with the micro-acoustic SAW RF-filter structures (RF front end) followed by the TFAP and the CPBs. At last, wafer singularization processes were applied.

TFAP is one of the thinnest commercially available wafer-level packages for RF-filter structures with only 15 µm to 25 µm package height (not taking into account the substrate and the electrical interconnections). TFAP consists of a material layer stack and protects the sensitive SAW or BAW structures from environmental impacts,

thus preventing corrosion and mass loading effects of the sensitive IDTs, which would negatively influence the electro-acoustic performance. The package provides a hermetically sealed air cavity above the filter structures to allow the unhindered formation and propagation of acoustic waves, which is crucial for high performance and low insertion loss micro-acoustic filters. The TFAP itself has no negative impact on the electrical performance of the RF-filters and is suitable for Si or $LiNbO_3$ substrates. During this study only TFAPs with solder bumps as electrical interconnection were available on the market. Fig. 9 schematically shows the SAW TFAP manufacturing steps with the new CPB interconnection technology. TFAP is built up as a multi-layer structure of different materials to create an air cavity above the filter structures. First, a structured and edge-rounded sacrificial layer is created on the IDTs as shown in Fig. 9 a) and Fig. 9 b). Onto the sacrificial layer the first dielectric layer is deposited, which is called capping layer. The capping layer is structured by standard lithographic and dry etch processes to create small openings in the capping layer above the sacrificial layer and large openings on the EP layer (electrical path) for later CPBs as illustrated in Fig. 9 c). In Fig. 9 d) the sacrificial layer is removed during the release process through the small openings in the capping layer without damaging the sensitive RF-filter structures. A sealed air cavity is then created by coating a photosensitive polymer onto the capping layer, which closes the small capping openings above the RF-filter structures. This polymer layer is called sealing layer and is shown in Fig. 9 e). The last manufacturing step for TFAPs is the deposition and structuring of the reinforcement layer. This layer is harder than the sealing layer and in combination with the edge-rounded shape, a good mechanical performance of the hermetically sealed air cavity is achieved. The reinforcement layer covers all previous TFAP layers but is opened above the EP layer to allow electrical connection to the CPB as illustrated in Fig. 9 f). Hence, the reinforcement layer opening of the TFAP defines the electrical contact area between the EP layer and the CPB. [22]

For the CPB implementation the TFAP process steps were not significantly changed. However, the usually fabricated under bump metallization and the solder bumping were omitted and replaced by CPBs. Further, design changes in e.g.

reinforcement layer opening sizes and the revision of design rules like the overlap between different layers according to process variations were implemented.

A simplified manufacturing summary in Fig. 10 schematically illustrates the CPB fabrication on TFAPs and the subsequent wafer singularization. The whole processing is performed on 150 mm LN wafers. Also, the CPB manufacturing is performed at wafer-level and starts with the deposition of a thin seed-layer of titan and copper. This

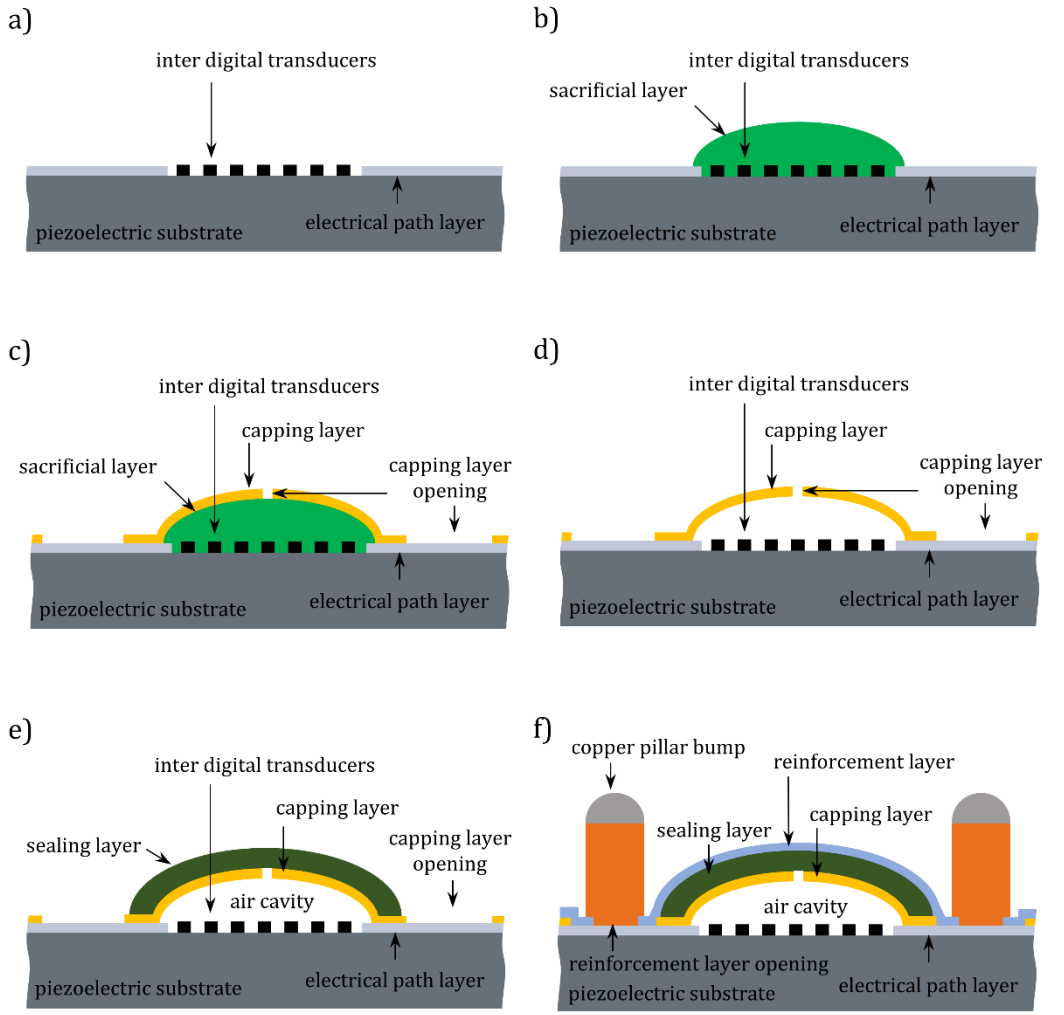


Fig. 9. Schematic cross-section of the TFAP manufacturing steps for SAW components. In a) the IDTs of SAW filter on a piezoelectric substrate material are shown. IDTs are electrically contacted by metallic electrical path layer. Coating and structuring of sacrificial layer on IDTs in b). In c) deposition and structuring of first dielectric layer (capping layer) including openings. d) shows the removal of the sacrificial layer through capping openings. The capping opening on top of the IDTs is closed by a polymer sealing layer creating a sealed air cavity as shown in e). In f) reinforcement layer is deposited as last layer followed by the CPB fabrication. Graph is adapted from [22].

seed-layer is deposited on the already manufactured TFAP as shown in Fig. 10 a) and b). Photolithography allows to structure small openings in a photoresist film which is on the whole wafer. These openings define the intended CPB position and shape. Therefore, a photoresist is applied by spin-coating (see Fig. 10 c)) and is then partly exposed to UV-light (ultraviolet light) through a photomask. This defines the exact position and shape of the photoresist openings after the liquid-based development as illustrated in Fig. 10 d). A soft plasma cleaning step removes potential resist residues from the surface of the seed-layer in the bottom of the resist openings. This step ensures good adhesion between the seed-layer and the following CPB's metal layer stack as shown in Fig. 10 e). The CPB itself is created by the subsequent electrochemical metal deposition of copper, nickel, and tin-silver alloy in the photoresist's openings, which is illustrated in Fig. 10 f). The photoresist and the metal seed-layer are removed and the cylindrical shaped tin-silver alloy is transformed into a spherical cap by briefly heating the whole wafer above the liquidus temperature of the tin-silver alloy, as shown in Fig. 10 g) – i). Singularization of the wafer to individual components is performed by firstly half-cut dicing from the top side of the wafer followed by a transfer of the wafer top down into a grinding foil. Then the wafer is thinned by grinding the wafer's back side until reaching the dicing streets of the front side, hence separating the wafer in single components as illustrated in Fig. 10 j) – k). The singulated components are transferred to a frame from where the components can be packed into a tape, as shown in Fig. 10 l) and Fig. 10 m). The tape is rolled up on a reel and can be used to feed components to an automated pick and place assembly machine.

In this work only standard industrial tools were used for CPBs manufacturing but due to confidentiality agreements the tool designations cannot be named. The process development was performed on LN ($LiNbO_3$) wafers only which have a rather strong anisotropic thermal expansion and show piezo- and pyroelectricity. Hence, LN is creating an electrical voltage if exposed to heat or mechanical stress which can create damage by electrostatic discharge (ESD). Further, the anisotropic CTE leads to wafer bowing during heat-inducing processes. This is difficult to manage for automated wafer handlers and may hamper a uniform heat distribution in hot plate processes.

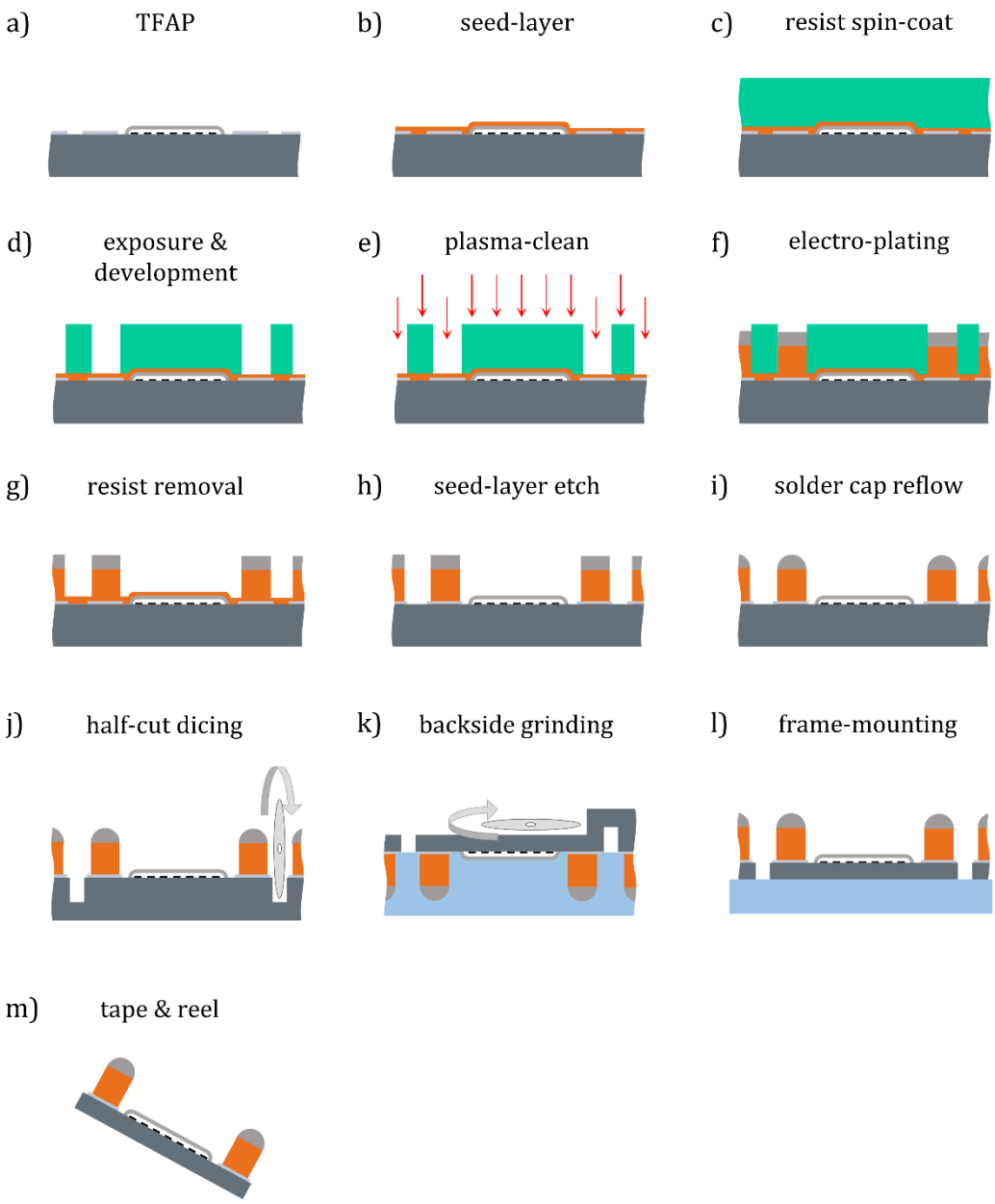


Fig. 10. Schematic cross-sectional overview of CPB manufacturing on a TFAP. Fabrication of CPBs on an already processed TFAP is performed at wafer-level. Schematic illustration of a cross-section of a single chip on the wafer with partly two neighboring chips. In a) the fully processed TFAP with the air cavity above the micro-acoustic filter structures (dashed black line). In b) seed-layer deposition of a thin Ti and Cu layer. Photoresist application by spin-coating in c) and partial UV-light exposure followed by puddle development in d) to open the resist. In e) plasma cleaning step to remove resist residues in the openings. Electro-plating of a copper, nickel, and tin-silver alloy layer stack in f). In g) and h) removal of the resist and seed-layer, respectively. In i) spherical solder cap formation by reflowing above liquidus temperature of tin-silver alloy. Wafer singularization via half cut dicing in j) followed by a transfer to a grinding foil and back side grinding until component singularization in k). Singulated components are transferred in a frame foil in l). In m) the component is ready for taping.

Overall, the thin LN wafers are very prone to fracture and must be carefully handled. However, tools and processes were adjusted to deal with LN material to avoid any wafer breakage. The respective manufacturing steps are described in more detail in the following chapters 2.2 to 2.8.

In Fig. 11 a) a fully processed SAW duplexer with CPBs as interconnection technology is shown. The SEM image (with secondary electron detector) shows

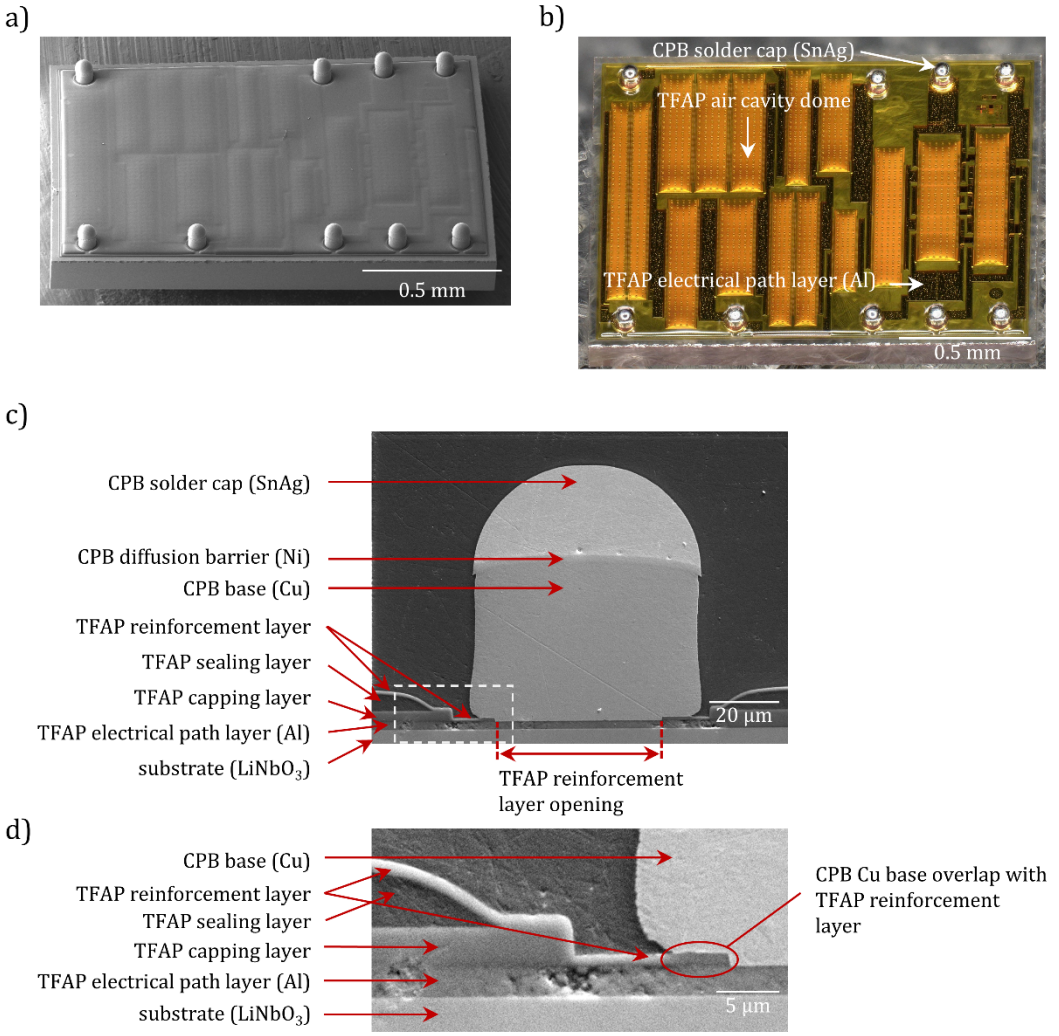


Fig. 11. a) shows an oblique top view SEM image of a fully processed 1.2 x 1.6 mm² SAW duplexer with a TFAP and CPBs. The SEM image reveals slightly the topology of the TFAP air cavity domes and the EP layer. b) shows the corresponding oblique top view optical microscopy image of a). In c) a SEM image of a mechanical cross-section through the CPB is shown. The different layers are named in the image. The area inside the dashed line of c) is magnified in d) and shows in more detail the layer structure of TFAP in combination with CPBs. The defects in the EP layer are due to mechanical polish during cross-section preparation.

slightly the topology of the air cavities below the TFAP layer stack. In Fig. 11 b) the corresponding optical microscopy image of the same SAW RF-filter chip type is shown. The substrate material $LiNbO_3$ and the TFAP layer stack are transparent in the visible light spectra. The EP layer is opaque, the TFAP air cavity domes appear goldish, and the CPB's solder caps are silver. Fig. 11 c) shows a mechanical cross-section through a CPB and the adjacent TFAP layer stacks. Reliability studies in this work showed that the reinforcement layer opening size is a crucial parameter for the reliability of the component. A magnification showing the TFAP layers at one edge of the CPB Cu base is displayed in Fig. 11 d). The TFAP reinforcement layer opening defines the electrically conducting contact area between EP layer and CPB Cu base. Shear force tests revealed that the adhesion between the brittle reinforcement layer and the EP layer is lower than the adhesion between CPB and EP layer. Therefore, mostly the reinforcement layer opening defines the mechanical strength of the connection between CPB and TFAP RF-Filter chip. It can be seen in Fig. 11 d) that the reinforcement layer is the top layer of the whole TFAP and covers all other layers below. Therefore, the CPB base overlaps (Fig. 11 d)) with the reinforcement layer to achieve a hermetically sealed package.

2.2 Seed-Layer Deposition

The seed-layer is a very thin metallic layer stack, which is deposited on the whole wafer after TFAP fabrication as shown in Fig. 12. It is the first step of CPB manufacturing. The very thin metallic layer stack consists of a 50 nm Ti (titanium) thin film followed by a 200 nm Cu (copper) film. The main purpose of the seed-layer is to build an electrically conducting surface on the wafer onto the already manufactured TFAPs. This is needed for the later electrochemical (galvanic) metal deposition of the CPBs. Ti acts as a diffusion barrier and an adhesion promoter between the Al (aluminum) EP-layer (electrical path) and the thin Cu seed-layer and CPB, respectively. However, a thin layer is needed as the seed-layer must be removed

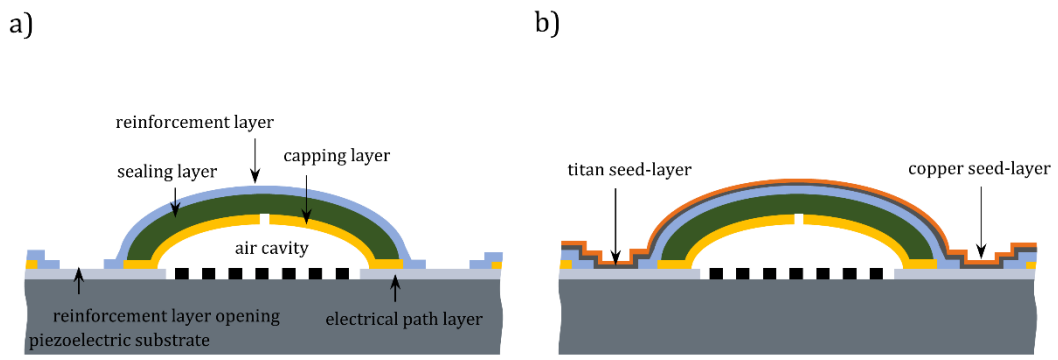


Fig. 12. Schematic cross-sectional sketch prior seed-layer deposition in a) and after seed-layer deposition on TFAP in b). The seed-layer consists of 50 nm Ti as first layer directly followed by 200 nm Cu as second layer. Deposition is performed on the whole wafer by physical vapor deposition after TFAP fabrication.

completely in a later process step to avoid electrically short circuited CPB interconnections.

The seed-layer was deposited via physical vapor deposition (PVD) in a commercial magnetron sputter deposition plasma tool. This tool is separated in three successive chambers. The first chamber is the low-pressure loading area, second is the cleaning chamber and the third camber is the magnetron sputter deposition chamber. First, up to 4 wafers are bombarded simultaneously with ions in the cleaning chamber to remove contaminations and metal oxides from the surface. This step ensures good adhesion and a good electrical conduction between the seed-layer and the EP layer by removing aluminum oxide which naturally grows at the EP layers surface if exposed to air. The wafer is then forwarded into the third chamber for sputter deposition. During the sputter process, non-thermal vaporized material from a Ti and a Cu target is condensed on the wafer, respectively. The target material is being sputtered, i.e. bombarded with accelerated high energy ions from a plasma source. The bombarding transfers a momentum into the target which creates a collision cascade inside the target. Some of this momentum can reach back to the surface of the target and unleash/sputter atoms (ions) from the target material, which are then deposited as a thin film on the wafer. The deposition rates of the metal films were determined on flat wafers via ellipsometry film thickness measurements. Deposition times for Ti and Cu were chosen accordingly to achieve a thickness of 50 nm Ti and 200 nm Cu.

However, the sputtering process is anisotropic, i.e. the resulting film thickness is dependent on the topology of the wafer. Surfaces parallel to the target achieve the highest film thickness compared to sloped surface areas. As the target is narrower in its geometry than the wafer itself, the wafer holder is constantly moved forward and backwards below the target during the sputtering process. The movement and the prolonged target geometry allow a uniform thickness distribution and a better sidewall covering of sloped topology on the wafer. Preliminary tests have shown that on topology with vertical sidewalls (no negative slope) roughly a third of the film thickness compared to a flat surface can be expected. Later tests confirmed that a Cu seed layer thickness of only 100 nm on the TFAP topology is sufficient for electroplating without visible defects. However, it was decided to use a stack of 50 nm Ti followed by 200 nm Cu seed-layer to ensure good covering on the topology sidewalls resulting in a completely sealed surface below the seed-layer.

2.3 Photolithography

Photolithography is a process which transfers a relief-like pattern into a light sensitive photoresist (polymer) coated on substrate (e.g. wafer) by exposing the photoresist with light at defined areas. In most cases the exposure is done through a photo-mask having light transparent and non-transparent areas. Therefore, typically a resist coating, a UV-light exposure, and a development process is needed, which may include several bake steps at elevated temperatures. In this work for every lithographic process step a dedicated tool was used. The photoresist application was performed on a spin-coater, the UV-light exposure was performed on a mask aligner, and the photoresist opening was done at a developer tool. All tools used, complied with industrial production standard. The lithography processes create relief-like patterns on the substrate with either remaining photoresist or areas where the photoresist is removed during the development process. This is caused by strongly differing dissolution rates between light exposed or non-exposed photoresist areas. Some areas on the substrate are masked by the remaining photoresist after the

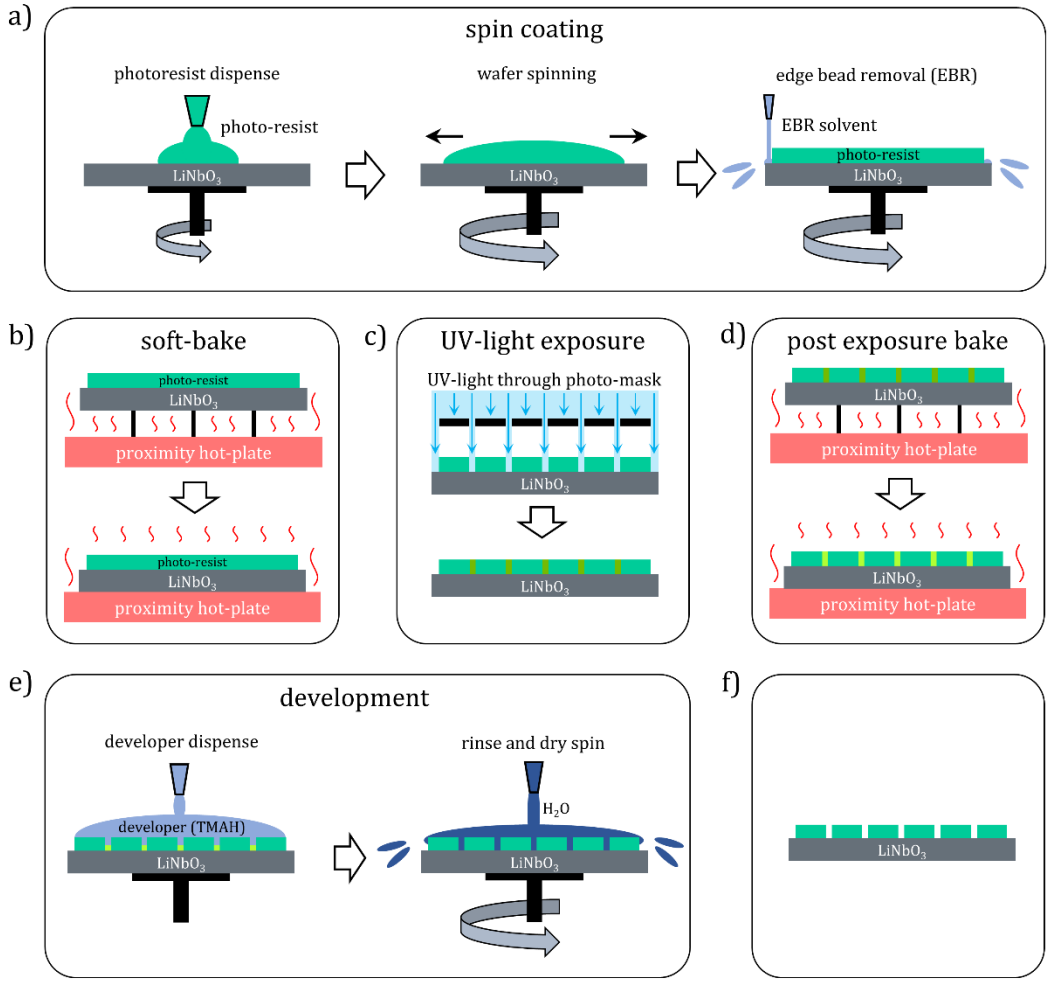


Fig. 13. Schematic cross-sectional overview of lithographic process steps to structure the positive tone photoresist for CPB manufacturing. a) illustrates the dispense and spread of the photoresist on the wafer by rotating the wafer. A fine solvent jet removes excessive photoresist at the wafer edge at the end of the spin coating process. The soft bake in b) evaporates excessive solvent from the photoresist whereby it dries. A proximity hotplate was used, which allows a slow lowering of the fragile LN wafer to prevent temperature induced wafer breakage and a gentle start of solvent evaporation. A second soft bake at higher temperature might be advantageous for gentle thick film photoresist drying. c) shows the UV-light exposure of defined areas through a photo-mask. If a chemically amplified photoresist is used an acid is produced in the exposed areas. This acid acts as a chemical catalyst and changes the solubility of the photoresist. During the post exposure bake, as shown in d), this chemical reaction is strongly accelerated. Therefore, in step e) the UV-light exposed areas are dissolved into the developer medium. Then a water rinse and the dry spinning of the wafer follows. In image f) the relief-like pattern in the photoresist is shown. Every hotplate step is followed by a cool down on a cool plate, which is not shown in this image.

lithography process. Hence, the initial surface of the substrate is covered in the following process steps. This allows to apply a certain process on defined positions of the substrate. In this work, photolithography is used to create small openings with a diameter of 55-75 µm in a 80-100 µm thick photoresist layer. The photoresist is

applied by spin coating. Here the liquid photoresist is usually dispensed in the middle of the spinning wafer, which forces the photoresist to spread on the wafer even following the eventual topology of the wafer. By adjusting the spin coating parameters, the required photoresist film thickness and uniformity can be adjusted in a certain range. However, every photoresist has its own individual limits in terms of e.g. achievable film thickness, photo-speed or resolution limits, which makes it essential to choose potential resists carefully according to the required properties, prior hands-on process development. A bake step at increased temperature dries the photoresist after spin coating by evaporating the excessive solvent from the photoresist. The simplified process steps for lithography used here are shown in Fig. 13.

Photoresists are distinguished in two polarities, namely, positive and negative tone photoresists. The basic principle of a photoresist is the difference in their dissolution rates during the development process, which is induced by light exposure, starting a chemical reaction. A negative tone photoresist shows a low dissolution rate in light exposed areas, due to e.g. a polymer cross-linking reaction. In unexposed areas of a negative tone photoresist, a much higher dissolution rate compared to exposed areas can be observed during development. Additionally, chemical side groups may define the chemical polarity of the polymer molecules, and therefore further influence the solubility in the developer medium. In contrast, a positive tone photoresist shows a high dissolution rate in light exposed areas due to e.g. a chemical reaction which changes the polarity of the photoresist's polymer molecules. The thereby induced solubility increase leads to a highly different dissolution rate between exposed and unexposed photoresist areas.

However, photoresists are divided into two further groups, namely, chemically amplified and non-chemically amplified photoresists. In a non-chemically amplified photoresist, one photon leads to a limited number (<1) of chemical reactions after light exposure, which is changing the dissolution rate. In contrast, a chemically amplified photoresist first generates a catalyst (usually a strong acid/proton) during light exposure. The catalyst itself drives the chemical reactions to change the

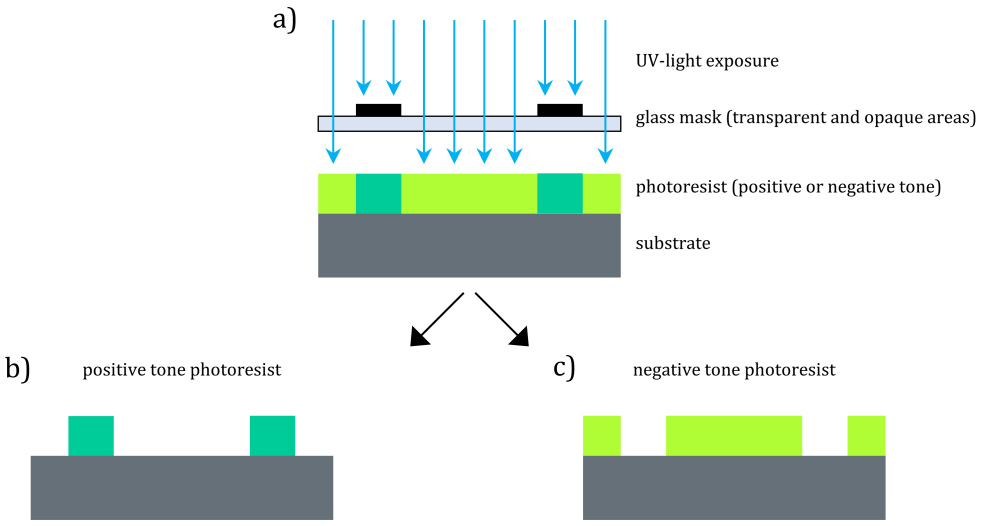


Fig. 14. Simplified schematic cross-sectional view to compare the resulting relief like pattern of a positive and negative tone photoresist after lithographic processing. In a) the UV-light exposure of a photoresist (either positive or negative tone) through a glass mask with transparent and opaque areas is shown. Depending on the photoresist's polarity the resulting relief like pattern of a in b) positive tone and a in c) negative tone photo resist is illustrated after all lithographic processes.

dissolution rate in the photoresist but is not consumed during the reaction. Therefore, in a chemically amplified photoresist one photon can trigger multiple chemical reactions by the created catalyst, to increase the solubility in the developer medium. This typically leads to much more light sensitive photoresists (higher photo-speed). The catalyst is generated during light exposure by the so called photoacid generator (PAG), which is a photoresist ingredient. Usually, the chemical reaction driven by the catalyst, is accelerated by a post exposure bake at increased temperature. Fig. 14 shows the remaining relief-like photoresist structure related to a positive and a negative tone photoresist after exposure and development process.

In this study, a non-chemically amplified negative tone photoresist and a chemically amplified positive tone photoresist was used for the lithographic part of the CPB manufacturing process development. Unfortunately, the negative tone resist proved to be unsuitable on the current TFAP design, due to photoresist residues in the intended resist openings. These photoresist residues prevent a reliable electrochemical metal deposition in the following CPB manufacturing process step, which then may cause issues in the component reliability. Nevertheless, the results of

the negative tone photoresist will be discussed as the lithography process might work well for different topologies around the intended photoresist openings.

The UV-light exposure process was performed at a standard mask aligner tool. In a mask aligner the whole wafer is exposed by UV-light through a photo-mask at once. The photo-mask consists of a UV-light transparent glass substrate with non-transparent areas made of a thin chromium layer. The photo-mask and its features have the same size as the features of the projected image onto the wafer. The photomask needs to be very close to the wafer to limit light diffraction, which cause a poor pattern transfer in the photoresist. Therefore, two different modes, namely, contact mode or non-contact mode are typically used. In contact mode the photo-mask is placed directly onto the wafer/photoresist, i.e. having no gap between each other achieving the highest resolution of the transferred pattern. However, with the used photoresist types contaminations of the photo-mask are very likely. The contaminations cause exposure defects on the following exposed wafers until the photo-mask is cleaned. Hence, the non-contact mode was used, where a defined gap between the wafer/photoresist and the photo-mask is provided. Prior loading the wafer on the exposure chuck, its thickness is measured including the photoresist layer, which then allows to set a defined gap between mask and photoresist surface. However, for the intended smallest resist opening diameters of approx. 45 µm, an exposure gap of 80 µm combined with the optics used in the mask aligner, the achievable resolution is not a limiting factor. Prior exposure it must be ensured that the intended resist openings are at the right position on the wafer. Therefore, an alignment between the wafer and the photo-mask is required. This step is very critical, as misalignment might cause issues in the later component assembly and the component reliability. The alignment is performed by optically overlaying known structures, the so-called alignment marks, on the photo-mask and the wafer, respectively. The wafer has two alignment marks on opposed sides at the wafer edge. The marks are already structured in the EP-layer during TAFP manufacturing and are protected against damage during the following processes. The associated marks for the overlay are on the photo-mask. For alignment a simple cross in cross structure was used and the overlay was set by top view optical inspection. However, the whole

alignment is automatically executed by the mask aligner after optically teaching the alignment marks and by defining their gross positions on the wafer and the photo-mask, respectively. The UV-light source was a mercury vapor lamp. Only the i-line wavelength at 365 nm was emitted to the wafer through a filter. The UV-light dose in [mJ/cm^2] and the exposure gap between photomask and resist surface was regularly calibrated according to industry standards.

Required baking steps at increased temperature to evaporate excessive solvent after spin coating or to enhance the solubility changing chemical reaction after the exposure of a chemically amplified resist were performed on proximity hot-plates. The hot-plates were either in the spin coater tool or in the developer tool. Proximity pins in the hot-plates allow a controlled slow lowering of the wafer onto the hot-plate to avoid temperature induced breakage of the fragile pyro- and piezoelectric LN wafers. The same procedure was applied on the cool-plates.

The development process was performed as a liquid puddle development with a 2.38 wt% TMAH (tetramethylammonium hydroxide) aqueous based developer in standard industry quality followed by a deionized water rinse.

The lithographic process steps of the negative tone and positive tone photoresist are different. Therefore, the exact process steps, conditions and results are explained in the following two chapters for each photoresist. One of the major challenges during lithographic process development was to overcome poor coating results due to the high topology on the wafer induced by the TFAP and the achievement of the required high photoresist film thickness combined with the imprint of high aspect features. An additional challenge was the development of a suitable process to clean the bottom of the created photoresist openings without deforming or damaging the photoresist itself. The cleaning step is mandatory to ensure good adhesion of the CPBs, which is described in chapter 2.4 Plasma Cleaning.

Further very well summarized and more detailed information about photolithography, photoresists working principals, chemical compositions, image configurations and the respective tool working principles can be found in [40–42].

2.3.1 Negative Tone Photoresist

The first choice fell on a non-chemically amplified negative tone thick film photoresist. This chapter will only give a very brief overview of the negative tone photoresist, the processing issues, and the strategies to solve them. The used negative tone photoresist chemically crosslinks when exposed to UV-light, which is beneficial for chemical and temperature stability. The temperature stability is important for the necessary plasma cleaning after lithography to remove potential residues. However, due to topography induced photoresist cross-linking by scattered UV-light which caused serious residues in the intendent openings, the negative tone photoresist was not suitable in combination with TFAP topology. A different or missing topology

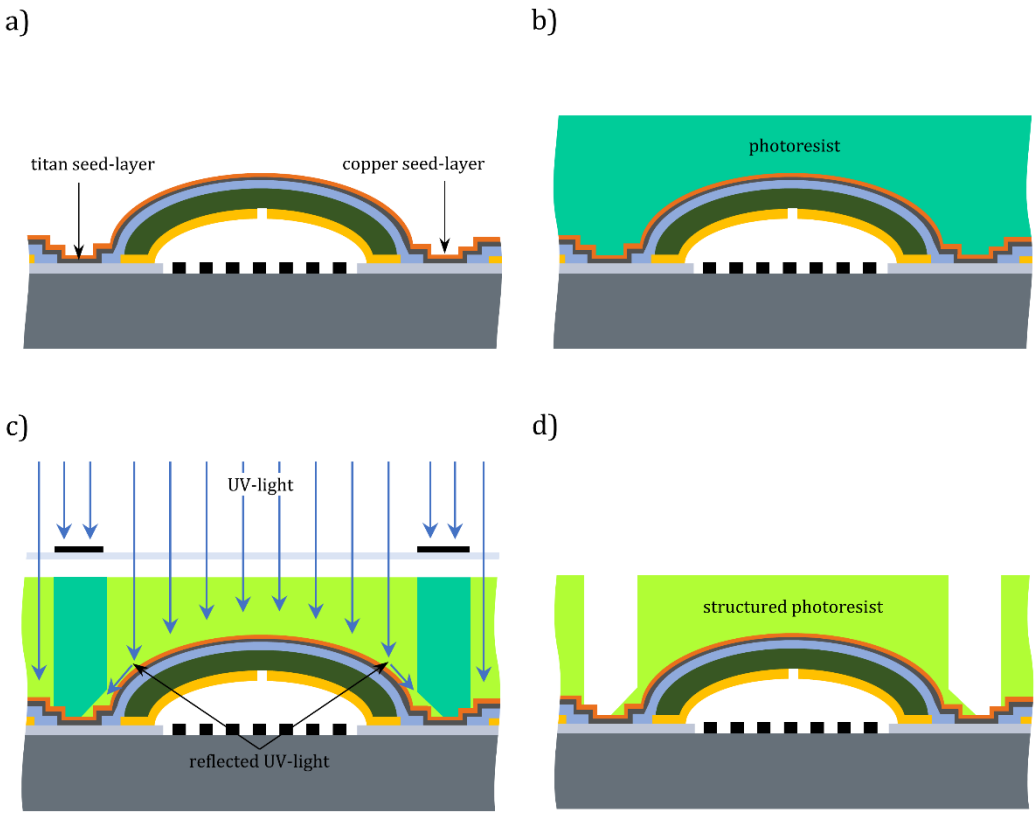


Fig. 15. Schematic cross-section of lithography process steps with negative tone photoresist. In a) the seed layer prior lithography. The photoresist is spin coated on the bare seed layer and dried during a one-step softbake to create a uniform photoresist thick film above the TFAP as shown in b). In c) the photoresist is exposed with UV light through a photomask. Only in the area for the intended photoresist openings the negative tone photoresist is not exposed by UV-light. However, the TPAF topology scatters UV-light into the area of the intended openings and cross-links the photoresist. Directly after exposure the puddle development follows, and the photoresist is opened at the non-exposed areas.

which surrounds the intendent photoresist openings would allow the use of this photoresist. But the change of the whole TFAP design was evaluated to have a high reliability risk because several layers would be affected by the redesign. Thus, the redesign was not conducted. Fig. 15 illustrates the lithography process using a negative tone resist. The schematic cross-section in Fig. 15 c) shows the emerge of reflected light from the surrounding TFAP topology, creating cross-linked photoresist in the intended opening area.

The photoresist was applied by a single coat including a solvent prewet and reached a minimum film thickness of 80 µm. A one-step softbake at 120 °C for 300 s was performed to evaporate excessive solvent. The LN wafer is lowered slowly towards the hotplate at the beginning of the softbake. The negative tone photoresist was exposed on a mask-aligner tool with 500 mJ/cm^2 (i-line wavelength at 365 nm) at an exposure gap of 80 µm directly followed by a puddle development. In total 4 puddles each 70 s with aqueous based TMHA developer opened the photoresist.

In Fig. 16 the cross-linked photoresist in the intended openings can clearly be seen. Even varying the number of puddles, the exposure dose, the exposure spectra, the softbake duration, the exposure gap, or changing the reflectivity of the seed-layer by oxidation, resulted in strong residues inside the round photoresist openings. The squared openings were less impacted by this phenomenon. One reason could be that the round topology focuses the scattered light into the opening. Antireflective

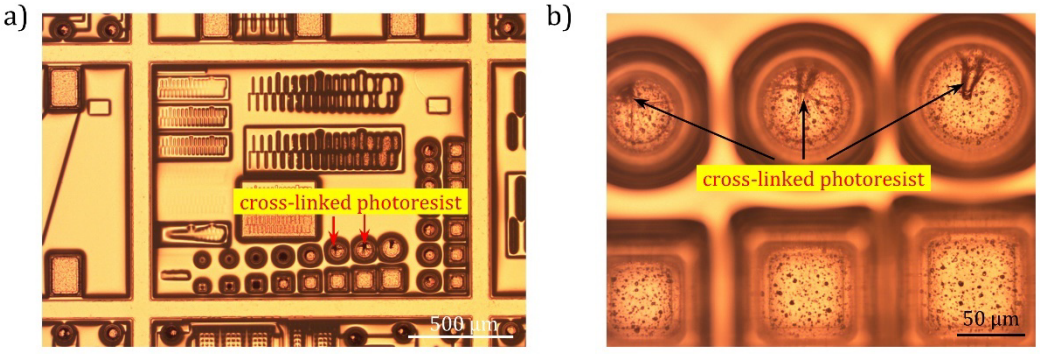


Fig. 16. Top view micrographs after lithography with negative tone photoresist. In a) round and squared openings with varying dimensions. Inside the photoresist openings cross-linked photoresist due to scattered light can clearly be seen. In b) more magnified negative tone photoresist openings with resist residues.

coating was not considered due to the extra processing steps and the resulting material and cost increase. Therefore, after multiple failed experiments to avoid the cross-linking inside the round shaped photoresist openings by adjusting lithography parameters, the decision was made to switch to a positive tone photoresist.

2.3.2 Positive Tone Photoresist

A large part of this chapter was already published in [43].

Due to the cross-linking issue of the negative tone photoresist, a commercial chemically amplified thick film photoresist with a viscosity of 4900 cSt was used for CPB lithography. The photoresist was applied by spin coating, followed by a two-step

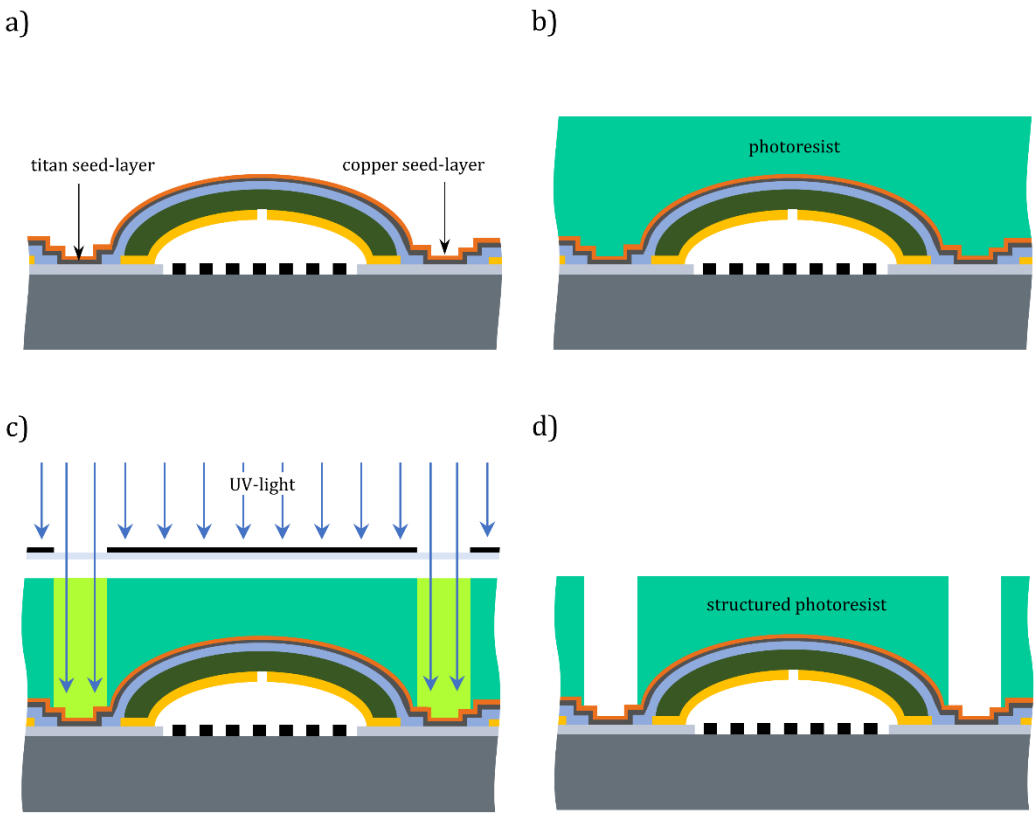


Fig. 17. Schematic cross-section of lithography process steps with positive tone photoresist. In a) the seed-layer prior lithography. The photoresist is spin coated on the bare seed-layer and dried during a two-step softbake to create a uniform photoresist thick film above the TFAP as shown in b). In c) the photoresist is exposed with UV-light through a photomask only in the area for the intended photoresist openings. After post exposure bake and the puddle development, the photoresist is opened at the UV-light exposed areas.

softbake for solvent evaporation, exposure on a mask aligner tool, post exposure bake (PEB), and a puddle development with TMHA based developer as shown in Fig. 17. The minimum of 80 µm film thickness required by the CPB electroplating was achieved with a single coat including a solvent prewet. The film thickness was measured via interferometry at approx. 2080 measurement points on a wafer with TFAPs after the two-step softbake. The photoresist film thickness is illustrated as thickness-map in Fig. 18. The measurement positions are on a dedicated test structure on the wafer. Wafer alignment marks, a corresponding wafer map, and a optical pattern recognition allow to precisely find the measurement point. Fig. 18 shows the edge bead, i.e. a higher film thickness at the wafer edge. Further, a thicker film thickness is present close to the wafer center and at three positions approx. at the half of the wafer radius as indicated with white dashed lines in Fig. 18. The increased film thickness is caused by a higher evaporation rate of the solvent, which creates a material flow to this exact area. The material flow carries solvent but also solid material, which is then not evaporated but increasing the remaining film thickness. At the wafer edge a larger ratio of air volume and resist area leads to a higher evaporation rate. The increased film thickness in the wafer center is caused by the proximity balls of the hotplate, which are the main physical contact during the soft bake process, hence the transferred heat quantity is increased. However, LN is a very fragile material, and the wafer therefore is lowered slowly, while laying on three hotplate pins, towards the hotplate and the proximity balls, respectively. These pins (indicated in Fig. 13 d)) transfer more heat quantity into the wafer; thus, evaporation starts earlier and faster in this wafer areas and film, increasing the film thickness. Nonetheless, the achieved film thickness and uniformity was sufficient for CPB electroplating. A better film thickness uniformity could probably be achieved by a double coat of the photoresist. Unfortunately, this would have the consequence of higher costs due to the need of increased amount of photoresist and spin coating tools.

The prewet with PGMEA (1-methoxy-2-propanol acetate) before dispensing the photoresist was mandatory because the complex topography of the TFAP tends to trap air inside the photoresist during spread out. This effect is enhanced using a

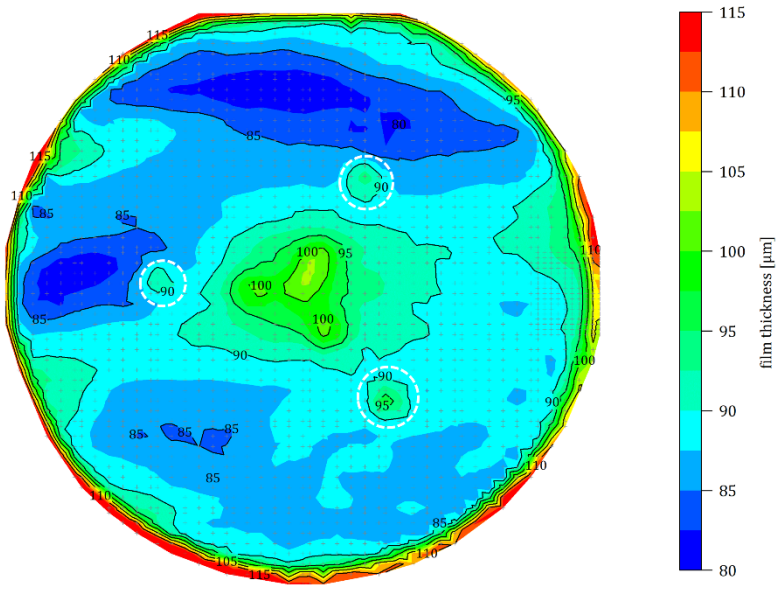


Fig. 18. Positive tone photoresist film thickness distribution on a 150 mm LN wafer with TFAPs measured via interferometry at approx. 2080 defined positions on the wafer. Measurement positions are indicated by crosses. Dashed lines indicate increased film thickness in the area of the hotplate pins.

multi-design wafer layout, where many different TFAP designs, and test structures are present on the same wafer. In the case of trapped air, bubbles are formed inside the photoresist, which grow during softbake. The air bubbles with a size of approx. 1 mm cause defects in the lithography. Further, the air bubbles contaminate the photomask by physical contact during exposure, which then cause defects on all following wafers if the photomask is not cleaned.

For the prewet step, PGMEA is dispensed onto the wafer prior to the photoresist to wet the whole wafer surface. Even topology with a high aspect ratio is filled by the solvent, which prevents the enclosure of air during spin coating. PGMEA is also an ingredient in the photoresist. Only small amounts of the solvent stay on the wafer surface and are mixed with the photoresist. However, there was no noticeable change in photoresist performance with a PGMEA prewet. The spin coat recipe for a 150 mm LN wafer with TFAPs is shown in Table 1 and as a graph in Fig. 19.

Table 1. Spin coat recipe of positive tone resist for thick-film lithography.

Step	Duration [s]	rotational speed [rpm]	Acceleration [rpm/s]	Function
1	4	60	100	solvent prewet (10 s)
2	6.5	800	800	
3	1	1800	2000	
4	2	0	2000	
5	3.5	0	0	photoresist dispense (12 s)
6	6	350	75	
7	9	870	101	
8	3	800	100	
9	10.5	600	100	
10	31	450	100	solvent - edge bead remove (30 s)
11	0.4	1400	3300	
12	1.5	0	3300	

A photoresist volume of 7.9 ml was dynamically dispensed in the center of the wafer with a duration of 12 s. After spin coating a two-step softbake was performed to evaporate the excessive solvent. Each softbake was performed on a proximity hotplate.

The first softbake was at 85 °C for 120 s directly followed by the second softbake at 135 °C for 480 s. The exposure dose was set to 1200 mJ/cm^2 (related to broad band calibration of mercury vapor lamp) using only the i-line spectra with a wavelength of 365 nm. A post exposure bake directly after the exposure at 100 °C for 100 s accelerates the chemical reaction for the solubility change of the light exposed photoresist areas. Followed by the development with an aqueous TMHA based developer creating five puddles on the wafer, each 60 s duration to ensure a complete and uniform opening of the photoresist. These lithography parameters were chosen according to a design of experiment (DoE) which evaluated the main impacts on the lithography performance when varying these parameters. Prior spin coating no

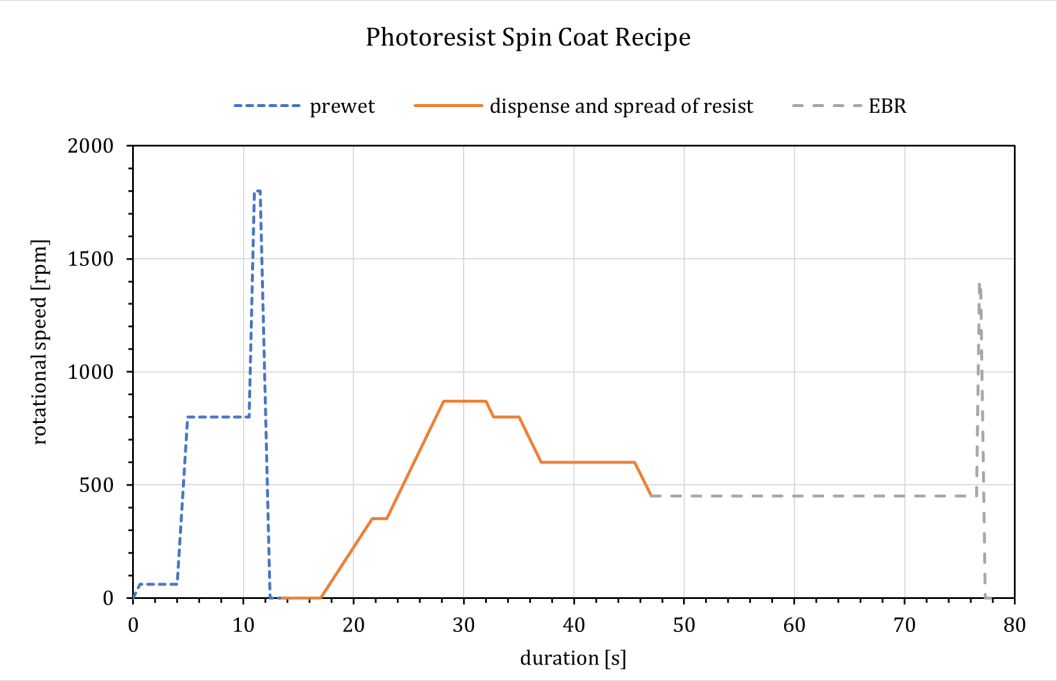


Fig. 19. Spin coat recipe of positive tone resist for thick film lithography. Graph shows rotational speed during spin coating vs. duration. Different process sections like prewet with solvent, dispense and spread of photoresist, and edge bead removal (EBR) are indicated.

adhesion promoter like HMDS (hexamethyldisilazane) is used because the photoresist already has excellent adhesion to the metallic seed-layer.

As mentioned, the lithography parameters were chosen after investigating the impact of those on the photoresist opening shape. The first and the second softbake duration, the exposure dose, the post exposure bake duration, and the number of

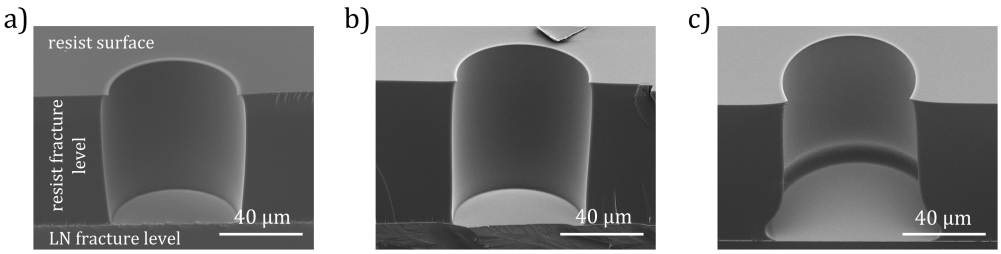


Fig. 20. SEM images of photoresist opening cross-sections with different duration times at the second softbake to compare opening shapes. Sample preparation by defined LN wafer breakage. In the center of each image half of the cylindrical photoresist opening. Fracture levels are exemplary indicated in a). The second softbake duration times are a) 360 s, b) 540 s, and c) 720 s.

development puddles were varied. The experiments were performed on blank LN substrates with the corresponding seed-layer of Ti and Cu but without any TFAP topology. After seed-layer deposition on the dummy wafers, photoresist was applied

Table 2. Detailed lithography parameters to investigate the impact on photoresist openings. Based on the investigation, the parameters of sample 9 (green highlighted) were chosen for lithography manufacturing.

	Step	seed-layer 50 nm Ti + 200 nm Cu	photoresist spin coating	first softbake	second softbake	exposure dose with 80 µm exposure gap			PEB duration at 100 °C			number of development puddles		plasma descum	Cu electroplating and resist removal	mean value of resist bottom diameter
	Parameter	50 nm / 200 nm	80 µm	85 °C for 120 s	135 °C for 480 s	900 mJ/cm^2	1200 mJ/cm^2	1500 mJ/cm^2	80 s	100 s	120 s	5	7	B_3-O2CF4 – 45 s	75 µm Cu	[µm]
Sample	1	x	x	x	x	x			x			x		x	x	63.2
	2	x	x	x	x	x			x				x	x	x	61.9
	3	x	x	x	x	x				x		x		x	x	64.6
	4	x	x	x	x	x				x			x	x	x	63.9
	5	x	x	x	x	x					x	x		x	x	64.3
	6	x	x	x	x	x					x		x	x	x	65.6
	7	x	x	x	x		x		x			x		x	x	66.2
	8	x	x	x	x		x		x				x	x	x	66.2
	9	x	x	x	x		x			x		x		x	x	66.0
	10	x	x	x	x		x			x			x	x	x	67.5
	11	x	x	x	x		x				x	x		x	x	68.0
	12	x	x	x	x		x				x		x	x	x	67.6
	13	x	x	x	x			x	x			x		x	x	68.2
	14	x	x	x	x			x	x				x	x	x	67.0
	15	x	x	x	x			x		x		x		x	x	69.9
	16	x	x	x	x			x		x			x	x	x	70.3
	17	x	x	x	x			x			x	x		x	x	71.6
	18	x	x	x	x			x			x		x	x	x	71.3

always by the standard spin coating recipe. The variation of the first softbake duration at 85 °C had no significant influence on the resist dryness nor photoresist opening shapes. However, the duration of the second softbake at 135 °C had a significant impact on resist dryness and the shape of the photoresist opening. The second softbake test duration times at 135 °C were 360 s, 540 s, and 720 s. The cross-section image in Fig. 20 a) shows a photoresist opening which is narrowing towards the bottom, i.e. the LN substrate when using 360 s at 135 °C. A duration of 520 s at 135 °C leads to almost vertical sidewalls of the photoresist openings as shown in Fig. 20 b). However, if the duration of the second softbake at 135 C is 720 s, the bottom area of the photoresist openings strongly broadens as illustrated in Fig. 20 c).

The dryness of the photoresist was reviewed by two tests. First the detection of film thickness loss saturation and second by sandwiching a paper sheet between two 150 mm LN wafers with photoresist face-to-face under a mechanical load of 400 g.

For softbake durations greater than 350 s only slightly further film thickness loss was detected by interferometry, because the solvent content in the remaining photoresist is already low. However, the mechanical dryness test revealed, that the photoresist appears still soft when using softbake duration below 420 s at 135°C as the imprint of the sandwiched paper was visible after 4 h of mechanical load. However, the impact of the second softbake duration at 135 °C on photoresist dryness and the opening shapes can be seen clearly. Therefore, because of almost vertical sidewall shape of the photoresist opening and the ensured dryness, a duration of 480 s at 135 °C was used for further lithography investigation.

The aim of the parameter variation was to investigate the impact on the photoresist opening shape and its dimension. It is very complex to quantitatively evaluate round shaped photoresist openings by wafer breakage followed by cross-sectional SEM images, because the break level should always be in the center of the opening. Therefore, the photoresist openings were filled by electroplating Cu. The Cu follows exactly the shape of the photoresist openings. Due to the round shape, the side view SEM images allow the exact evaluation of the dimensions. The lithography parameter variation can be seen in Table 1 defined for each test wafer. Seed-layer

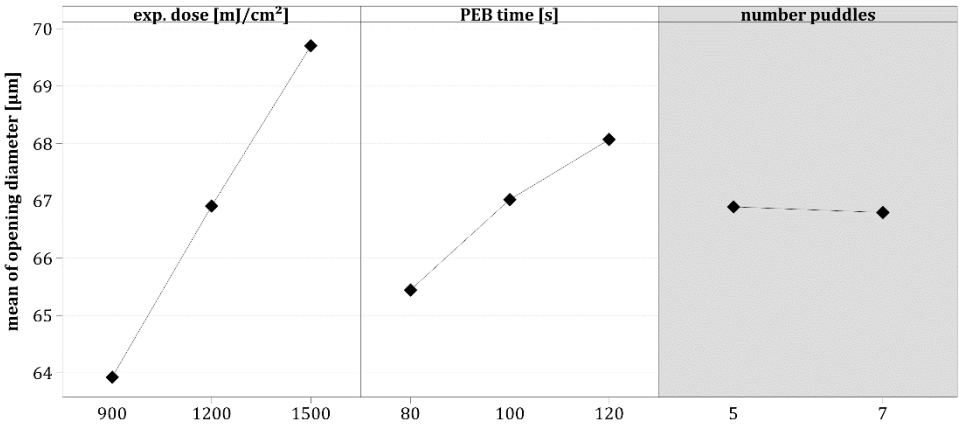


Fig. 21. Main effect diagram for photoresist opening diameter. The individual impact of exposure dose, post exposure duration, and the number of puddles for development is shown. The gray area indicates that there was no statistically relevant impact of the number of puddles.

deposition, spin coating and softbake steps were kept the same for each test wafer. Exposure dose, post exposure bake and the number of puddle developments were varied. Plasma descum cleaning after lithography, Cu electroplating, and photoresist removal were kept the same for each wafer. After that, the Cu posts on the wafer were investigated by SEM to measure the bottom diameter. The main effect diagram in Fig. 21 illustrates the impact of each individual parameter on the mean value of the photoresist opening. The higher the exposure dose or the post exposure bake duration, the higher the photoresist opening diameters. The chosen variation of the number of puddles had no significant influence. However, the steeper the slope in the diagram, the stronger the impact. The strongest effect on the mean photoresist opening diameter was caused by the exposure dose followed by the post exposure bake duration.

The main effect diagram is an easy way to demonstrate the impact of the isolated lithography parameters. However, the interaction plot allows to illustrate the combined effects on the photoresist opening diameter as shown in Fig. 22. One can see that the combination of the exposure dose and the post exposure bake duration mutually amplify when increasing both. The main effect on the photoresist opening is still the exposure dose. The number of puddles during photoresist development does not show a statistically impact when combined with exposure dose or the post

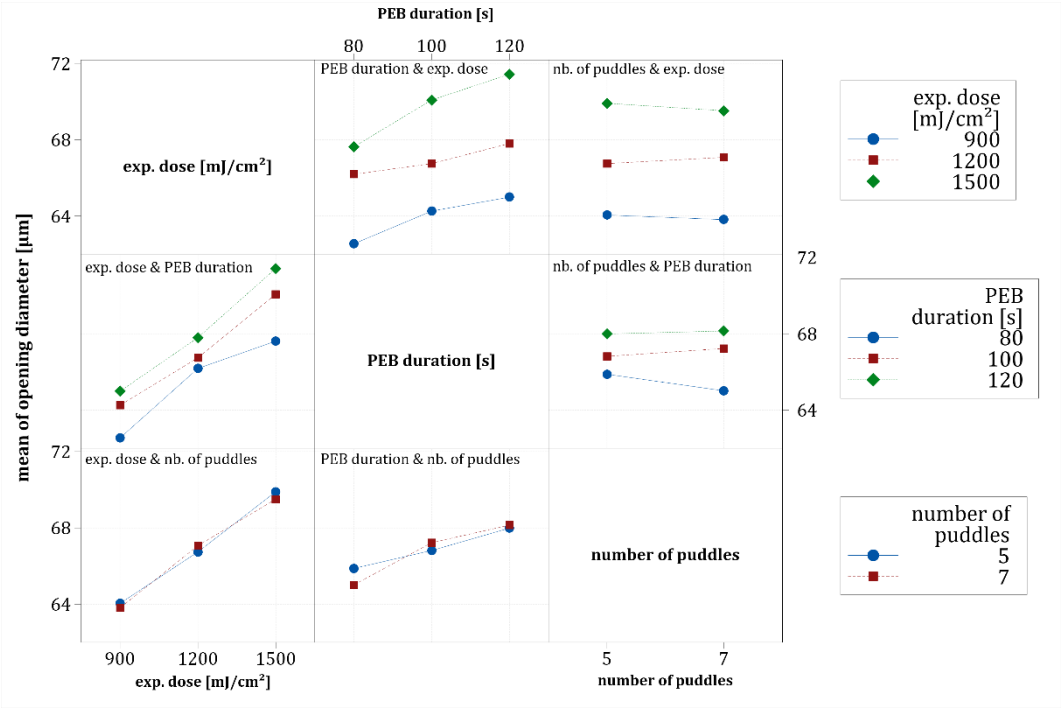


Fig. 22. Interaction plot of lithography parameter variation on photoresist opening diameter. The vertical axis is the mean value of the resist opening diameter and repetitive illustrated for each row of the interaction plot. Each box illustrates the combination of two lithography parameters. Each column has its own vertical axis, e.g. the first column represents the variation of the exposure dose, the second column the post exposure bake duration, and the third column the number of puddles. On the very right of the chart, each of the three legend boxes belongs to the adjacent row and defines the second parameter of each combination. The combined parameters are named in the upper left corner of the box.

exposure bake duration. In contrast to the second softbake duration, the varied parameters had no significant influence on the sidewall shape in the investigated range. The statistical evaluation was performed by the “minitab” software [44].

The design of experiment allowed to investigate a broad lithography process window and to quantitively understand the main effects and the interaction between them. Based on that study, the lithography parameters for 150 mm LN wafers were set like the ones of sample 9 in Table 2. Hence, variable parameters were set to 1200 mJ/cm^2 for exposure dose, 100 s duration for the post exposure bake at 100 °C, and 5 puddles each 60 s for the development. These parameters were used for the lithography manufacturing steps on structured wafers with TFAPs. However, the lithography parameter evaluation was performed on LN wafers with only seed-layer

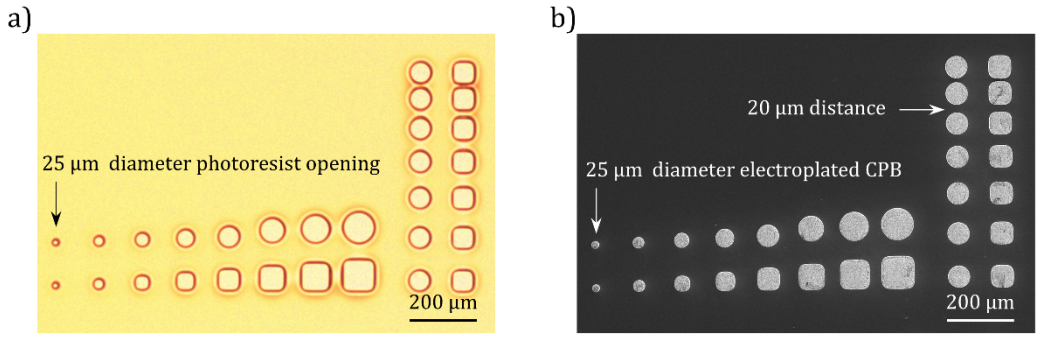


Fig. 23. Images of lithography performance related to critical dimension and feature-to-feature distance. In a) the top view micrograph of test structures. In b) the same test structures after electroplating and resist removal. The critical dimension for a film thickness of 80 µm is a diameter of 25 µm and a feature-to-feature distance of 20 µm.

on top but without topography. Therefore, the lithography results like photoresist opening diameter vary slightly when transferred to structured wafers. Nonetheless, even if the absolute values are not exactly be the same, the impact on the behavior of the photoresist and its relevant process window, to ensure a reliable process, is fully given. This lithography process allows to create photoresist openings with the intended diameter of approx. 65 µm with a minimum film thickness of 80 µm. The alignment concept ensures that the photoresist opening precisely includes the EP-layer opening and a part of the reinforcement. As a result, the later CPB will cover the whole opened EP-layer and additionally will overlap a defined area on the reinforcement layer. The smallest structure size created in the 80 µm thick photoresist was an opening with a diameter of 25 µm and a feature-to-feature distance of 20 µm, as shown in Fig. 23. A plasma clean after photolithography was mandatory to ensure good adhesion between the seed-layer and the electroplated CPB metal layer stack.

2.4 Plasma Cleaning

A plasma cleaning step to remove surface contaminations in the photoresist openings was mandatory. It ensures good adhesion between the Cu surface of the seed-layer and the electroplated Cu of the CPB base. If there is no sufficient plasma clean (also

called descum), the adhesion of the electroplated metal layer stack will be weak and the CPBs are just washed off during the photoresist removal process. However, the surface contaminations must be very thin, as no visible layer was present in cross-sectional SEM analysis for both photoresist types. Preliminary experiments showed that the increase of development puddles did not increase the adhesion of the electroplated Cu.

For the negative tone photoresist, which was not used further due to cross-linking effects in the photoresist openings when TFAP topology is present, an intense plasma which can ash organics will remove all contaminations. Especially with raised temperature the etch rate amplifies but the chemically cross-linked negative tone photoresist will not start softening, hence the openings do not start to flow.

The positive tone photoresist also requires a plasma cleaning step. However, the plasma must be softer in terms of temperature transfer on the wafer. This is due to the photoresist softening tendency when temperature is raised too high, as the positive tone photoresist is not chemically cross-linked. Standard descum processes turned out to transfer too much temperature and deform the photoresist openings or even burn the resist at the wafer edge (cotton candy). Temperatures of 100 °C already significantly soften the photoresist, which leads to a material deformation towards the photoresist openings as shown in Fig. 24 b). Therefore, various plasma processes

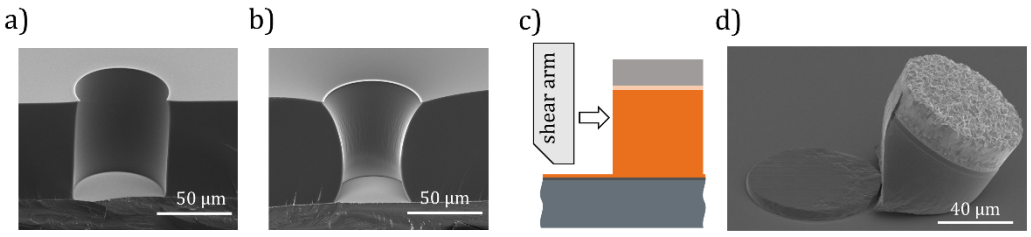


Fig. 24. a) and b) show SEM images prepared by sample breakage through the positive tone photoresist openings. In a) a cross-sectional SEM image of an opening after plasma cleaning without any defects and in b) with plasma cleaning induced photoresist deformation due to high temperature. In c) the schematic cross-section of CPB shear testing, where the shear arm moves in a defined height and speed through the CPB. The SEM image in d) shows a sheared of CPB (after photoresist removal) with a ductile fracture mode, i.e. completely sheared through the bulk material without any delamination from the seed-layer.

were tested on different tools. The quality of the plasma clean was determined via optical investigation of the photoresist opening shape and a mechanical shear test. The optical valuation was done by optical microscope or SEM as shown in Fig. 24 a).

The plasma cleaning investigation for the positive tone photoresist was performed on 150 mm LN wafers with deposited Ti/Cu seed-layer followed by the standard lithography to create photoresist openings. These wafers were exposed to different plasma processes which varied in tools, gas composition, and plasma power. The photoresist was optically inspected to detect temperature induced damages. Afterwards Cu was electroplated into the resist openings with a height of approx. 60 µm. The photoresist was removed and up to 90 CPBs with a diameter of approx. 65 µm were sheared off by a shear tool at various defined positions on the wafer. While shearing off the Cu posts with the shear tool in a defined height of 8 µm and a shear speed of 80 µm/s, the maximum force during the test is detected. If the

Table 3. Details of plasma cleaning investigation. Tools, process names, and process parameters are listed accordingly.

		Process Parameter		
Tool	Process Name	Time [s]	IC/CC Power [W]	Gas Composition
A	A_1.1 – O2	25 s	100/n.a.	O_2/N_2
	A_1.2 – O2	50 s	100/n.a.	O_2/N_2
	A_1.3 – O2	75 s	100/n.a.	O_2/N_2
B	B_1.1 – Ar/O2	30 s	500/10	Ar/O_2
	B_1.2 – Ar/O2	60 s	500/10	Ar/O_2
	B_1.3 – Ar/O2	90 s	500/10	Ar/O_2
	B_2.1 – O2/Ar	30 s	500/50	O_2/Ar
	B_2.2 – O2/Ar	60 s	500/50	O_2/Ar
	B_2.3 – O2/Ar	90 s	500/50	O_2/Ar
	B_3.1 – O2/CF4	30 s	500/50	O_2/CF_4
	B_3.2 – O2/CF4	60 s	500/50	O_2/CF_4
	B_3.3 – O2/CF4	90 s	500/50	O_2/CF_4
C	C_1.1 – O2/CF4	30 s	500/n.a.	O_2/CF_4
	C_1.2 – O2/CF4	60 s	500/n.a.	O_2/CF_4

measured force drops 90 % compared to the highest value during the running test, an additional shear distance of 10 µm is added, before the test automatically ends. A schematic cross-section of the shear test and a SEM image of a sheared off CPB is illustrated in Fig. 24 c) and d), respectively.

In total 3 different plasma tools were tested, which are named with A, B, and C. Tool A creates an IC (inductively coupled) plasma in a gas mixture of nitrogen and oxygen. Tool A can hold up to 25 wafers at once in the plasma chamber. The plasma etch is isotropic. However, due the IC power of 100 W and the number of wafers in the chamber, this plasma can be considered as a soft plasma, i.e. it creates a very low etch rate of organic residues in the photoresist openings. Nonetheless, the process of tool A creates defined surface conditions. Therefore, the process of tool A was always additionally used prior electroplating to ensure equal wettability of electrolyte inside the photoresist openings, e.g. if the wafers are not directly processed at electroplating.

Tool B is a single wafer tool, i.e. only one wafer can be processed at once inside the plasma chamber. Tool B allows electrostatic chucking of the wafer onto the wafer chuck. In addition, the chuck actively cools the wafer by a helium gas flow at the backside of the wafer. The cooling was set to a temperature of 16 °C for all processes with tool B. This allows to use more powerful plasma conditions but keeping the wafer and photoresist temperature in a non-critical range. Tool B creates an IC plasma which acts isotropic and additionally a CC (conductively coupled) plasma which enables ion bombarding towards the wafer. The ion bombarding is an anisotropic etch process. In Tool B different gas mixtures were tested.

Tool C is also a single wafer tool. However, it did not provide an active wafer cooling, which created a significant temperature increase of the wafer. This led to photoresist opening shape deformation and burned photoresist at the wafer edge. Due to the temperature raise and electrostatic charge the LN wafers started to bow during plasma processing in tool C. This caused a higher energy impact at the wafer edge and triggered the photoresist burn. Even after customization of the plasma process, tool C was not suitable for a plasma clean after positive tone photoresist lithography. Therefore, no further tests were performed.

A detailed overview of all tested plasma cleaning variations and the staggered time durations are shown in Table 3. The plasma cleaning procedures of tool A and tool B had no significant impact on the photoresist opening shape in terms of heat induced deformation. In addition to the microscopy and shear test investigation, an impact on the Cu seed-layer in terms of thickness loss or corrosion was examined. Therefore, one LN wafer with seed-layer but without photoresist was exposed to each plasma cleaning procedures. The corresponding Cu layer thickness was investigated via micro x-ray fluorescence at 5 defined positions prior and after the plasma cleaning procedure. None of the plasma cleaning procedures had an impact on the seed-layer thickness of approx. 200 nm Cu. The standard deviation over all measurements was 1.1 nm. At some areas a slight color change of the Cu surface was noticeable, which was caused by oxidation. However, these oxides were removed by a 10 s dip into the electroplating activation bath, which mainly consists of diluted sulfuric acid.

The results of the shear tests are shown in Fig. 25. In this graph each plotted box corresponds to one plasma cleaning process, which is indicated at the vertical axis. The line inside the box represents the median value of all measured maximum shear forces of one plasma process. Additionally, the median value is written next to each box. The box size represents both inner quartiles. The two whiskers attached to the box represent the range of each of the two outer quartiles. One quartile contains 25 % of the total measurement values of one sample. The sheared off Cu post diameter can be considered equal for all samples. Therefore, the absolute values of the shear force can be compared. Not only the maximum shear force was evaluated but also the failure mode was assessed. Three different failure modes were detected. One directly and only at the interface between electroplated Cu and the Cu seed-layer, as shown in the red framed micrograph of Fig. 25. This “red” failure mode proofs a poor adhesion at the Cu-Cu interface. Another failure mode was a combination of the shear off at the interface of the electroplated Cu and the Cu seed-layer, and a shearing through the bulk Cu material as shown in the yellow framed micrograph in Fig. 25. This “yellow” failure mode is critical related to the Cu-Cu interface even if shear forces are high. The

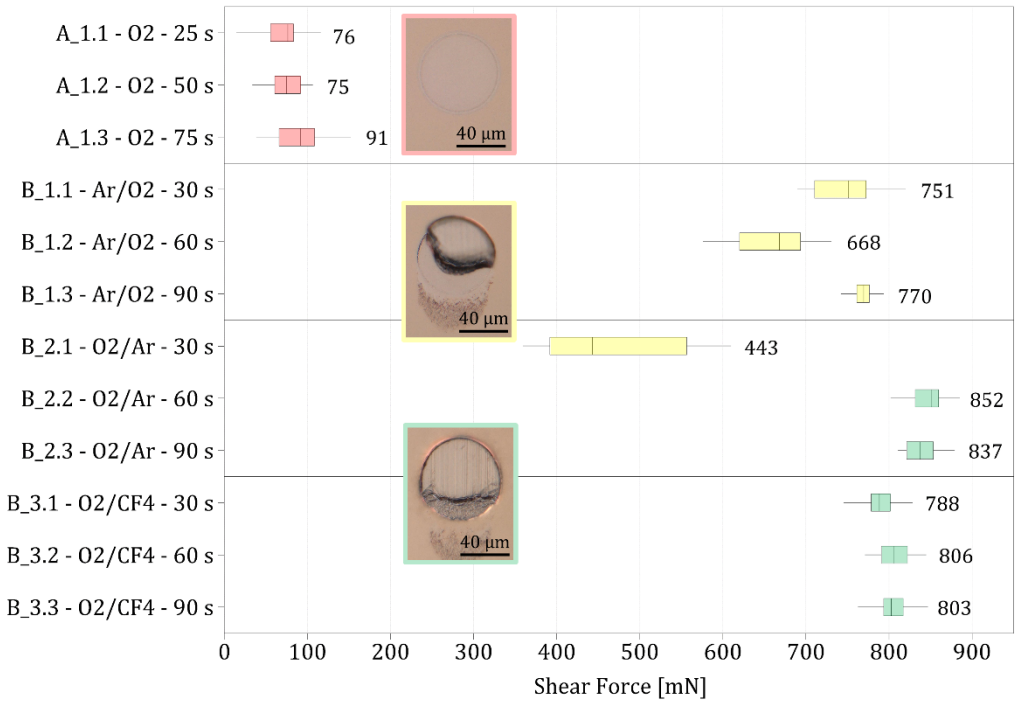


Fig. 25. Box plot of maximum shear force vs. plasma cleaning process. Shear testing through 65 µm diameter Cu posts. The three top view micrographs after shear testing illustrate the three different failure modes. Fracture at the Cu-Cu interface of the seed-layer and the electroplated Cu is framed red. The yellow framed micrograph shows the combination of a fracture at the interface and through the bulk material. The green framed failure mode shows the shear off only through the bulk Cu material. The line in each box and the written number represents the median value of the maximum shear force of the whole sample. The two inner quartiles of all values from one sample are characterized by the box. The whiskers attached to the box show the outer quartiles of the values. One quartile equals 25 % of the measured values. The color of the boxes indicates the detected failure modes for each plasma process tested.

last failure mode was a shearing only through the bulk Cu material and is shown in the green framed micrograph of Fig. 25. This "green" failure mode proves an excellent adhesion at the Cu-Cu interface and the sufficient removal of photoresist residues prior electroplating.

The plasma cleaning processes A_1.1 – O2, A_1.2 – O2, A_1.3 – O2 of tool A resulted in very low shear forces and a failure mode only at the Cu-Cu interface, proofing an insufficient plasma clean. The plasma cleaning processes B_1.1 - Ar/O2, B_1.2 - Ar/O2, B_1.3 - Ar/O2, and B_2.1 – O2/Ar showed the yellow failure mode, i.e a mixture of Cu-Cu interface fracture and through the bulk Cu material. However, the shear forces do vary occasionally pronounced. This indicates an unreliable plasma

cleaning process. Further the partial fracture at the Cu-Cu interface shows an insufficient removal of photoresist contaminations on the seed-layer surface. Nonetheless, the increased plasma duration time for B_2.2 – O2/Ar and B_2.3 – O2/Ar lead to an increased and a narrowly distributed shear force. Both plasma procedures showed only the "green" failure mode, i.e. only sheared through the bulk Cu. These results proof a reliable and proper plasma cleaning step. Likewise, the plasma cleaning processes B_3.1 – O2/CF4, B_3.2 – O2/CF4, and B_3.3 – O2/CF4 show narrowly distributed and high shear forces with only the green failure mode, i.e. sheared through the bulk Cu. Even with a short process time of only 30 s the plasma cleaning process B_3.1 – O2/CF4 shows suitable residue removal from the bottom of the photoresist openings.

The shear tests clearly revealed the importance of a proper plasma cleaning process after lithography to ensure an impeccable adhesion of the electroplated Cu base and the Cu seed-layer. The sufficient adhesion is crucial for the mechanical connection of the CPB to the EP-layer. Poor adhesion at the Cu-Cu interface carries the high risk of reliability issues like delamination of the CPBs. Therefore, the plasma cleaning process on tool B with a gas composition of O_2/CF_4, an IC power of 500 W, a CC power of 50 W, the active wafer cooling at 16 °C, and a time duration of 45 s was chosen as standard plasma clean for CPB manufacturing. The duration of 45 s is between B_3.1 – O2/CF4, and B_3.2 – O2/CF4 to ensure a reliable process window.

2.5 Electroplating

Electroplating or electrochemical metal deposition is a processing method widely used in various industries. The process deposits metal layers from a liquid solution onto electrical conducting surfaces. In this work the metal layer stack of CPBs is manufactured by electroplating. First the Cu base, then the Ni diffusion barrier, followed by the Sn-Ag solder is electroplated on the seed-layer. Due to photolithography, the electroplating takes place only inside the structured photoresist openings, as shown in Fig. 26.

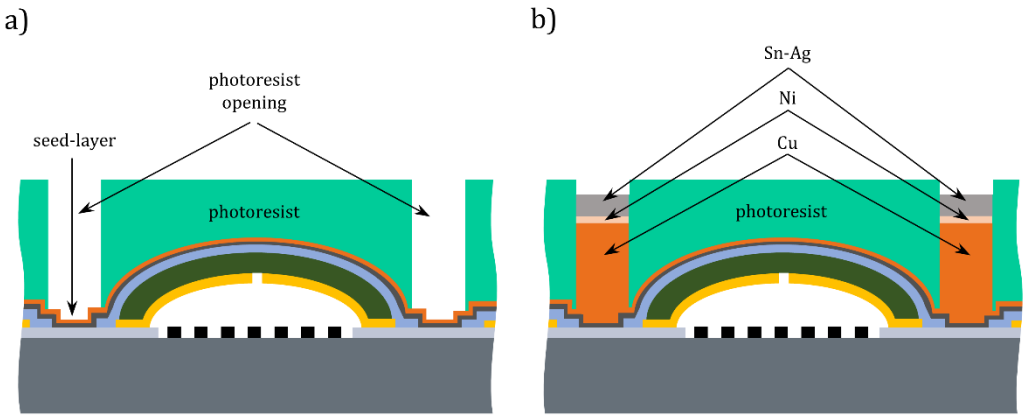


Fig. 26. Schematic cross-section of metal deposition by electroplating. Seedlayer is used as cathode to allow electroplating inside the photoresist openings as shown in a). In b) the metal layer stack resulting from consecutive electroplating steps of Cu, Ni, and Sn-Ag inside the photoresist openings.

For electroplating a liquid electrolyte, containing positive ions of the metal, which is intended to be deposited, and two electrodes (anode and cathode) under electric voltage inside the electrolyte are needed. The intended metal is deposited on the cathode, which in this case is the open seed-layer defined by the lithography. The applied electric voltage between the two electrodes must create an excess of electrons at the cathode and a lack of electrons at the anode. Due to the ions in the electrolyte and the applied voltage, an electrical current flows, i.e. electrons are transferred. This electron transfer is defined as chemical reduction reaction and chemical oxidation reaction. If an atom or molecule gains one or more electrons, the oxidation number is reduced, i.e. a chemical reduction reaction took place. In contrast, if an atom or molecule emits one or more electrons, the oxidation number is increased, i.e. a chemical oxidation reaction took place. Therefore, at the anode (lack of electrons) a chemical oxidation (electron loss at atom/molecule) takes place and at the cathode (excess of electrons) a chemical reduction (electron gain at atom/molecule) takes place, which is enforced by the applied electrical voltage. Oxidation and reduction take place at the same time. In Fig. 27 the electroplating of Cu using a Cu anode in a sulfuric acid copper electrolyte is schematically shown. The applied voltage oxidizes Cu at the anode into fresh Cu^{2+} ions which are dissolved into the acidic electrolyte. At the same time, Cu^{2+} ions are reduced back to elemental Cu by receiving two electrons,

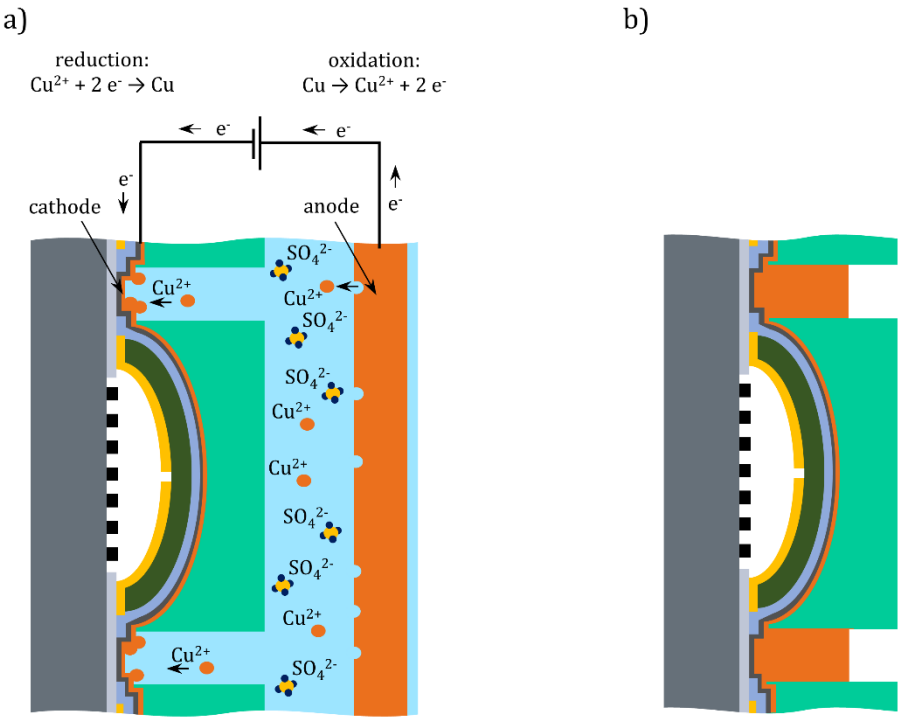


Fig. 27. Schematic cross-section of Cu electroplating. In a) the electroplating of copper in a sulfuric acid-based electrolyte is shown. The applied voltage to the cathode and anode enforces the chemical reduction and oxidation reaction of Cu. The lack of electrons at the Cu anode results in a dissolution of the elemental Cu to Cu^{2+} ions into the electrolyte. At the same time, the excess of electrons at the cathode (seed-layer in photoresist openings) leads to a Cu deposition starting on the seed-layer by the reduction of the Cu^{2+} ions to elemental Cu. The process is performed until the aimed metal thickness is reached as schematically shown in b).

building up the CPB Cu base at the cathode. This process is performed until the required metal thickness is achieved. A special wafer holder seals the wafer from the electrolyte except the front side. The seed-layer is electrically connected at the very wafer edge by metal contacts in the sealing ring of the wafer holder. The front side edge area of the wafer is also structured by lithography and therefore free of photoresist but following the sealing ring geometry. This allows the sealing ring in the wafer holder to electrically connect to the seed-layer and additionally seal the wafer edge and the backside against the electrolyte. Only the photoresist openings on the front side of the wafer are exposed to the electrolyte. Hence, only the openings are filled up by deposited metal from the seed-layer towards the top of the photoresist.

Directly prior electroplating, the wafers are exposed in a batch process 55 s to a soft oxygen plasma. The plasma ensures same surface conditions, hence same wettability of the electrolyte for each wafer, which is important especially for small photoresist openings. Without the plasma step and in case of a hydrophobic surface, small resist openings might not be filled with the electrolyte causing missing pillars.

For electroplating a fully automated commercial tool was used. The plating tool includes different electrolyte, activation, rinse, and spray containers. The wafers are automatically placed in double sided wafer holders, which can hold two wafers. The wafer edge and the back side is isolated from the electrolyte by the wafer holder and its sealing ring. Electrical contacts inside the whole sealing ring ensure a good electrical connection to the seed-layer at the edge of the wafer. The first step in the electroplating tool is the wetting with deionized water with spray nozzles. Optimal resist opening filling or wetting with deionized water is ensured by the hydrophilic surface (oxygen plasma), the water jet from the spray nozzles, and a wafer movement during deionized water spray. The wafer is then handled 30 s into the activation bath. The activation bath contains approx. 10 w% sulfuric acid and removes contaminations and naturally grown copper oxides from the seed-layer surface. The wafers are then handled to the Cu electroplating bath, electroplating the approx. 47 µm height CPB Cu base onto the bright Cu seed-layer surface. The wafers are rinsed with deionized water and handled into the Ni electroplating container, depositing approx. 3 µm Ni directly on the CPB Cu base. After another water rinse, the wafers are brought to the Sn-Ag electroplating container and approx. 20 µm Sn-Ag with an Ag concentration of approx. 3 w% is electroplated directly onto the Ni layer. After Sn-Ag deposition the wafers are rinsed with deionized water and dried by an air stream. The electroplating was performed with commercially available electrolytes. Electrolyte quality was monitored by frequent bath analysis according to supplier requirements.

Cu electroplating was done with an acidic copper sulphate bath containing additives like brightener (Cu deposition accelerator), carrier (Cu deposition suppressor), and leveler (Cu deposition suppressor). The additives allow a stable bath and uniform Cu deposition rates on the wafer. Two different anodes were tested for

Cu electroplating. First an inert platinum anode was used for electroplating. The platinum does not chemically react during electroplating; hence an additional Cu source is provided by copper pellets in a separate tank. The Cu pellets can be flushed with electrolyte if the Cu^{2+} ion concentration gets to low, due to the already deposited Cu from the electrolyte. However, to dissolve the Cu into the electrolyte an Fe^{2+}/Fe^{3+} redox (reduction and oxidation) mediator is added into the electrolyte. If the iron (Fe) redox mediator gets in contact with Cu without applying electrical voltage, the Fe^{3+} ions reduce their oxidation state by receiving electrons from the Cu. Hence, Fe^{3+} ions get reduced to Fe^{2+} ions and at the same time elemental Cu is oxidized to Cu^{2+} ions, which dissolve into the electrolyte. However, the Fe^{2+}/Fe^{3+} redox mediator also dissolves the Cu from the seed-layer during the wafer holder moves into the Cu electrolyte container. The Cu seed-layer is dissolved within a few seconds, before the actual Cu electroplating starts. Hence, Cu is directly electroplated on the Ti adhesion layer which is underneath the Cu seed-layer. The adhesion of electroplated Cu on Ti is very poor. Some of the copper posts were already partly washed off during photoresist removal. Therefore, the use of inert platinum anodes in combination with an Fe^{2+}/Fe^{3+} redox mediator is not suited for electroplating on very thin Cu seed-layer. In Fig. 28 the attacked Cu seed-layer can be seen after Cu electroplating and photoresist removal when using a redox mediator.

By using pure Cu as anode material instead of platinum and omitting the Fe^{2+}/Fe^{3+} redox mediator, the dissolution of the Cu seed-layer was prevented. Therefore, the

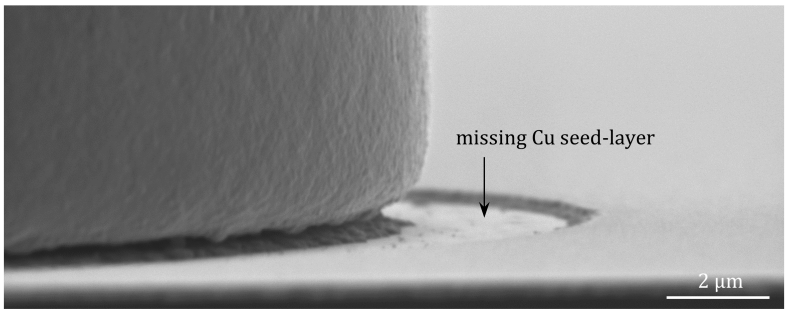


Fig. 28. SEM image showing a part of the CPB Cu base on the substrate after electroplating and photoresist removal but prior seed-layer removal. The 200 nm thick seed-layer is missing next to the CPB. The seed-layer is etched below the photoresist from the Fe^{2+}/Fe^{3+} redox mediator if electroplating with an inert anode.

electrolyte and the anode were changed in the electroplating tool. The use of a Cu anode allowed electroplating of Cu with excellent adhesion on the Cu seed-layer surface. Even small photoresist openings with a diameter of approx. 15 µm were filled with Cu. As stated in Table 4, a Cu deposition rate of 2.0 µm/min was achieved using a current density of 10 A/dm^2 and fast bath agitation. Total electroplating duration for 47 µm Cu was 23.5 minutes. However, even higher Cu electroplating rates are feasible by using > 15 A/dm^2.

Table 4. CPB electroplating process parameters.

Material	Current Density [A/dm^2]	Deposition Rate [µm/min]	Bath Temp. [°C]	Agitation
Cu	10	2.0	25	fast
Ni	4	0.8	50	fast
Sn-Ag	5	2.4	25	medium

The Ni electroplating bath is based on a boric acid solution with a Ni anode. Directly after Cu plating and the water rinse, the Ni is electroplated on the fresh Cu. The Ni electroplating runs, comparable to Cu electroplating, under an applied voltage. Dissolved Ni^{2+} ions are reduced to elemental Ni when receiving two electrons. At the same time the Ni atoms from the anode are oxidized to Ni^{2+} ions and are dissolved into the electrolyte. Ni acts as diffusion barrier between the Cu and solder, hence prolonging solder joint reliability. Ni was electroplated with 4 A/dm^2 at 50 °C and fast bath agitation. A deposition rate of 0.8 µm/min was achieved. Total electroplating duration for 3 µm Ni was 3.75 minutes.

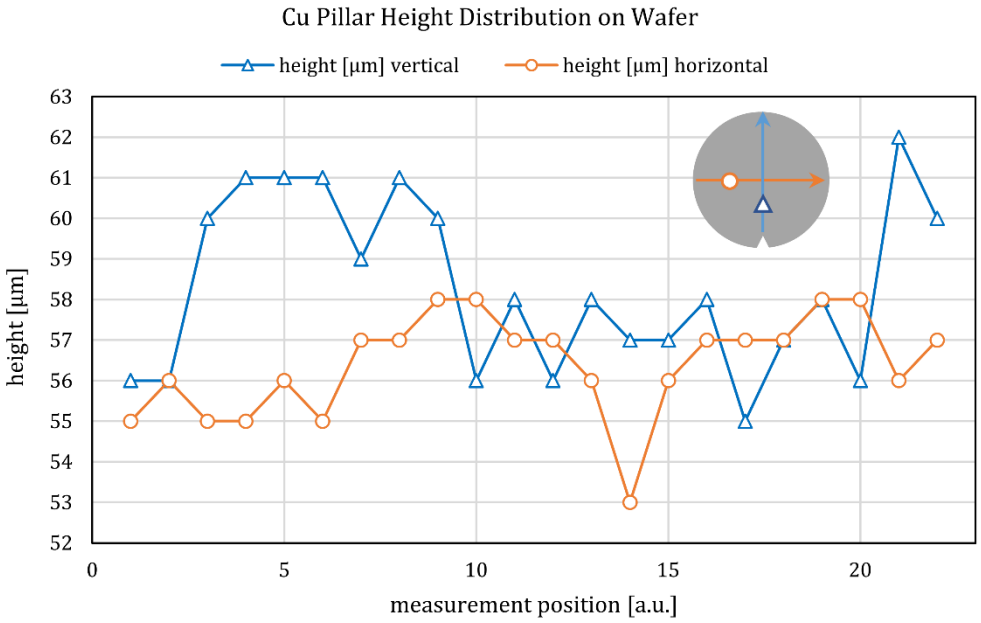
The Sn-Ag bath is based on a methanesulfonic acid solution containing Ag^+ and Sn^{2+} ions with a Sn anode. Directly after Ni plating and a water rinse, the Sn-Ag is electroplated on the fresh Ni. The Sn-Ag acts as the solder material of the CPB and provides the ability for the electrical and mechanical connection of the component to a circuit board. However, having two different metals in a solution, bares the risk of a spontaneous and ongoing redox reaction between both metals. The Ag is more noble than the Sn, i.e. the standard electrode potential of Ag against the standard hydrogen electrode is higher than the one of Sn. As a result, the Ag^+ ions in the electrolyte would

be reduced to elemental Ag by snatching electrons from the less noble Sn. When providing electrons from elemental Sn, an oxidation of the Sn takes place. These reactions would cause the precipitation of silver in the electrolyte, which than cannot be used for electroplating from the solution anymore. Additionally, the Sn anode would be passivated from elemental silver, also stopping the supply of fresh Sn^{2+} ions to the electrolyte during electroplating. To avoid this unwanted chemical reduction of Ag^{+} ions, the electrolyte contains an Ag^{+} ion complexing agent. The complexing agent ensures that the Ag^{+} is stabilized in a complex, i.e. it is not available for the unwanted spontaneous chemical reduction reaction. However, when applying a voltage, the metal ions Ag^{+} and Sn^{2+} are reduced to elemental Ag and Sn, hence deposited at the

Table 5. Main ingredients of the commercial Cu, Ni, and Sn-Ag electrolytes used for electroplating. Exact additive components and concentrations were not available (n.a.).

Electrolyte	Main Ingredients	Concentration
Cu	Cu	33-37 g/L
	sulfuric acid	165-195 g/L
	chloride	45-55 mg/L
	additives	n.a.
Ni	Ni	65-75 g/L
	boric acid	35-45 g/L
	additives	n.a.
Sn-Ag	Sn	40-50 g/L
	methanesulfonic acid	85-115 g/L
	Ag	0.9-1.1 g/L
	complexing agent	n.a.
	surfactant	n.a.

cathode. Fresh Sn^{2+} ions are provided from the Sn anode. The silver must be regularly re-dosed to the bath with a liquid Ag containing solution. Although, Sn and Ag are electroplated at the same time, no real alloy is electroplated. Both metals create individual metal crystals. The Sn-Ag alloy is formed during the reflow (heating above melting point followed by cool down) of the Sn-Ag solder. The Ag content in the electroplated metal mix depends mainly on the Ag content in the electrolyte (the higher the more Ag), the electroplating current density (the higher the less Ag), and the agitation of the bath (the higher the more Ag).



$$\text{uniformity within wafer (WIW)} = \pm \frac{h_{max} - h_{min}}{2 \times \frac{1}{n}\left(\sum_{i=1}^{n} x_i\right)} \times 100\ \% = \pm 8\ \%$$

Fig. 29. Graph showing Cu pillar height vs. position on one wafer. The height is related to Cu only and measured via focus with a micrometer scale of an optical microscope. Blue indicates the evenly distributed 22 measurement positions from wafer flat to anti-flat. Orange indicates the evenly distributed 22 measurement points from left to right of the wafer as illustrated on the schematic wafer top view. Further the result and the formula for the approx. within wafer Cu height uniformity is shown. The Cu height does not represent the targeted CPB Cu base height.

The summarized electroplating process parameters can be found in Table 4 and the corresponding main ingredients of Cu, Ni, and Sn-Ag electrolytes can be found in Table 5.

One important feature of electroplating is the height uniformity within the whole wafer and within one die. At the time of investigation, no suitable measurement tool was available for setting up an automated measurement of CPB height after plating. Therefore, only the height of plated Cu pillars was measured using the focus with a micrometer scale of an optical microscope. The accuracy of the measurement is estimated to be ± 1 µm. However, it gives a approx. value of ± 8 % uniformity within the wafer for Cu electroplating as shown in Fig. 29. The uniformity within one die, i.e. the Cu pillar height variation in the die area of 1.2 x 1.6 mm^2 was measured to be less than 1 µm absolute, which equals less than ± 2 %. Later measurements on different

a) b)

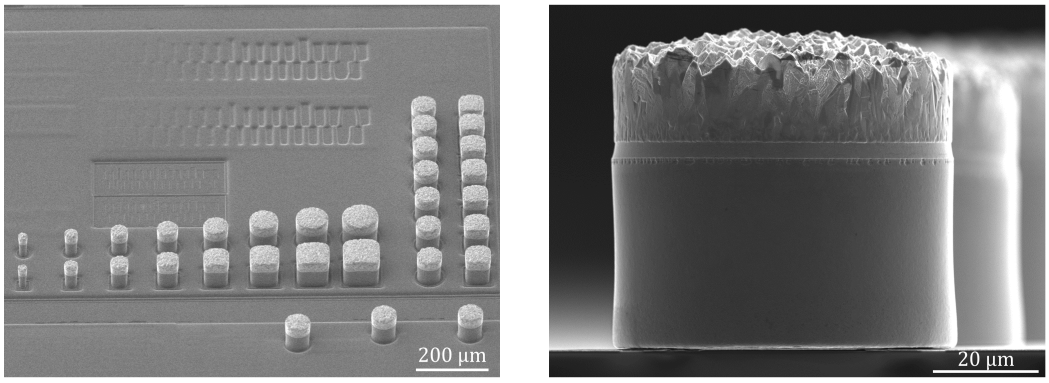


Fig. 30. SEM images of electroplated CPBs with the metal layer stack Cu, Ni, and Sn-Ag after photoresist removal. In a) a test die with varying CPB diameters and shapes. In b) one CPB with clearly visible Sn grain structure.

designs had shown, that the fully processed CPB (Cu, Ni, Sn-Ag) including the reflow showed similar uniformity results.

Energy dispersive X-ray (EDX) and X-ray fluorescence (XRF) spectroscopy had confirmed the aimed Ag content of approx. 3 w% with an absolute wafer to wafer fluctuation of less than ± 1 w% and a within wafer fluctuation of less than ± 0.5 w%. However, there was no exact investigation of the Ag content fluctuation because the performed tests were in accordance with the galvanic electrolytes manufacturer data and no automated test was available.

Still, electroplating of Cu, Ni, and Sn-Ag was successfully performed by a fully automated commercial tool and commercial electrolytes, as shown in Fig. 30. Reliable electroplating results with a sufficient uniformity within wafer and within die were achieved.

2.6 Photoresist Removal

The positive and negative photoresists were removed after electroplating metal deposition by a spray batch process, as schematically displayed in Fig. 31. The chamber of the commercial tool can hold up to 50 wafers at once. A commercial

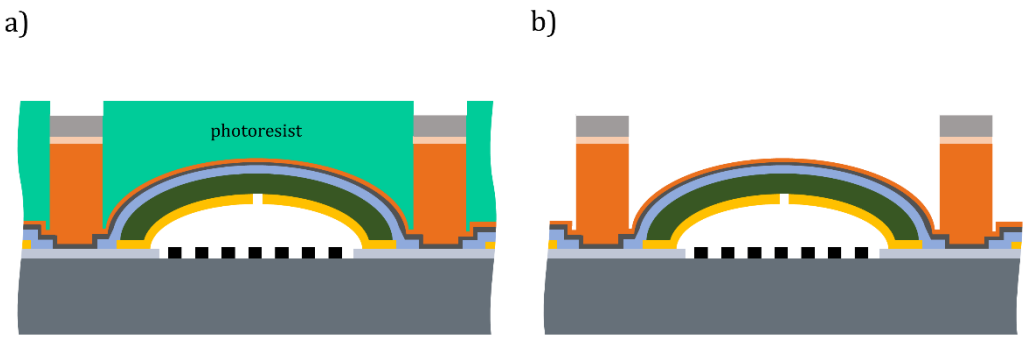


Fig. 31. Schematic cross-sectional image of photoresist removal. In a) the photoresist after electroplating process is removed by spray-batch process resulting in stand-alone CPBs on TFAPs in b).

stripper medium ensures the total dissolution of the photoresist on the wafers. The stripper medium consists of mainly water, DMSO (dimethyl sulfoxide), and TMHA (tetramethylammonium hydroxide). The dissolution process is accelerated by using an enhanced temperature of around 60 °C. After the photoresist strip the wafers are rinsed with deionized water and dried with a hot nitrogen stream in the chamber. The wafers are held in a carrier. However, the carrier rotates during the whole process to ensure a faster and uniform dissolution, rinse, and drying procedure. The whole process takes about 45 minutes and does not significantly attack or influence the present materials. The removal process step time was chosen rather long because the same recipe was used for the negative and the positive tone resist. Negative tone resists are usually strongly chemically crosslinked and hence harder to remove. The stripper medium was renewed according to manufacturer recommendation. No visible resist residues were detected for all processed wafers.

2.7 Seed-Layer Etch

The seed-layer metal stack of 50 nm Ti and 200 nm Cu was initially deposited to provide a base and an electrically conducting layer from wafer edge to the photoresist openings for the electroplating metal deposition. However, the seed-layer still electrically connects all electroplated metal layer stacks (Cu/Ni/Sn-Ag) and therefore needs to be removed. The seed-layer is removed after the resist removal. To keep

process times and costs low a wet batch spray process in a commercial tool was developed. Usually 12 (or up to 24) wafers are fixed in a rotating carrier. The etch process can be separated in three steps. First, the Cu etch by an aqueous solution of potassium iodide (KI) and iodine (I_2). Second, the removal of copper iodide (CuI) from the copper surface by an aqueous ammonia solution. The copper iodide is created during the first step and would hinder the Ti etch. The third and last step is the Ti etch by an aqueous ammonium bifluoride solution. After every step an intense deionized water rinse step was performed to avoid chemical residues on the wafers.

The approximate etch rates were determined for different etchant concentrations in preliminary experiments. The experiments were performed simply in a beaker with a stirrer. The preliminary experiments were kept very simple on purpose, because the wet spray process is strongly influenced by the tool architecture and the set parameters of the tool. However, it allowed to get an idea of the etch rates and the corresponding times dependent on the etchant concentration. The thin metal films require relatively slow etch rates for a reliable etch process to be developed. Therefore, the etchant concentrations were set in a range, where the etch process time was in a good compromise of etch speed and controllability. That means, e.g., that the process step times are long enough to allow most of the etchant solution to flow back into the etchant container from the etch chamber, prior water rinse, without over-etching the metals or to worsen etch rate uniformity. By adjusting the rotational speed of the wafer carrier and the etchant spray flow, a uniform etch result

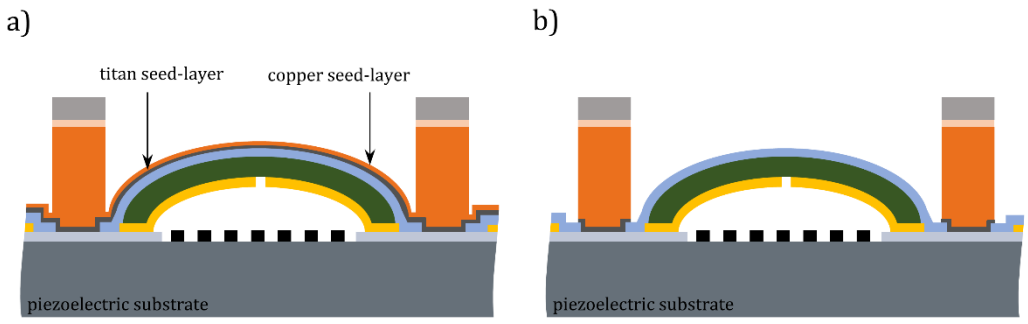


Fig. 32. Schematic cross-sectional image of seed-layer etch. In a) first the copper is etched followed by titan etching. In b) the CPBs on TFAPs are electrically separated from each other as the seed-layer is removed.

for both metal layers were achieved on structured wafers with TFAP topology. Table 6 shows the corresponding etch duration times used for each process step and the etchant concentration. The etch rates related to the tool, do correspond to structured wafers with a TFAP and CPBs.

Table 6. Parameters of the seed-layer etch process including etchant concentrations and approx. etch rates of the seed layer on structured wafers.

	Aqueous etchant concentration	Etch rate	Etch duration	Rotational speed
Cu-Etch	KI 4.4 g/L * I_2 3.2 g/L *	approx. 5 nm/s	50 s	15 rpm
CuI	NH_3 3.0 g/L	unknown	60 s	30 rpm
Ti-Etch	NH_4HF_2 2.85 mg/L	approx. 1.5 nm/s	50 s	15 rpm

* Etchant concentration estimated due to dilution of commercial product

In Fig. 33, SEM images of one CPB at the wafer edge and another CPB at the wafer center is shown prior and after the seed-layer etch. The CPB base is made of Cu, hence it is also attacked by the Cu etchant. A Cu loss at the base of only 0.7 µm was detected for the wafer edge and the wafer center. Obviously, the lost Cu thickness at the CPB base is higher than the thickness of the actual Cu seed-layer thickness. This is caused by a slight over-etch to ensure the removal of the whole Cu seed-layer even in topology areas with lower agitation, and therefore with lower etch rates. Further, the sputtered Cu seed-layer shows a different crystalline structure compared to the electroplated Cu, which additionally induces lower etch rates for the sputtered Cu seed-layer.

The Ti layer is etched subsequently after the Cu etch. During the Ti etch process the thin Ti layer below the CPB Cu base is also attacked by the Ti etchant. Unfortunately, the etch rate is highly accelerated for the Ti sandwiched between CPB Cu base and the reinforcement. This causes an under-etch and if it is too pronounced, mechanical reliability issues can occur. Therefore, the Ti under-etch was investigated

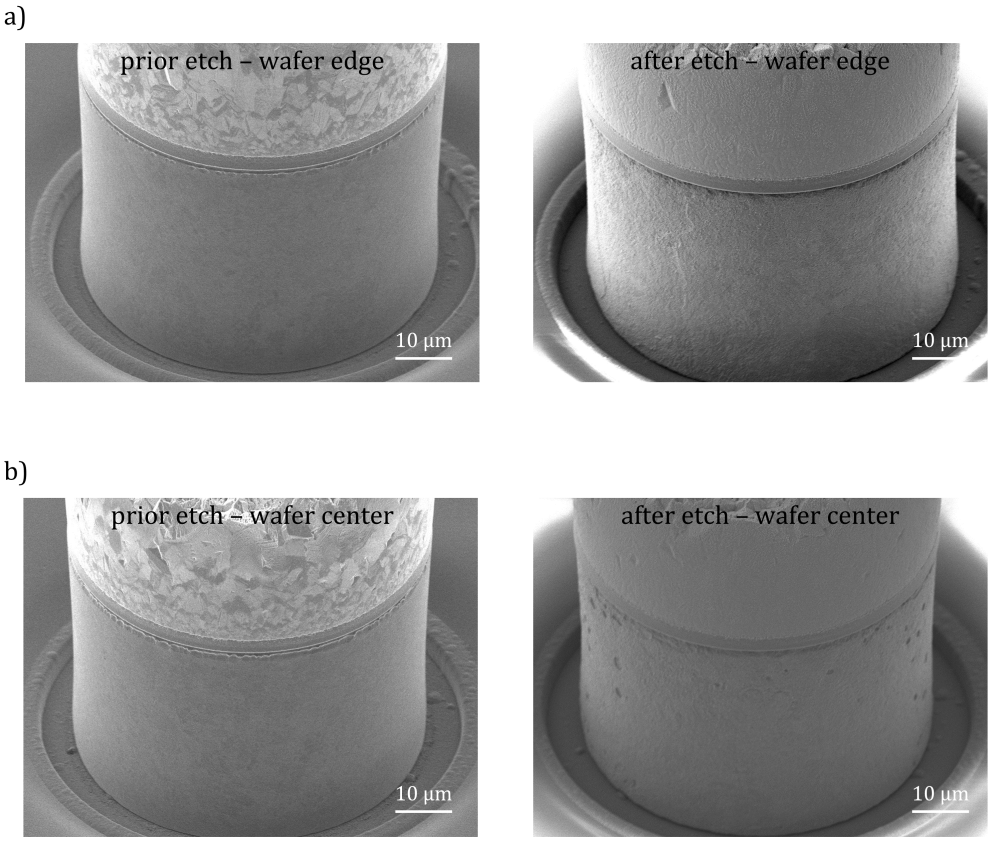


Fig. 33. SEM images of one CPB each at the wafer edge and the wafer center. In a) the left SEM image shows a CPB prior the seed-layer etch at the wafer edge. The right SEM image in a) shows the exact same CPB as in the left image of a) but after the seed-layer etch of Cu and Ti. The two images in b) show the same as in a) but for a different CPB in the wafer center. For SEM images after etch process no thin film of Pt or Au were sputtered to enhance electrical conductivity during SEM imaging. Therefore, SEM image details appear different.

by a FIB cut through the whole CPB after seed-layer etch as shown in Fig. 34. The overlap between the CPB base and the TFAP reinforcement layer must be large enough to prevent that the under-etch reaches the TFAP electrical path layer. If the Ti under-etch would reach the TFAP electrical path layer, the small 50 nm gap would weaken the mechanical connection of the CPB to the TFAP. Furthermore, there would be a serious risk of corrosion of the Al induced by etch chemical residues trapped in the gap and by later penetrated humidity. The FIB cut investigation on two different positions showed a maximum Ti under-etch of approx. 1.5 µm. The etch progress in the gap is much further advanced compared to the determined etch rate of Ti on the bare surface. The reason of a higher Ti etch rate inside the gap is not fully understood,

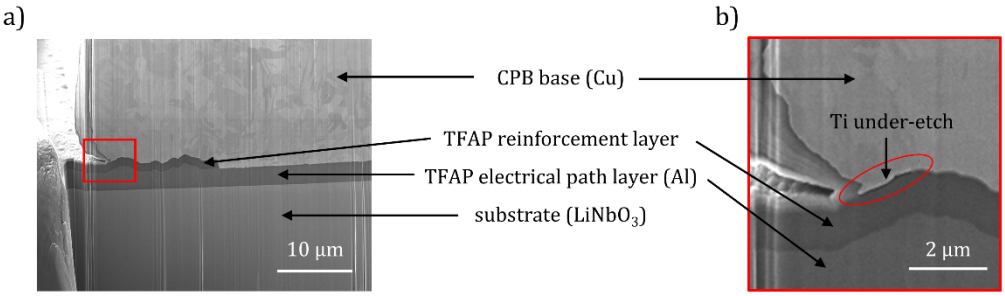


Fig. 34. SEM images of a FIB cut through the left part of the CPB base and some TFAP layers after seed-layer etch process to determine Ti under-etch. In a) the left part of the perpendicular FIB cut through the CPB and the TFAP is shown. The CPB base, TFAP reinforcement layer, TFAP electrical path layer, and the substrate are visible in a cross-sectional view. The red frame in a) is displayed magnified in b). In b) the under-etch of the 50 nm thick Ti is visible with approx. 1.5 µm length. The additional layers at the side of the CPB Cu base and the TFAP reinforcement layer are artifacts and emerge by material redeposition during the FIB cut process.

but the physical contact of Ti to Cu might play a role, increasing speed of the chemical etch reaction. Additionally, a longer etch time of the Ti inside the gap can be expected, due to the poorer accessibility of deionized water during the rinse step. However, the detected Ti under-etch is uncritical for the chosen overlap between the CPB base and the TFAP reinforcement layer. The developed Cu and Ti etch processes are suitable and do neither attack significantly the other metals (Ni, Sn-Ag) present nor the TFAP.

2.8 Sn-Ag Cap Reflow

Initially the electroplated Sn-Ag has a cylindrical shape with large grains as shown in Fig. 36 a). After electroplating the Sn-Ag is not a true alloy, as each material may appear in separated crystals. To achieve a uniform shape with a small surface to volume ratio and a true homogeneous alloy, a reflow needs to be performed. During the reflow, the whole wafer is heated above the liquidus temperature of the Sn-Ag alloy and subsequently cooled down. The surface tension of the molten Sn-Ag forces the liquid material into a spherical shape as schematically shown in Fig. 35. The Ag content in the electro-plated Sn-Ag solder was aimed to be approx. 3 w%, which is close to the eutectic composition of 3.5 w% Ag and 96.5 w% Sn. The eutectic composition of Sn-Ag has a melting temperature of 221 °C. EDX and XRF spectroscopy had confirmed an Ag content of approx. 3 w% with an absolute wafer-to-wafer

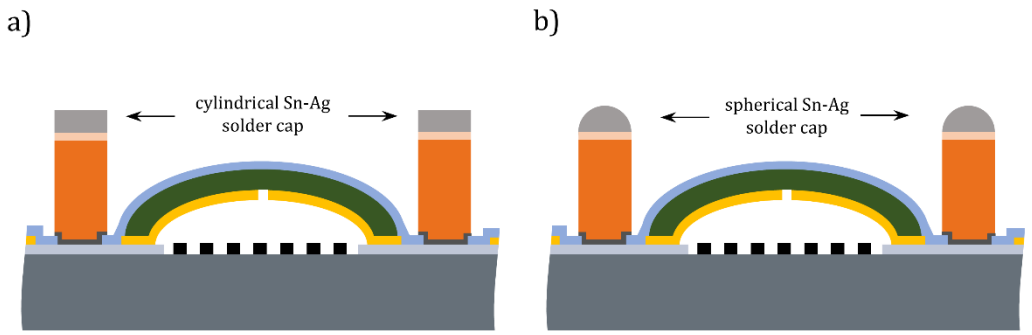


Fig. 35. Schematic cross-sectional image of CPB solder cap reflow. In a) the Sn-Ag solder material has a cylindrical shape after the electro-plating. Heating the whole wafer above the liquidus temperature of the Sn-Ag and removing the tin oxides on the solder surface by e.g. flux, results in spherical Sn-Ag caps shown in b).

fluctuation of less than ± 1 w% and within wafer less than ± 0.5 w%. The melting temperature of the electro-plated Sn-Ag solder is, according to the Sn-Ag phase diagram, in the range of 221 °C to 226 °C. [45]

However, naturally grown tin oxides on the Sn-Ag solder surface, which are formed after electro-plating deposition, have a much higher melting point compared to pure Sn-Ag. During the liquidous time of Sn-Ag, these unmolten tin oxides float on

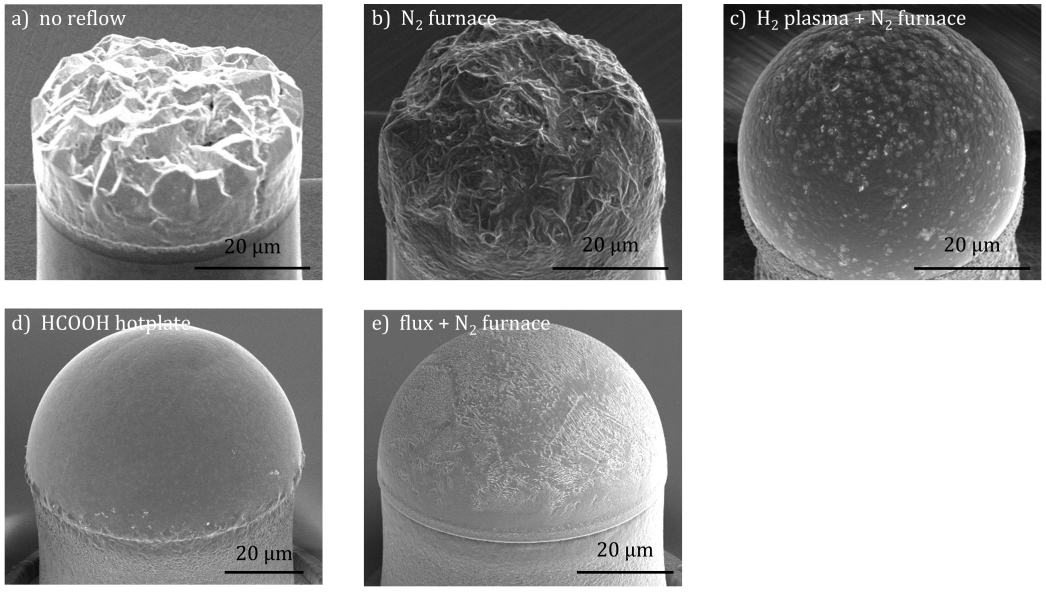


Fig. 36. SEM images of Sn-Ag solder of CPBs prior and after different solder reflow processes. In a) the electro-plated Sn-Ag of a CPB prior reflow is shown and can be considered as the reference. Reflow results after b) N_2 furnace, c) H_2 plasma pretreatment followed by N_2 furnace, d) hotplate with formic acid atmosphere and e) flux application followed by N_2 furnace and flux clean are shown. Peak reflow temperature for the results shown was 250 °C.

the surface of the molten solder material. Unfortunately, the tin oxides disturb the spherical shape formation and additionally in the later component assembly the tin oxides hinder the soldering of the CPBs to the landing pads of the module substrates. Hence, tin oxides must be removed prior or during the actual reflow process. In this study the reflow is performed at wafer level after the seed-layer etch and prior the wafer singularization.

In total four different wafer-level reflow processes were tested and the corresponding reflow results are shown in Fig. 36. First, a simple convection reflow in a continuous furnace under N_2 (nitrogen) atmosphere was performed, which can be considered as the reference to the other three processes. Generally, the N_2 gas is known to be chemically unreactive under the given reflow conditions. This prevents further accelerated tin oxide growth during the reflow process. The second procedure was done the same as the first, but with an additional H_2 (hydrogen) gas containing plasma pretreatment shortly prior the continuous furnace. The H_2 gas containing plasma creates a strong chemically reducing environment, i.e. it has the potential to chemically reduce tin oxides back to pure elemental Sn. A plasma cleaning tool which creates a direct current plasma stream via a hot filament was used. The third procedure was a reflow process on a hotplate under formic acid (HCOOH) atmosphere. Formic acid atmosphere has a very strong chemically reducing potential at increased temperatures. The fourth reflow procedure was again in a continuous furnace with multiple temperature zones but with flux application on the whole wafer prior reflow. Flux is the most common in industry when performing Sn based soldering. It cuts through the tin oxides, flushes them away and partly reduces them back to elemental Sn in the heat-up zone of the continuous furnace. A commercial standard activated rosin-based flux was used and washed off directly after the reflow. The possibly corrosive acting flux residues must be removed. Therefore, a standard water-based commercial flux cleaning agent in a wafer cleaning tool was used. The flux cleaning procedure did not attack the present metals nor the TFAP. The main process parameters of the convection reflow in the continuous furnace and the reflow in the formic acid chamber are listed in Table 7 and Table 8, respectively. Reflow profiles were adapted from the IPC/JEDEC J-STD-020F standard.

Table 7. Main steps of continuous furnace convection reflow profile with related parameters.

Continuous Furnace Convection Reflow Profile		
Step	**Reflow Profile Feature**	**Parameters**
1	atmosphere	total process flushed with N_2 gas
2	preheat	$T_{preheat1}$: 25 °C to 150 °C $t_{preheat1}$: variable to reach T_{peak} < 480 s ramp-up $rate_{preheat1}$: max. 3.0 K/s $T_{preheat2}$: 150 °C to 217 °C $t_{preheat2}$: 60 s to 120 s ramp-up $rate_{preheat2}$: 0.6 K/s to 1.1 K/s
3	reflow	$T_{total\ reflow}$ > 217 °C $t_{total\ reflow}$: 60 s to 150 s ramp-up $rate_{total\ reflow}$: max. 3.0 K/s T_{peak}: 250 °C +5/-2 °C t_{peak}: 20 s to 40 s max. duration from 25 °C to reach T_{peak}: 480 s
4	cool down	ramp-down rate: max. 6.0 K/s

Table 8. Main steps of formic acid hotplate reflow profile in a closed chamber with related parameters.

Formic Acid Hotplate Reflow Profile (closed chamber)		
Step	**Reflow Profile Feature**	**Parameters**
1	atmosphere	1) N_2 gas flush 2) N_2 + HCOOH gas flush (starting at 120°C)
2	preheat	$T_{preheat1}$: 25 °C to 150 °C $t_{preheat1}$: variable to reach T_{peak} < 480 s ramp-up $rate_{preheat1}$: max. 3.0 K/s $T_{preheat2}$: 150 °C to 217 °C $t_{preheat2}$: 60 s to 120 s ramp-up $rate_{preheat2}$: 0.6 K/s to 1.1 K/s
3	reflow	$T_{total\ reflow}$ > 217 °C $t_{total\ reflow}$: 60 s to 150 s ramp-up $rate_{total\ reflow}$: max. 3.0 K/s T_{peak}: 250 °C +5/-2 °C t_{peak}: 20 s to 40 s max. duration from 25 °C to reach T_{peak}: 480 s
4	atmosphere	N_2 gas flush starting at 230 °C
5	cool down	ramp-down rate: max. 6.0 K/s

In summary one can see that the reflow only in a N_2 flushed continuous furnace is insufficient due to poor spherical solder cap shape and the risk of poor solderability during component assembly caused by the increased amount of tin oxides as shown in Fig. 36 b). H_2 plasma pretreatment, formic acid atmosphere and the use of flux show

all sufficient reflow results, i.e. well spherical formed Sn-Ag solder caps on the CPB copper base without visible defects as shown in Fig. 36 c), d), and e). The H_2 plasma pretreatment has the drawback to be time consuming due to single wafer processing and high tool costs. Additionally, it involves the risk of a repetitive tin oxide formation degrading the reflow result influenced by the time span between the pretreatment and the reflow, and environmental conditions. The reflow under formic acid atmosphere requires also special tools and precautions due to the toxicity of formic acid but gives very good reflow results related to the Sn-Ag cap surface and shape. However, the formic acid reflow favors the CPB Cu base sidewall solder wetting by Sn-Ag surface diffusion, i.e. the solder moves from the solder cap slowly down at the Cu base surface. This behavior was observed to sometimes cause a partial or a total collapse of the Sn-Ag solder cap with the chosen tool and process parameters. Furthermore, a uniform heat distribution in the specific tool was not achieved. The heat is transferred to the wafer using a standard hotplate with mechanical clamping; however, the non-uniform thermal expansion behavior of the LN material causes a strong bow of the wafer during the reflow process. In many cases this led to non-reflowed Sn-Ag caps at the edge area of the wafers and wafer breakage caused by the mechanical clamping. However, using a different tool might avoid these drawbacks.

Performing the solder reflow in a continuous furnace does not show these drawbacks. Therefore, the flux-based convection reflow in a continuous furnace was assessed to fit best as it is a well-established and an easily controllable industrial

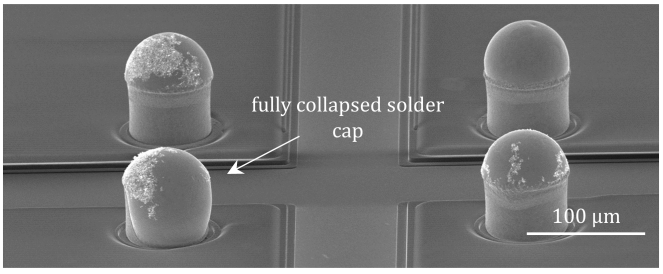


Fig. 37. SEM image of CPBs with a TFAP after solder cap reflow under formic acid atmosphere. Dicing lane can be seen between the 4 TFAP corners. The lower left solder cap collapsed during reflow, hence wetting the CPB Cu base.

process with low acquisition and operating costs resulting in very reliable solder cap reflow results. Additional tests with reflow peak temperatures of 240 °C and 260 °C showed no significantly better results compared to the reflow peak temperature of 250 °C. The flux-based reflow led to excellent reflow results as can be seen in Fig. 36 e).

2.9 Wafer Singularization

Up to here, all manufacturing steps are at wafer-level. During the wafer singularization process, the whole wafer is separated into individual components as the last manufacturing step. A process called DBG (dicing before grinding) ensures singularization of the components even with the brittle LN substrate material. The DBG process consists of topside wafer half-cut dicing, topside laminating into a grinding protection foil, back side grinding, followed by mounting-frame lamination on the grinded back side. The DBG process allows excellent results when separating fragile wafer materials like LN. Compared to processes which grind prior to dicing, DGB avoids the need to handle already thinned LN wafers as the separation is performed during the grinding. Furthermore, the chipping at the dicing edge is significantly reduced compared to dicing after grinding. Chipping is a phenomenon, where parts of the chip edge are lost during dicing. However, this chipping area must be taken into account for the design rules to avoid damage of the package; hence chipping is reducing the total number of components on one wafer.

In the first step of DGB, the wafers are half-cut diced from the top side of the wafer with a fast-rotating thin dicing blade, as illustrated in Fig. 38 a). The half-cut dicing is aligned along the approx. 85 µm broad dicing lanes between the TFAPs on the wafer's topside using a fully automated commercial dicing tool. The dicing grooves reach a depth of approx. 170 µm. The wafer is optically aligned and hold via vacuum on the dicing chuck inside the tool. The topside half-cut dicing is steadily rinsed with water to cool the dicing blade and to flush the dicing particles away. A final water rinse and air-dry ensures that no dicing residues remain on the surface. After half-cut dicing,

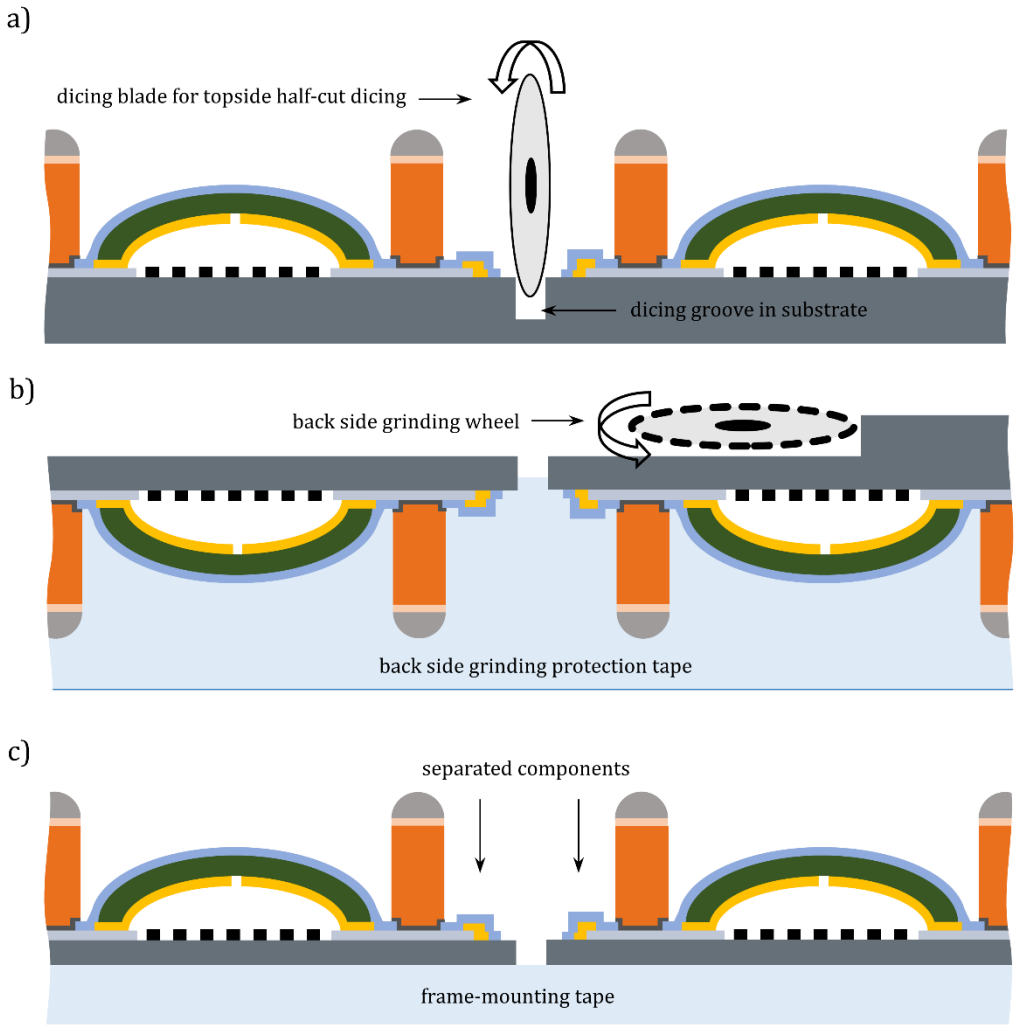


Fig. 38. Schematic cross-sectional image of DBG (dicing before grinding) component separation. In a) the wafer topside is half-cut diced in the dicing lane between the TFAPs. In b) the wafer is then laminated on the topside with a back side grinding protection tape. Then the wafer is thinned by the grinding wheel coming from the back side untill topside grooves are reached. Here wafer seperation starts but singulated components are further thinned until 125 µm LN substrate thickness. The back side grinding protection tape is exposed to UV-light to loose most of its adhesion. Then the already separeted components on the back grinding tape are laminated on the mounting-frame tape and the back side grinding tape is carefully peeled off. In c) the separated components are now easily available for pick up on the also UV-light exposed mounting frame.

the LN wafer with its topside grooves is then laminated into a so-called back side-grinding protection adhesive tape. The tape is rolled over the topside of the wafer embedding the TFAPs and CPBs. This process is performed on a commercial tool with temperature, pressure, and speed adjustment to ensure a good adhesion and an enclosure of the CPBs. The back side-grinding tape protects the TFAP and the CPBs

during back side grinding and it holds the components in place when the grinding wheel hits the grooves, hence separating the wafer in single components. The complete enclosure of CPBs in the tape is important to reduce the resulting mechanical stress induced by the back side grinding. The highest mechanical stress is induced when the component separation begins, as the former unseparated wafer cannot additionally distribute the mechanical load.

For back side grinding, the laminated LN wafer is placed inside a commercial wafer grinding tool with an appropriate grinding wheel for LN substrate and thinned from the back side. The actual wafer separation begins, when the wafer thinning is progressed so far that the back side grinding wheel hits the grooves from half-cut dicing, as shown in Fig. 38 b). Parameters like grinding wheel rotation speed, feed rate, water flow, and target thickness are set accordingly to achieve a uniform LN thickness of 125 µm without losing separated components during final component thinning. The back side grinding protection tape is then exposed to a certain dose of UV-light, which leads to a significant loss of adhesion between tape and separated components.

The grinding tape with the embedded individual components is then transferred as a whole, with the backside of the components on a frame-mounting tape, i.e. a UV-light sensitive tape braced in a metal frame. The still pasted back side grinding protection tape on the top of the individual components is then carefully peeled off in a commercial tool with a defined peel angle and peel speed, leaving the separated components on the mounting-frame tape, as shown in Fig. 38 c). This is possible because the UV-light exposed back side grinding protection tape has now a significant lower adhesion compared to the frame-mounting tape. However, also the frame-mounting tape is exposed to UV-light after grinding tape peeling to weaken the adhesion capability and therefore allowing an easy pick up of single components by a vacuum pipette picking tool.

The grinding tape peeling is a very critical step in terms of physical component damage, as the mechanical impact on the TFAP and on the CPBs is high. Therefore, the separated components and the tapes from DBG were optically investigated, in

addition to the later reliability tests of the assembled components, to ensure that the whole wafer singularization process, which induces serious mechanical stress to the TFAPs and the CPBs, has no negative impact. Each processed wafer had multiple different component designs on it, which also included components suitable for revealing the DBG limitations. This included designs with CPBs very close to the dicing lane, CPBs with very small or even missing reinforcement openings, and varying CPB diameters. CPBs very close to the dicing lane pose the risk, that the back side tape does not fully embed the CPB. This can lead to grinding particle residues on the component's top side and mechanical damage of the CPB due to missing mechanical tape support during grinding.

In Fig. 39 one can see the schematic cross-sectional view, a CPB's SEM image, and the grinding tape with the imprints of the topology after peeling, if the CPB is placed at the outer edge of the TFAP. Having the CPB so far on the later chip edge helps to define the required design rules, needed for critical processes. In this case, the CPB is placed directly to the outer edge of the TFAP as shown in Fig. 39 b). The back side grinding tape, which is laminated to the top side of the wafer was investigated after wafer singularization and tape peel off. The tape shows the topology characteristics of the wafer top side after peeling off as shown in Fig. 39 c). There, it can be clearly seen, that the CPB is completely enclosed by the tape. The imprint also reveals that the half-cut dicing groove and the CPB have no

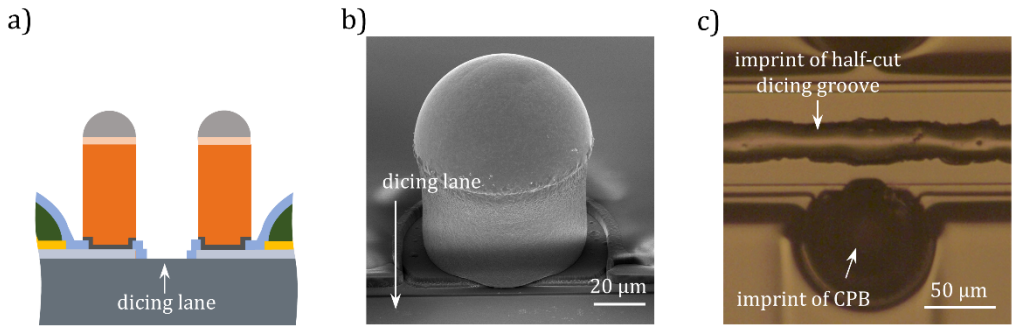


Fig. 39. DBG process limitation characterization. In a) a schematic cross-sectional image of CPBs very close to the dicing lane. In b) a SEM image prior DBG of an actual CPB set directly to the TFAP edge. In c) an optical micrograph of the back grinding protection tape after back side thinning and peeling off the tape. The tape shows the topology characteristics of the TFAPs and the CPBs. The imprint in the tape reveals, that the CPB is completely enclosed and separated from the half-cut dicing groove.

connecting cavity in the tape even having the CPB so close to the half-cut dicing groove. Hence, designing CPBs on the TFAP edge is not a process limitation for DBG.

Another critical component design was a very small or missing reinforcement opening. The reinforcement opening defines the contact area of the CPB to the EP layer, as shown in Fig. 40 d). The metal layers of aluminum (EP layer), Ti/Cu (seed-layer), and Cu (CPB Cu base) have a very good adhesion in between the layers. Typically, a ductile fracture mode appears in the aluminum when high mechanical loads are applied on the layer stack. However, the reinforcement layer consists of a very stiff and brittle material with a weak adhesion to the EP layer compared to the metal layer stack. The CPBs with a diameter of 65 µm on a missing reinforcement

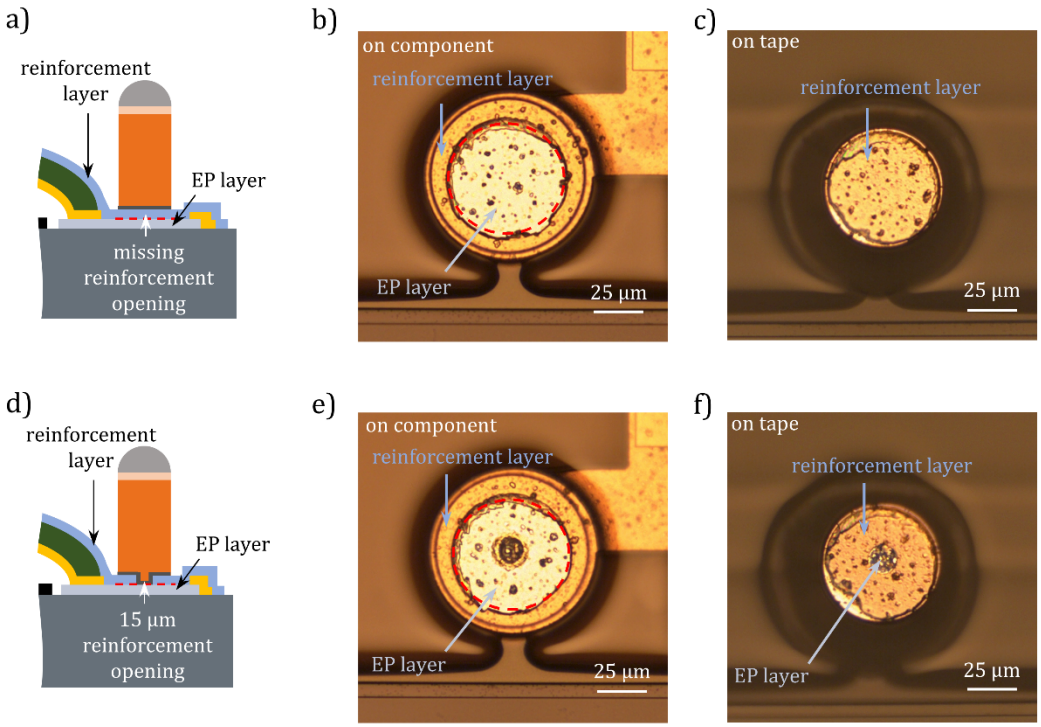


Fig. 40. Sheared/teared off CPB during DBG tape peeling. In a) schematic cross-section of a CPB on a completely closed reinforcement layer and the corresponding top view micrograph of the component with missing CPB in b) after tape peeling. In c) a top view micrograph of a CPB stuck to the grinding tape, which was teared off from a component with missing reinforcement opening. In d) the schematic cross-section of a CPB on a 15 µm diameter reinforcement opening and the corresponding top view micrograph of the component with missing CPB in e) after tape peeling. In f) a top view micrograph of a CPB stuck to the grinding tape, which was teared off from a component with 15 µm diameter reinforcement opening. The dashed red lines indicate the fracture interfaces. Reinforcement, capping, and sealing layer appear transparent in optical micrographs.

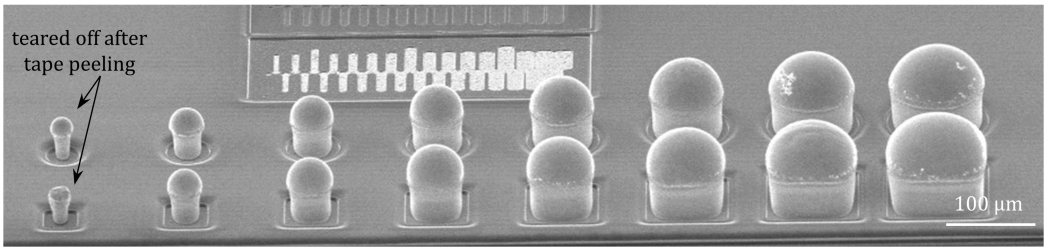


Fig. 41. SEM image of test structure component prior DBG. Round and square CPBs with varying size.

opening were sheared/teared off during tape peeling. The fracture interface was between the reinforcement and the EP layer underneath as shown in Fig. 40 b) and Fig. 40 c). The missing opening is just a test design, because the reinforcement layer electrically isolates the CPB from the EP layer.

Designs with a reinforcement opening of only 15 µm diameter for a CPB with 65 µm diameter were also sheared/teared off during the tape peeling. However, there are two fracture interfaces, one in between the reinforcement layer and the EP layer, and the other appeared as a ductile fracture in the aluminum of the EP layer as shown in Fig. 40 e) and Fig. 40 f). For both designs the teared off CPBs stuck into the grinding tape, which allowed to investigate the corresponding fracture interfaces. However, not all CPBs with a reinforcement opening of 15 µm were teared off. Already a reinforcement opening diameter of 27 µm with a CPB diameter of 65 µm showed no teared off CPBs after DBG grinding tape pealing.

Further, CPB diameter variations were investigated after DBG grinding tape peel off. The smallest CPB diameter was approx. 15 µm but had no reinforcement opening underneath. These CPBs were also frequently teared off. However, already the next larger CPB diameter with approx. 25 µm and a reinforcement opening diameter of only 8 µm did not appear to be teared off during the grinding tape peeling process. In Fig. 41 the test structures with varying CPB diameters are shown.

DBG is a suitable separation process for components with a TFAP and CPBs. The process gives reliable results and a large processable design window in terms of CPB size and position on the component. However, the mechanical connection of the CPB is essential to avoid missing CPBs after peeling the grinding tape. This is mainly

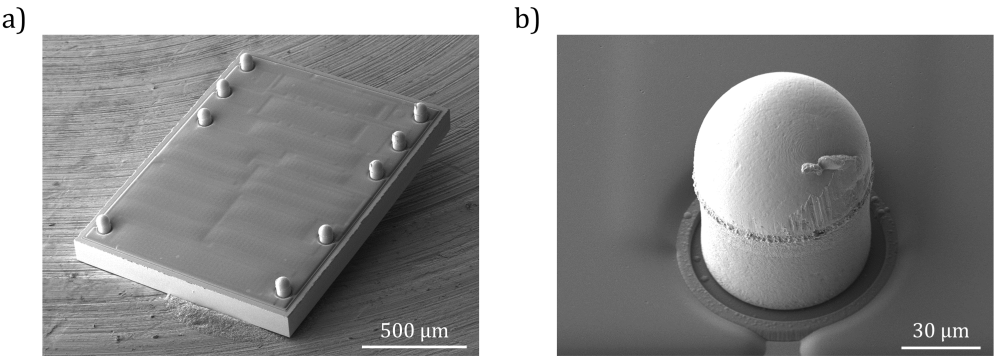


Fig. 42. SEM images after DBG. In a) a whole RF-filter component with a TFAP and CPBs after DBG is shown. In b) one CPB of the component in a) is shown. The slight CPB solder cap damage was caused by sample preparation.

dependent on the ratio of reinforcement opening and CPB diameter. After the DBG wafer singularization, components of interest are ready for pick and place into an assembly feeding tape, i.e. a stripe with repetitive small recesses for the components. The assembly tape is then sealed with a foil on top and rolled on a reel. In this state the tape & reel can be used for automated component pick and place assembly on e.g. a PCB. A representative component after DBG is shown in Fig. 42.

2.10 CPB Manufacturing summary

Manufacturing process steps might have significant fluctuations, malfunctions, etc., which then negatively impact the quality and reliability of the components. Therefore, in a manufacturing fab the environment, the manufacturing tools, intermediate component states and the manufacturing outcome of single process steps are typically monitored. The monitoring must fulfill the requirements of a measurement system analysis to ensure a reliable tool, process, and component quality monitoring. This allows to monitor if e.g. a process is inside a defined specification to ensure good manufacturing results. A failure mode and effects analysis (FMEA) is an option to identify the probability, the impact on a product, and the probability to detect a specific failure. The FMEA helps to identify failure risks and to implement monitoring if needed. This could be for example the photoresist film thickness and its variation

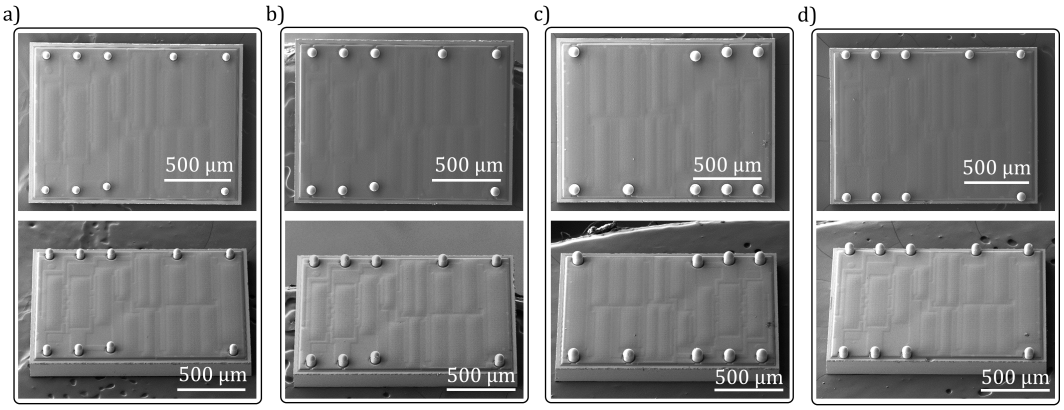


Fig. 43. SEM images of multiple RF-filter component designs with s TFAP and CPBs. The upper image is in the top view and the lower image in an angled view of the same component. CPB diameter variations with 55 µm in a), 65 µm in b), and 75 µm in c). In d) the CPB diameter is 65 µm but the position of the CPB is on the outer edge of the TFAP very close to the chip edge.

on one and over all processed wafers in a defined specification. Further, specifications arise also from the customer in terms of component reliability and performance.

However, in this work the focus was not the implementation of "frozen" processes and the corresponding monitoring for mass production; but to provide first demonstrator components by the development of CPB manufacturing processes and to investigate the miniaturization potential, the suitability and reliability of TFAP RF-filters with CPBs. Nevertheless, the developed manufacturing processes are used at least as a base for the intended implementation of monitored mass production processes, which then must fulfill all requirements requested by quality standards and customers.

In summary, suitable processes were developed for CPB wafer-level manufacturing on TFAP using a multi-design layout including the component singularization. This demonstrates the feasibility of CPB on RF-filters as interconnections. Some design variations with varying CPB diameters and CPB position are shown Fig. 43. In Fig. 44 a) a SEM image of a FIB cut through the whole CPB is illustrated. Fig. 44 b) shows the crystal structure of the electroplated Cu and Ni, and the intermetallic compound (IMC) Ni_3Sn_4.

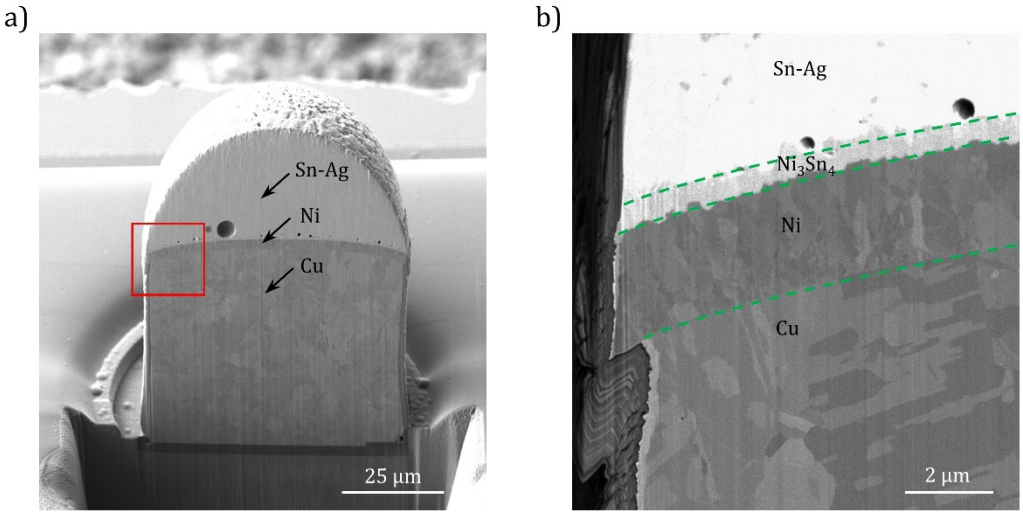


Fig. 44. SEM images after FIB cut through the CPB. In a) the front view on the cutting plane. Some voiding in the Sn-Ag solder is visible. The red frame in a) is shown as magnified SEM image in b). b) shows the crystal structure in the cutting plane of electroplated Cu and Ni. The magnified SEM image reveals the IMC of Ni_3Sn_4 formed during the solder cap reflow between the electroplated Ni and the Sn-Ag solder. The dashed green line indicates the material change.

3 TEST VEHICLE

The reliability of components with a TFAP and CPB interconnections was tested by special test vehicles. The test vehicle provides mounting spaces on a PCB for the assembly and soldering of 49 RF-filter components and their required passive components. Two component functionalities were tested. First, daisy chains which do

Table 9. Components tested for reliability. "Design" is related to CPB diameter and reinforcement opening diameter. Functionality is either daisy chain or functional. Assembly and soldering onto the PCB is performed with either solder paste or solder flux. Component footprint size is 1.20 mm x 1.60 mm.

Design	Interconnection Diameter	Reinforcement Opening Diameter	Functionality	Assembly	Sample Name
A	CPB - 65 µm	38 µm	fc (functional)	sp (solder paste)	**A_fc(CPB65/REop38)_sp**
A			dc (daisy chain)	sp (solder paste)	**A_dc(CPB65/REop38)_sp**
A				flux	**A_dc(CPB65/REop38)_flux**
B	CPB - 65 µm	47 µm	dc (daisy chain)	sp (solder paste)	**B_dc(CPB65/REop47)_sp**
C	CPB - 65 µm	27 µm	dc (daisy chain)	sp (solder paste)	**C_dc(CPB65/REop27)_sp**
D	CPB - 55 µm	28 µm	dc (daisy chain)	sp (solder paste)	**D_dc(CPB55/REop28)_sp**
E	CPB - 75 µm	48 µm	dc (daisy chain)	sp (solder paste)	**E_dc(CPB75/REop48)_sp**
SB	SB - 140 µm	n.a.	fc (functional)	flux	**SB_fc(140µm)**

not have a RF-filter function but do allow the detection of an interconnection interruption during reliability testing. Second, functional RF-filters which allow a sensitive detection of interconnection faults, and package or front-end related malfunctions. Either flux or SAC305 solder paste was applied to the PCB prior assembly and reflow to allow a fixation of the components and good solderability. The test vehicles were then exposed to standardized reliability tests followed by failure analysis. However, this chapter only describes the setup of the test vehicle and the components used. The details of components tested are listed in Table 9.

3.1 Test Components

The components tested are listed in Table 9 and include variations in CPB diameter, reinforcement opening diameter, and functionality. Additionally, one component design with solder bump interconnections with a diameter of 140 µm was tested as a reference. The CPB diameters were 55 µm, 65 µm, and 75 µm. The reinforcement opening defines the contact area between the CPB Cu base and the electrical path layer made of Al. The CPB overlap defines the area where the CPB Cu base overlaps the reinforcement layer. However, the mechanical strength is mainly defined by the contact area of CPB Cu base and the electrical path layer, i.e. the reinforcement opening diameter. This is because the reinforcement layer is very stiff and the adhesion to the electrical path layer below is weaker than between the Cu and the Al. In Fig. 45 the most important layers and dimensions in a mechanical cross-section SEM image related to the component variations tested are shown. All variations tested have a component size of 1.20 mm x 1.60 mm and 9 unevenly distributed CPBs. The chip size is relatively large and in combination with the unevenly distributed CPB positions on the component this design is more sensible to interconnection failures during temperature cycling testing and therefore, reliability testing with this design is preferred. The stand-alone CPB at lower right edge of the component in Fig. 46 endures the highest mechanical stress during temperature changes and is the most stressed CPB during TC (temperature cycling) reliability testing.

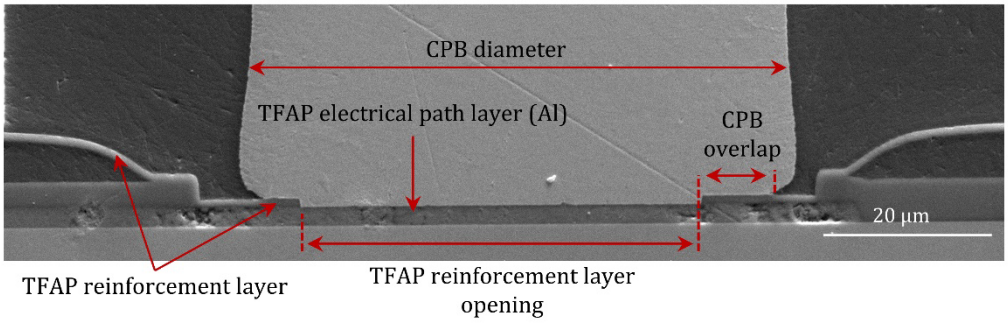


Fig. 45. SEM image of mechanical cross-section of CPB on a TFAP. Most important layers and dimensions for reliability testing are indicated.

Daisy chain components have no RF-filter function instead 8 of the in total 9 interconnections are electrically connected in pairs to each other. This allows a serial electrical routing through each CPB one after the other in combination with the daisy chain PCB. If any of the 8 interconnections fail, it can be detected by a simple electrical resistance measurement. Fig. 46 schematically illustrates the electrical routing for daisy chain components. The stand-alone CPB at the lower right edge, illustrated in Fig. 46 must endure higher mechanical stress compared to e.g. each of the 3 CPBs in the upper left corner. Because of the uneven number of CPBs on the components, one CPB which is mechanically less stressed during reliability testing, is electrically floating. An interconnection failure at this floating CPB (the middle CPB of the 3 CPBs

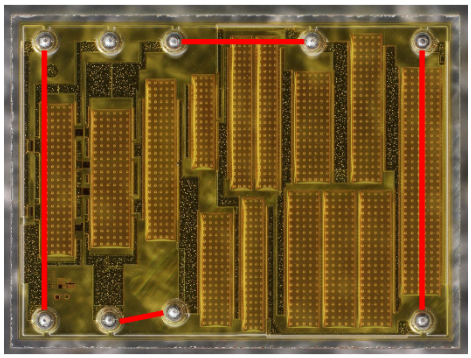


Fig. 46. Top view micrograph of a CPB component. The red lines indicate the electrical connection between pairs of CPBs for daisy chain functionality.

in the upper left corner of Fig. 46) cannot be detected in daisy chain test vehicles. However, under mechanical load during e.g. temperature cycling testing the unconnected CPB is not likely to fail first.

The functional SAW RF-filter components are frequency division duplexers for LTE Band 26 and support the uplink frequency of 814-849 MHz and the downlink frequency of 859-894 Mhz. The functional components were not optimized in terms of specific filter characteristics in the test environment. Daisy chain and functional filters were manufactured on the same multi-design wafers, i.e. all components have seen identical manufacturing steps. The geometry of the respective CPBs is shown in Table 9.

3.2 Printed Circuit Board

The standard FR4 multilayer PCBs have a dimension of 5 x 5 cm^2 with a thickness of 0.86 mm and 49 mounting spaces for RF-filter components. The PCB consists of a four-layer stack as illustrated in Fig. 47. The core and the prepreg (pre-impregnated fibers with polymer matrix) are made of glass fiber reinforced epoxy resin. The combination of the woven glass fiber fabric and the epoxy resin reduces the CTE of epoxy resin in the in-plane direction i.e. in x and y direction. The effective in-plane CTE of the whole PCB, which includes all PCB layers is approx. 16-17 ppm/K.

Two different PCB designs were used. One for daisy chain components and the other for functional RF-filter components. The difference is related to the electrical routing and the required mounting spaces for additional passive components. The PCB for daisy chain components support a serial electrical routing through CPBs one after the other. Additionally, each mounting space has a parallel connected mounting space for SMD resistors. This allows for a failure detection by simple electrical resistance monitoring. The PCBs for functional RF-filter components provide additional mounting spaces for passive components e.g. inductors and the electrical

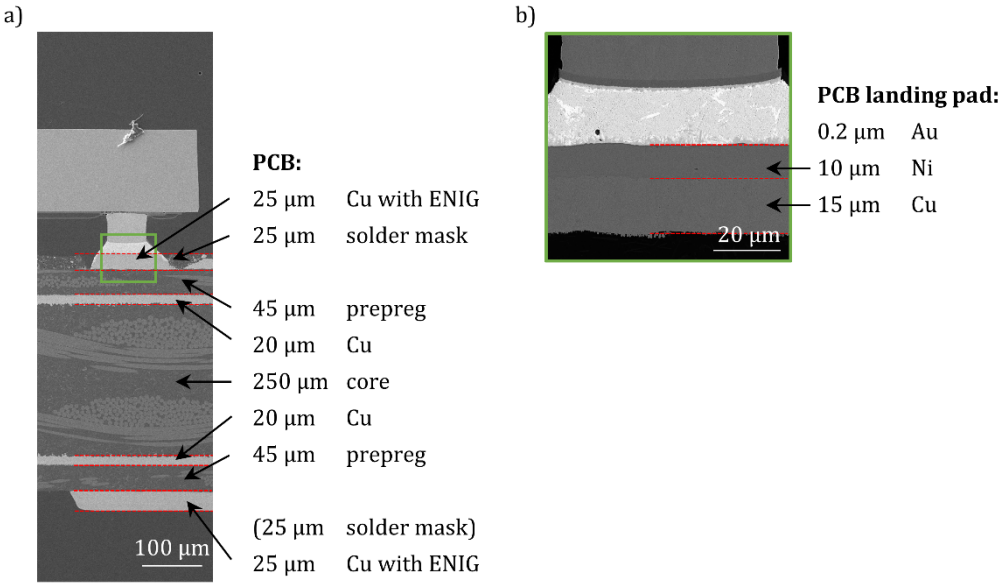


Fig. 47. In a) SEM image of PCB cross-section. Top-down layer stack of PCB: solder mask, Cu with ENIG (landing pads), prepreg, Cu, core, Cu, prepreg, Cu with ENIG (back side contact pads for electrical characterization), and solder mask (not visible in cross-section). In b) the magnified green frame in a) showing the cross-section of ENIG – PCB landing pad stack: Au, Ni, Cu. The thin Au layer is not visible because it dissolves into the solder during assembly soldering.

routing for RX (receiver signal), TX (transmitter signal), ANT (Antenna), and ground. The passive components are needed to match the RF-filter components close to the specified 50 Ω system impedance.

The landing pads are defined areas where the CPBs are soldered to the PCB. The landing pads consist of an electrically conducting trace made of a layer stack of Cu, Ni, and Au which is called Cu with ENIG (electroless Ni, immersion Au), as shown in Fig. 47 b). The traces have a width of 80 µm. Au acts as oxidation barrier and therefore supports the solder wetting during soldering. However, the gold is dissolved into the solder material during the solder process. The final landing pad size of 80 x 80 μm^2 is defined by the solder mask opening with a size of 120 x 80 μm^2 as the final layer on the PCB and the trace width of 80 µm. A schematic top view image is shown in Fig. 48. Landing pad size and solder volume are critical parameters in terms of component reliability and must kept constant and reproducible. The solder mask is an electrically insulating resin layer created by photolithography and acts as a solder barrier during the solder process. However, the accuracy in which the solder mask openings can be

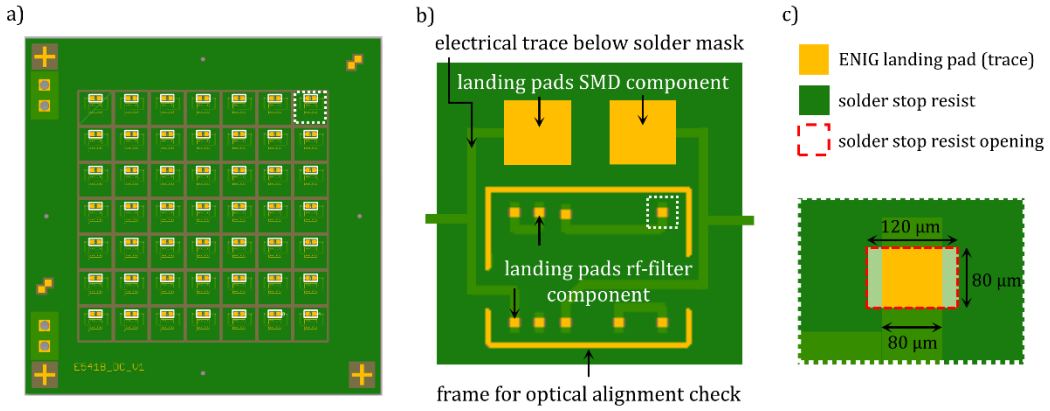


Fig. 48. Top view schematic of a daisy chain PCB. In a) with alignment marks in the corners for assembly and solder paste printing. The area inside the dashed white line in a) is magnified in b) and schematically shows the mounting spaces for one daisy chain component and its electrically parallel SMD resistor. The visible frame allows an easy top view alignment check after the assembly process. The area inside the white dashed line in b) is magnified in c). c) shows one landing pad and its dimensions of 80 x 80 µm², which is given by the solder mask opening and the trace width.

aligned to the Cu with ENIG layer during PCB manufacturing is limited. Therefore, the solder mask openings on the trace were designed broader than the actual trace. By combining the trace width and a broader solder mask opening, the limited overlay accuracy of the solder resist does not impact the landing pad size. A slight shift of the landing pad position, had no negative impact on the assembly process of the components if components were assembled into solder paste. The PCBs were cleaned with degreasing solvent prior assembly to remove potential contaminations.

3.3 Solder Paste Stencil Print or Flux Application

To ensure proper soldered joints between the PCB landing pad and the CPBs after the soldering process, either flux or solder paste was applied to the PCB shortly prior component assembly. A commercial standard activated rosin-based flux was applied via a flux-pen on the whole PCB. The flux-pen contains a solvent to keep the rosin-based flux in a low viscosity, which supports the spreading on the surface. Most of the contained solvent did evaporate fast after pen application. The left thin flux layer is sticky enough to hold the components on place after assembly until the

soldering process in the continuous furnace. Component flux dipping was not supported on any available pick-and-place assembly tools at the time present. Fluxed PCBs were cleaned in a commercial flux-cleaning tool after the soldering process.

The solder paste was printed onto the PCB through a stainless-steel stencil with a thickness of 40 µm and rectangular openings in the dimensions of 100 x 80 µm^2. The stencil was optically aligned to the PCB using the alignment marks in the corners of the PCB to ensure a well-placed solder paste depot on each of the PCB's landing pads. A commercial SAC305 (ROL0, type 5 powder) no-clean and halogen-free solder paste was printed with an automated solder paste printer. The solder paste's metal content of 88.5 w% was composed of 96.5 w% Sn, 3.0 w% Ag, and 0.5 w% Cu. The components were then assembled directly onto the solder paste depots. The sticky solder paste allowed to handle the assembled PCBs without shifting the components until soldering process. Both, small landing pads for CPBs and large pads for passive components have been sufficiently printed with solder paste using the same stencil. In Fig. 49 the stencil layout, the stencil opening position after alignment on the interconnection landing pad, and a micrograph after solder paste printing is illustrated. Fig. 49 c) shows some flux bleeding from the solder paste around the landing pads. By adjusting the print parameters this effect was eliminated.

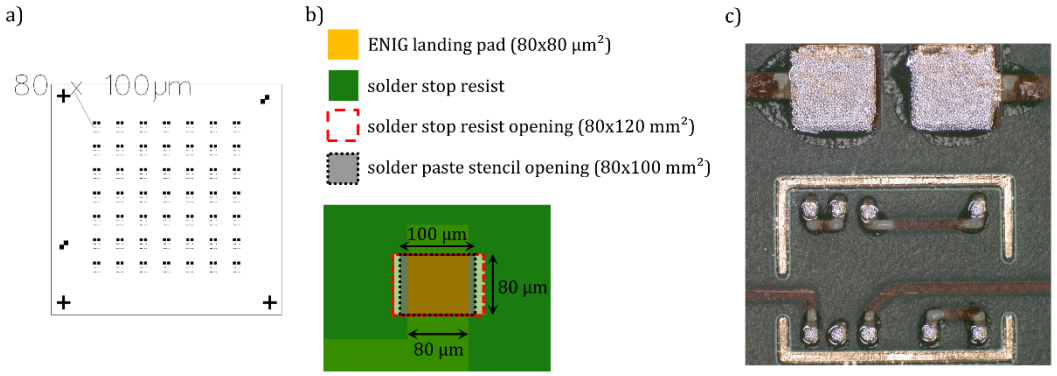


Fig. 49. In a) the top view design of the stencil for solder paste printing. The alignment features (cross and double-square) are in the corners of the stencil. Black color represents the stencil openings. b) shows the schematic top view of one CPB landing pad on the PCB including the stencil opening position. In c) a top view micrograph of the daisy chain component landing pads and the corresponding electrical resistor mounting space are shown after the solder paste print. Some flux bleeding from the solder paste is visible.

3.4 Assembly & Soldering of Components

Assembly of the components was performed with a commercial laboratory pick and place tool. The RF-filter components and the passive components were supplied to the assembly tool via tape & reel. The geometry data of the corresponding PCB design and the optical detection of the alignment marks on the PCB allowed a precise definition of the landing pad position for assembly. Further, each component position was automatically detected by a camera when picked via vacuum pipette from the tape and placed precisely onto the PCB. The soldering process or also called reflow was performed directly after the assembly in a continuous furnace according to the IPC/JEDEC J-STD-020F standard, as already described in Table 7 of chapter 2.8 Sn-Ag Cap Reflow. The soldering process using only a fluxed PCB was critical for component reliability, due to poor soldering between the CPB solder cap and the PCB landing pads. This behavior is described in more detail in chapter 4.3.3 Failure Analysis & Discussion (Flux Assembly). For the assembly into flux only, PCBs with already assembled/soldered passive components were used. However, the assembly onto printed solder paste depots followed by soldering in the continuous furnace provided an excellent interconnection between the component and PCB as illustrated in Fig. 50. The additional solder material even supported a self-centering of the CPBs in relation to the landing pad's center, i.e. slight component misalignment prior to the soldering

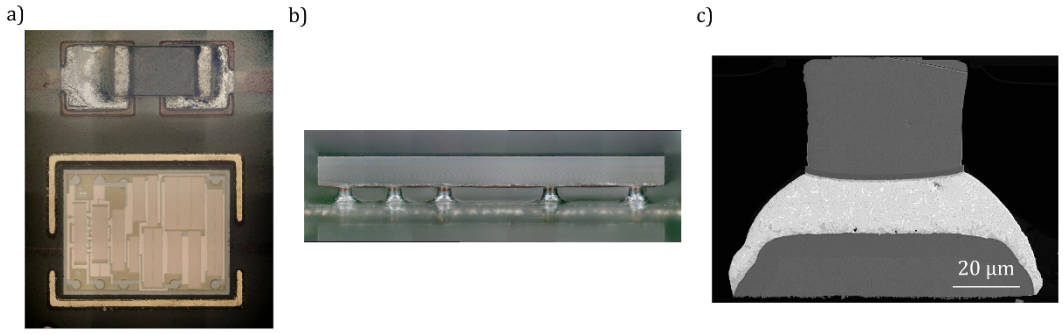


Fig. 50. Components assembled and reflowed with solder paste. In a) the top view micrograph with electrical resistor and the RF-filter component after soldering to the PCB. In b) the side view micrograph of a soldered RF-filter component. In c) a SEM image of a mechanical cross-section of one CPB interconnection soldered to the PCB.

was corrected by a self-alignment mechanism induced by the surface tension of the liquified solder.

3.5 Component Failure Detection

Failures in the test vehicles during reliability testing were detected in three different ways. The first method is a simple manual discontinuous electrical resistance measurement of daisy chain test vehicles after a defined reliability test duration. The daisy chain test vehicle is designed in a way, that the electrical path is routed through 8 of the in total 9 CPBs of one component to achieve a serial routing. Hence, two CPBs each are electrically bridged to each other on component side. On the PCB side 6 landing pads are electrically bridged and 2 landing pads are used for electrical input and output, respectively. Each mounting space has a 1 kΩ electrical resistor in parallel. In the case of functional CPB interconnections, the electrical resistance measured will be very low. However, if one CPB interconnection fails the small electrical current for the electrical resistance measurement will flow through the parallel 1 kΩ resistor. The electrical resistance measurement can be done at every single mounting space or by measuring the whole PCB at once as all mounting spaces

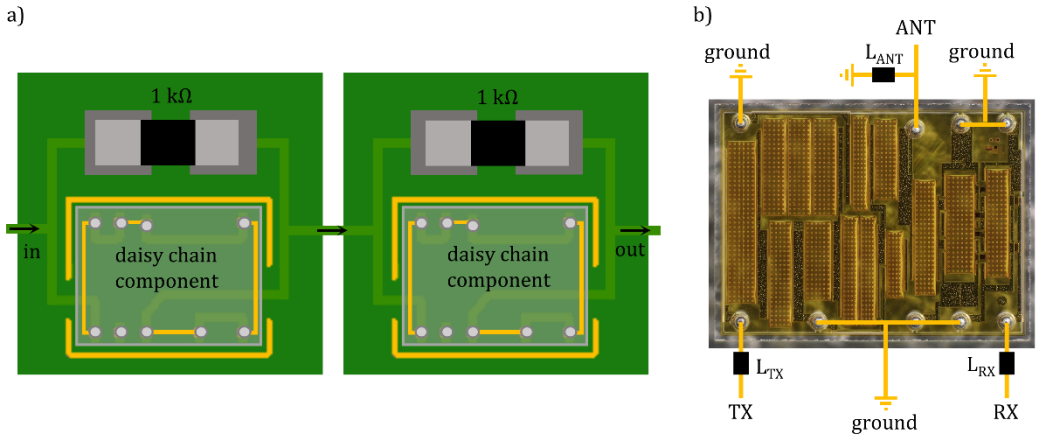


Fig. 51. In a) the schematic of the serial electrical routing through the CPB interconnections for daisy chain components. The schematic shows two serially connected mounting spaces. The electrical current during resistance measurements flows either through the daisy chain component or if an interconnection fails through the 1 kΩ resistance. b) shows a functional RF-filter component facing upwards with the respective matching circuit designated. The inductors used for the resistance matching were L_{TX} = 5.8 nH, L_{RX} = 6.2 nH, and L_{ANT} = 9.1 nH.

are also electrically connected in series. The second method is the continuous electrical resistance measurement of the daisy chain test vehicle. This method allows an automated detection of interconnection failures with a high resolution in terms of timing without reliability testing interruption, which was used during temperature cycling reliability testing. The electrical routing of the daisy chain test vehicle is schematically illustrated in Fig. 51 a). However, the daisy chain test vehicle does only reveal a total failure or interruption of the electrical path and cannot detect already occurring RF-filter characteristic changes. Further, using the continuous electrical resistance monitoring does not show, which exact component on the PCB failed.

The third method was the frequency vs. insertion loss characteristic measurement of the functional RF-filter test vehicles by a network-analyzer. Each mounting space on the test vehicle was composed of the functional RF-filter and passive components to reach a system impedance of approx. 50 Ω. The matching circuit and the respective inductors are shown in Fig. 51 b). The fully automated characterization by contacting the PCB backside with measurement probes was performed after the assembly and soldering as the non-stressed reference. The comparison-measurements of the stressed components were performed after a defined reliability test duration.

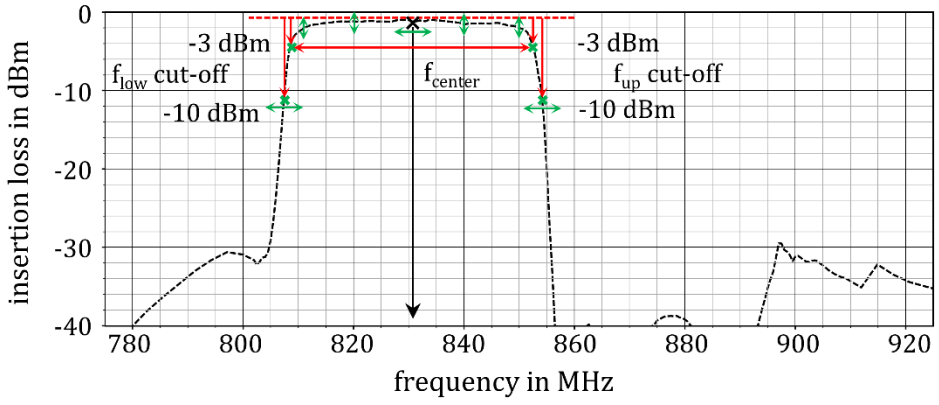


Fig. 52. Graph of frequency vs. insertion loss of a RF-filter component to illustrate failure criteria. The center frequency (black cross) is defined as the mean value of the lower and upper cut-off frequencies at -3 dBm (measured from the top of the pass-band, indicated with a red dashed line). A center frequency shift and/or a shift at the -10 dBm cut-off frequencies of more than 1 ‰ after reliability testing is considered as a component failure (horizontal green arrows). An insertion loss change of more than -0.5 dBm in the frequency pass-band area above the -3 dBm limit is also considered as component failure (vertical green arrows).

Using the RF-filter characteristic as a reliability test criterion is the most important and strictest method because any occurring failure which influences the RF-filter characteristic will be detected. Therefore, the origin of the failure e.g. corrosion of RF-filter acoustic or CPB interconnection failure, does not matter. Each functional test vehicle was composed of 49 individual RF-filter components and their respective passive components. Each functional component was assessed by the comparison of the non-stressed and the stressed measurement of center frequency, insertion loss, and the cut-off frequencies (pass-band edges). The component's center frequency is the mean value of the lower and upper cut-off frequency at an additional signal insertion loss of -3 dBm. A component is considered as failed if at least one of the following applies; the center frequency shifts more than 1 ‰, the lower or upper cut-off frequency shifts more than 1 ‰ at an insertion loss of -10 dBm, or the insertion loss shifts more than -0.5 dBm above the -3 dBm pass-band limit. Center frequency shift, cut-off frequency shifts, and the insertion loss as failure criteria are schematically illustrated in Fig. 52.

However, the test vehicle characteristics cannot directly be referred to the final component specifications, due to the different component and PCB environment, and the missing molded underfill.

4 Component Reliability & Failure Analysis

Large parts of this chapter were already published in [46–48].

Consumer products often consist of hundreds of electronic components. Each of these components contributes to the function of these products. However, if one component fails the entire device could be affected. Since most products get increasingly powerful functions in smaller device size, single failed components cannot easily be replaced. Hence, a failure of one single component can lead to an irreparable misfunction of the whole device. Reliability testing is used to reduce the risk of unexpected component failures. Temperature cycling (TC), unbiased highly accelerated stress test (uHAST), damp heat steady state (DHSS), and dry heat (DH) are the main reliability tests for electronic components and systems. After assembly onto the PCB all components tested were preconditioned according to JEDEC J-STD-020E moisture sensitivity level 2a (MSL 2a) for 120 h at 60 °C and 60 % RH followed by 6 additional reflows.

4.1 Overview Reliability Testing

During TC reliability testing the components investigated were stressed according to JEDEC JESD22-A104E (test condition G) alternatingly with -40 °C / 125 °C in a two-sectional climatic chamber with a moving platform. The soak time in each temperature section was 15 min (soak mode 4). Hence, one cycle took 30 minutes. TC

allows the accelerated simulation of alternating temperature induced mechanical stress affecting the components. During normal use such harsh conditions will not be reached in the final consumer product, however, the harsh conditions allow accelerated aging. Alternating temperatures induce mechanical stress into the components. This is caused by the mismatch of the CTE between the various materials. The largest part to this mismatch is contributed by the PCB and the component's LN substrate. The CTE of the PCB is influenced by e.g. the electrical path material and its portion in the PCB, the PCB's woven fiberglass cloth and epoxy material, and the solder mask. The in-plane CTE of the PCB can be considered as isotropic, i.e. the in-plane thermal expansion is independent of the direction. The effective CTE for the whole PCB material composition is approx. CTE_{PCB} = 16-17 ppm/K. The CTE of the SAW RF-filters emerges from the TFAP, filter structures, electrical path layers and the LN component substrate. However, the greatest impact can be expected from the LN substrate due to its thickness and its high modulus of elasticity. LN has an anisotropic thermal expansion, i.e. the CTEs are different for different directions. This behavior arises from the LN's crystal orientation. The LN single crystal can be orientated in various angles to achieve best micro-acoustic properties, which then also has an influence on the CTE of the SAW

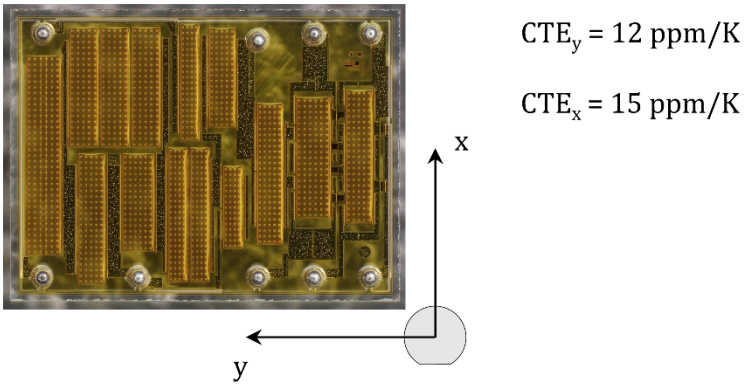


Fig. 53. Top view micrograph of SAW RF-filter with TFAP. Definition of in-plane anisotropic thermal behavior of LN via coordinate system for LN cut used. Chip orientation on the wafer is as indicated with the schematic wafer in the coordinative cross.

RF-filter. The LN crystal orientation used in this work has a thermal expansion in the direction of the short component edge of approx. CTE_x = 15 ppm/K and in the direction of the long edge of approx. CTE_y = 12 ppm/K.

In Fig. 53 the CTE orientation is illustrated. The largest CTE mismatch arises between the y-direction of the LN substrate and the PCB board. The fact that the long component edge has the largest CTE mismatch to the PCB causes large stress during TC. Due to the uneven distributed CPBs the mechanical forces acting are also different. The stand-alone CPB in the upper left chip corner in Fig. 53 experiences the highest mechanical stress during temperature cycling.

High temperature can accelerate physical and chemical effects like the growth of IMCs between two contacting metals. Additional humidity increases the probability of chemical corrosion reactions. The uHAST was performed according to JEDEC JSTD-A118B at 130 °C and 85 % RH (relative humidity) and the DHSS reliability test was performed according to IEC 60068-2-67 Cy at 85 °C and 85 % RH in appropriate chambers. DH testing was carried out according to IEC 60068-2-2:2007 Bb at 150 °C in a drying oven.

Although in the final device application mainly components with molded underfill are used. But for reliability testing only open top components were investigated, i.e. after assembly and reflow no molded underfill was applied. The open top components are significantly more vulnerable to failure because the missing underfill does not mechanically support and further seal the components from the environment. From practical experience of similar builds and from other publications [49], components with molded underfill achieve much better reliability results by several factors especially for TC reliability testing. However, the testing of molded components demands much time and resources. Hence, the open top vehicles are preferred for reliability testing as they allow a faster detection of possible weaknesses in the package or at the CPB interconnections.

In summary, TC testing can point out mechanical vulnerabilities in the design and material composition, whereas DHSS and uHAST can reveal potential corrosion sensitivity. DH testing will accelerate diffusion reaction like IMC growth. Depending

on the functionality, for daisy chain components mostly the interconnections affect the reliability results but for functional components both, the interconnections and the package which protects the sensible acoustic structures affect the reliability of the components tested.

In the following chapters the reliability results of three different test groups are presented. First, components with CPBs which are soldered to the PCB only by using flux. Second, various component designs with CPBs which are soldered to the PCB after the application of solder paste to the PCB prior assembly. And third, components with the already established SB interconnection technology which are soldered to the PCB only by using flux. The minimum reliability testing requirements to classify component designs as pass are listed in Table 10. The table refers to components which are tested open top, i.e. molded underfill is not applied to the test vehicle.

Table 10. Minimum reliability test requirements to pass testing for daisy chain and functional test vehicles. Testing may only be performed with open top components, i.e. the components are neither mechanically supported nor sealed by a molded underfill. A minimum of 40 components shall be tested.

Test	Conditions	Minimum Requirement	
		Daisy Chain	Functional
DH	150 °C	504 h	504 h
uHAST	130 °C / 85 %RH	504 h	144 h
DHSS	85 °C/ 85 %RH	504 h	504 h
TC	-40 °C / +125 °C 15 min dwell	no failures at 480x and failure probability < 5 % at 500x with 90% confidence interval	no failures at 480x and failure probability < 5 % at 500x with 90% confidence interval

The preparation of mechanical cross-sections which are used for failure and IMC analyses must not have any impact on the samples. The separation and cross-section techniques induce mechanical stress to the components. For analyses however, only the damage induced by the reliability testing is of interest and further damage during sample preparation must be prevented. The components to be tested were therefore embedded into a two-component resin with low shrinkage during curing. The liquid resin mixture was applied on the whole test vehicle and a soft vacuum to ensure the filling of the gap between components and PCB. After resin curing, the mounting spaces of interest were separated by sawing. The mounting spaces were then again

casted in a two-component resin under soft vacuum to prevent trapping of air bubbles. The cured resin was then ready for mechanical grinding and polishing until the plain of interest. This technique prevented further damage after reliability testing, e.g. crack formation or delamination induced by the mechanical separation and cross-sectioning methods.

4.2 Statistical Fundamentals for Temperature Cycling Reliability Evaluation

In this study no statistical fundamentals are required to understand uHAST, DHSS, and DH reliability results. However, the TC reliability results are usually fitted against a distribution, which describes the trend of the data set best. Depending on the failure mechanisms of the components, different distributions like Weibull, Lognormal, Exponential, and Loglogistic can be used. For distribution analysis the "Minitab" software is used. Each component design and the related assembly method with flux or solder paste represent a different data set. To determine which distribution fits best to the TC reliability data sets the adjusted Anderson-Darling (AD*) method or the Pearson correlation coefficient are suitable. The distribution parameters are estimated either by the "maximum likelihood method" or the "least square method". Typically, the maximum likelihood method should be preferred for Weibull distributions, because it is assumed to achieve more accurate parameter estimates [50, 51]. A confidence interval can only be calculated for distributions where the parameters are estimated with the maximum likelihood method. Using the least square method does not allow to calculate a reliable confidence interval [51]. However, in some data sets the maximum likelihood method did not achieve appropriate parameter estimates; thus, the least square method was used. The AD* statistic or the Person correlation coefficient evaluate the correctness of one fit for the arbitrarily censored reliability data. Low AD* values indicate a good fit of the data set to the respective distribution. However, AD* values may not be compared between different data sets. [52, 53] For these data sets the Person correlation coefficient is a

positive number and can go up to +1, which would indicate a perfectly fitting distribution. [54]

It is common practice to apply the Weibull distribution for TC reliability results of solder joints. The Weibull cumulative distribution function (cdf) $F_{(x)}$ is given by:

$$F_{(x)} = 1 - e^{-\left(\frac{x}{\alpha}\right)^{\beta}}, x \geq 0, \alpha > 0, \beta > 0, \tag{4.1}$$

where x is the number of TCs, α is the Scale parameter, and β represents the Shape parameter [55]. The fitted Weibull distribution is linearized in the Weibull plot by scaling the ordinate as $ln\left(-ln\left(1 - F_{(x)}\right)\right)$ and the abscissa as $ln(x)$. The MTTF (mean time to failure) of a Weibull distribution is given via the formula [56]

$$MTTF = \alpha\Gamma\left(1 + \frac{1}{\beta}\right). \tag{4.2}$$

The MTTF is calculated by using the gamma function Γ, the Scale, and Shape parameters of the Weibull distribution. The gamma function allows the extension of the factorial function, which is defined only for positive integers, to non-integer values and complex numbers (except non-positive integers). The MTTF value gives the average time when to expect a failure. However, the MTTF does not give information of the survival probability of a component at a certain time [57]. In the following chapters the TC data sets are evaluated against Weibull, Lognormal, Exponential, and Loglogistic distributions to ensure the correct distribution selection.

4.3 Reliability Results of Copper Pillar Bump Components (Flux Assembly)

Large parts of this chapter were already published in [47].

In this chapter the reliability results of daisy chain RF-filter components with a TFAP and CPBs which were soldered to the PCB with flux only (without solder paste) are presented. The reliability requirements were not fulfilled due to poor soldering to

the PCB using flux. Nonetheless, the results are presented because it can be assumed that the failures were caused by an assembly and soldering issue during the fluxing and assembly process rather than by the components themselves. Flux was applied to the whole test PCB shortly prior daisy chain component assembly. The reflow which solders the CPBs to the PCB followed directly after the assembly. Details of the assembly and soldering are given in chapter 3 Test Vehicle. The daisy chain test vehicles were cleaned with a commercial flux cleaner tool after assembly. Unfortunately, the cleaning agent used at first attacked the unprotected Cu surface of the CPB base. Some material was etched from the CPB Cu base. However, the mechanical weakening was not significant as enough material remains. Fig. 54 shows a well-soldered CPB component using only flux after assembly.

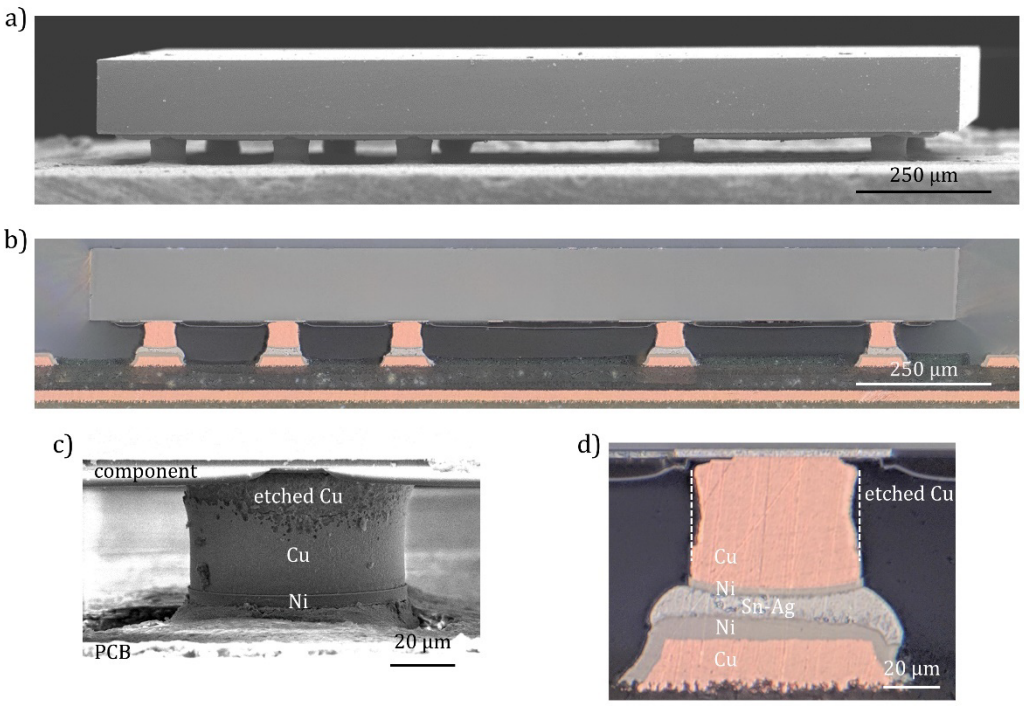


Fig. 54. Components soldered (1x reflow) with flux and subsequent flux cleaning. In a) the side view SEM image of a RF-filter component with CPB interconnections. In b) a micrograph of a mechanical cross-section. The RF-filter component is well-soldered to the PCB. The width of the CPBs in images of mechanical cross-sections strongly depend on the cross-section plane, due to the cylindrical shape. c) shows a magnified SEM image of one soldered CPB. The flux cleaning agent attacked the Cu base, which can also be seen clearly in the cross-sectional micrograph of one CPB in d). The dashed white line in d) indicates the original shape of the CPB.

The corroded CPB Cu base is mostly present in the region close to the component and not close to the solder (PCB side). This effect is caused by a very thin IMC layer formed between Sn and Cu. The thin layer is created during the solder cap reflow process (CPB manufacturing) and the soldering to the PCB by surface diffusion of the solder along the CPB Cu base [58]. The formed IMC of Cu_3Sn on the Cu sidewall is resistant against the flux cleaning agent; hence, no corrosion occurs in this area. However, test vehicles of later reliability testing were flux cleaned only using an alternative commercial flux cleaning agent which was non-corrosive.

4.3.1 Preconditioning, Dry Heat, uHAST, and Damp Heat Steady State (Flux Assembly)

The daisy chain test vehicles were first checked for their electrical resistance after assembly (1x reflow) and the subsequent flux clean. Therefore, the electrical resistance was measured to be approx. 60 Ω if the test vehicle was fully functional for reliability testing. Components not electrically connected (1 kΩ) were identified and inked by manual resistance measurements of all mounting spaces of the test vehicle. The test vehicles were preconditioned after assembly according to JEDEC J-STD-020E moisture sensitivity level 2a (MSL 2a) at 60 °C / 60 % RH for 120 h followed by 6 additional reflows in the continuous furnace directly after the moisture soak. The test

Table 11. Reliability results of daisy chain test vehicles soldered with flux only. The reliability for DH, uHAST, DHSS is classified to have failed. Minimum test duration required to pass is 504 h for daisy chain functionality. Sample A_dc(CPB65/REop38)_flux tested, i.e. design A with 65 µm CPB diameter and 38 µm diameter reinforcement opening as daisy chain component soldered to the test PCB with flux only.

Sample	Test	Passed components				
		assembly 1st reflow	MSL 2a 7th reflow	72 h	96 h	504 h
A_dc(CPB65/REop38)_flux	DH 150 °C	100 %	100 %	98 %	n.a.	98 %
	uHAST 130 °C 85 % RH	100 %	98 %	n.a.	95 %	95 %
	DHSS 85 °C 85 % RH	100 %	100 %	98 %	n.a.	96 %

vehicle was measured again for functionality and forwarded into the reliability testing. The results of DH, uHAST, and DHSS are presented in Table 11. The sample size was 49 components each for DH and DHSS, and 44 components for uHAST.

For daisy chain test vehicles, none of the components may fail before 504 h test duration to pass DH, uHAST, and DHSS reliability testing. However, single components failed early during reliability testing whereby the reliability is classified to have failed for RF-filter components with CPB interconnections which were soldered to the test PCB with flux only (without solder paste). The failure root cause is assumed to be poorly soldered interconnections of CPBs and the PCB as discussed in chapter 4.3.3 Failure Analysis & Discussion (Flux Assembly).

4.3.2 Temperature Cycling (Flux Assembly)

The test vehicles were preconditioned after assembly according to JEDEC J-STD-020E moisture sensitivity level 2a (MSL 2a) at 60 °C / 60 % RH for 120 h followed by 6 additional reflows in the continuous furnace directly after the moisture soak. The daisy chain test vehicle was tested for functionality prior and after the preconditioning. The preconditioning caused no failure at a total amount of 46 components. The electrical resistance is monitored continuously to detect interconnection failures during TC reliability testing. Fig. 55 shows the Weibull cumulative failure probability plot of the test results. The AD* value of 147 indicates that the failure-duration behavior is not well described by the Weibull distribution. The high failure rate at the beginning of the TC testing decreases significantly in the advanced stage of the test. Until 157 temperature cycles a total of 21 (46 %) components prematurely failed. However, during the further testing until 384 temperature cycles only 1 (2 %) additional component failed. The test was continued until 770 temperature cycles, but no further components failed, thus 24 (52 %) components were still functional and in total 22 (48 %) components failed early within only 384 temperature cycles. The test vehicle clearly failed the minimum TC reliability requirements of a maximum of 5 % failure probability at 500 temperature cycles.

The early failing of 48 % of the components tested can be explained by the presence of various failure modes. The prematurely failed components were poorly soldered to the PCB's landing pad; hence solder fatigue, which follows a Weibull distribution, was not the relevant failure mode here. The first attempt to fit the data to a Weibull distribution curve using the maximum likelihood method did not give reasonable results. The estimated MTTF was approx. 6000 temperature cycles and a standard deviation of 20000 temperature cycles. With this method the standard deviation is several times higher than the actual MTTF value. An attempt with the least square method resulted in a more reliable MTTF value of 279 temperature cycles and a standard deviation of 365 temperature cycles. But also, the standard deviation is higher than the actual MTTF value which further emphasizes the lack of a failure-duration behavior sufficiently describable with a Weibull distribution

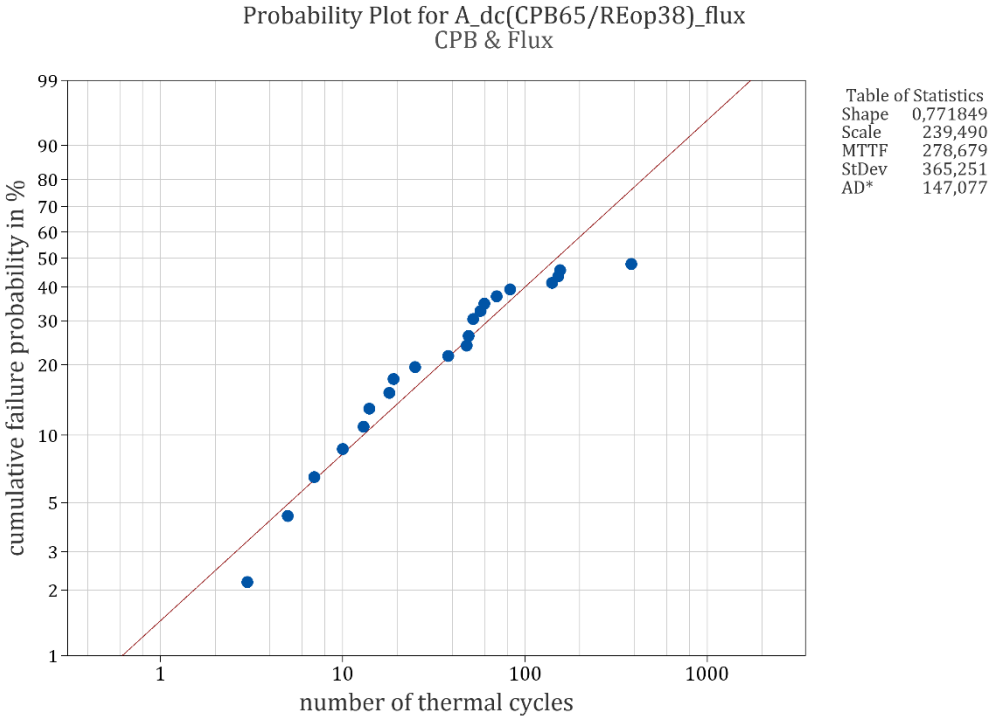


Fig. 55. Results of TC reliability testing as graph of cumulative failure probability vs. the number of thermal cycles. TC was performed with sample A_dc(CPB65/Reop38)_flux at -40 °C / +125 °C with 15 min dwell time each. Red line indicates the Weibull distribution fit using least square fitting method. The Weibull distribution does only describe the reliability behavior of premature failures. However, between 384 and 770 temperature cycles no further component failed and 52 % were still functional.

related to the whole dataset. Further, the least square estimation method to create the cumulative failure probability plot in Fig. 55 considers only the actual detected exact failure times and not the time span without any failures (384 – 770 temperature cycles) or the still functional components at the end of TC testing (right censored data) to calculate the fitting curve. This is why the 770 temperature cycles data point is not displayed in the graph. However, this further reinforces the assumption of variant failure modes and the derived imprecise description by the Weibull distribution for the results if not considered separately. On the other side, time spans of 386 temperature cycles without any failure suggest, that in case of a proper soldered test vehicle, the reliability requirements can be met. But in this experiment, it could not be established with reasonable time and tool effort.

Beside the electrical resistance monitoring during TC reliability testing, the formation of IMCs was quantitatively investigated. IMCs are formed by a reaction of e.g. Ni or Cu with Sn. IMCs are more brittle than pure Sn solder. Hence, this can promote crack formation along IMC interfaces or delamination of materials which are exposed to thermo-mechanical stress. The IMC formation between Cu and Sn is much faster than between Ni and Sn. Generally, the IMC formation is accelerated by raised temperatures. In this test vehicle design Ni layers function as a diffusion barrier between Cu and Sn to decelerate IMC formation. The test vehicles were prepared for IMC analysis via SEM investigation on mechanical cross-sections after the assembly (1x reflow), after the preconditioning (6x additional reflows), and after preconditioning followed by 770 temperature cycles. The main IMC is formed between Sn and Ni. The electroplated solder cap contains approx. 97 w% Sn and 3 w% Ag, which is sandwiched between two Ni layers. The thin Au layer on the landing pad surface is first dissolved during the reflow process and may then precipitate as solid $AuSn_4$ or $(Au,Ni)Sn_4$ IMC. Sn and Ni will mainly form Ni_3Sn_4 if Cu is absent or only present in small amounts. The CPB Cu base is usually separated from the solder by the Ni diffusion barrier if the component is soldered well-aligned to the PCB, therefore, mainly the IMC Ni_3Sn_4 is formed. But, if a Cu source additionally provides Cu, e.g. by diffusion from the CPB Cu base when solder is wetting the sidewall, the IMC composition might change and depends then on the Cu

concentration. Sn, Ni, and low Cu concentrations will mainly form $(Ni,Cu)_3Sn_4$ IMCs and with an increasing Cu concentration the formation of $(Cu,Ni)_6Sn_5$ will be more probable. Sn and Ag form the IMC Ag_3Sn. A detailed EDX spectroscopy analysis of IMC formation in the solder joints in chapter 4.4.5 Temperature Cycling (Solder Paste Assembly) supports these presumptions. IMCs are visible in the BSE (back scattered electron) detector SEM images by their different grayscales, which allows a qualitative area evaluation of the IMC formation progress. The quantitative material composition is evaluated by EDX. The IMC formation progress of the solder joints in

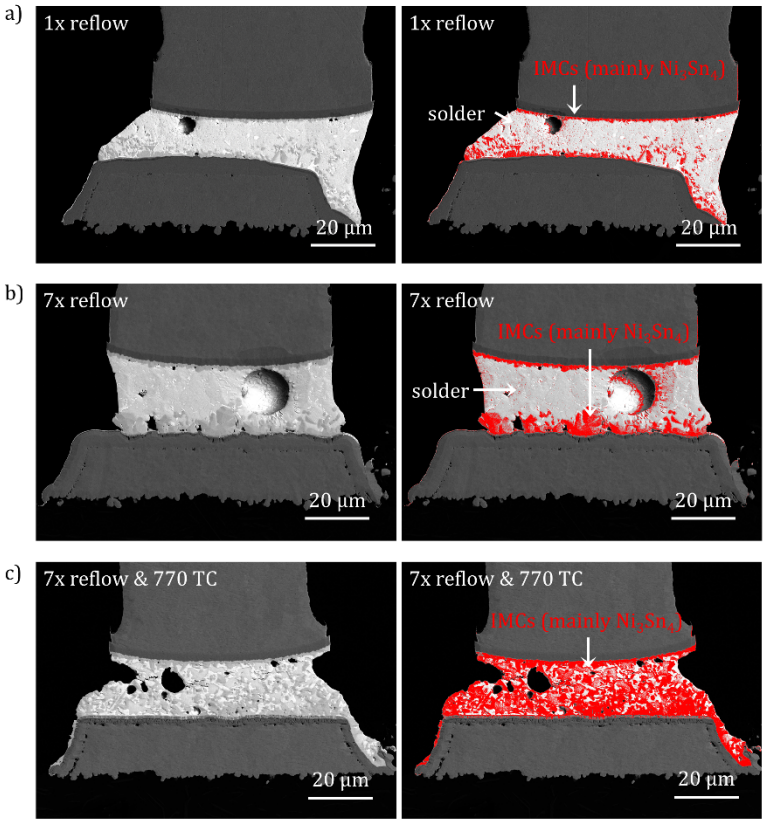


Fig. 56. SEM images taken with BSE detector of solder joint cross-sections to evaluate IMC growth. Components were assembled with flux only. The CPB can be seen in the upper and the PCB landing pad in the lower region of each image, respectively. IMCs are made visible in red by grayscale threshold filtering in the right of each image pair. In a) IMCs are formed only slightly after 1x reflow, i.e. after the assembly. b) shows the IMC formation after MSL2a preconditioning, i.e. in total 7x reflows. IMCs are more present compared to 1x reflow. Also, a large solder void is visible in b). In c) the IMC growth after 7x reflows and additional 770 temperature cycles at -40 °C / 125 °C with a dwell time of 15 min each is shown. Almost the whole solder is converted to IMC. The Ni barriers are still present. The very bright small areas in the solder region are Au containing IMCs.

the test vehicle soldered with flux only can be seen in Fig. 56. The IMC proportion after 1x reflow further increased after 7x reflow but still mainly Sn-Ag solder is visible. However, the temperature cycling converted most of the solder material into Ni_3Sn_4 IMC, as shown in Fig. 56 c). Ag_3Sn, and $AuSn_4$ or $(Au,Ni)Sn_4$ were present on a small scale. This bears a higher risk of crack formation in the solder joint because of the increased brittleness. The formation speed of Ni_3Sn_4 at the electroless deposited Ni from the PCB landing pad is faster than the formation at the electroplated Ni barrier side from the CPB. As the Ni barriers are still present the thickness is sufficient to avoid additional Cu diffusion, which would strongly accelerate the IMC formation.

4.3.3 Failure Analysis & Discussion (Flux Assembly)

Already the first reflows using a fluxed PCB revealed, that about half of the components were not correctly soldered to the PCB. Electrical resistance measurements and the additional side-view optical inspection by microscopy detected the missing electrical connection of CPBs to the PCB. Soldering experiments to improve solderability with an additional PCB cleaning prior assembly, a variation of the flux amount, a variation of the time spans between fluxing, assembly or soldering, a prolonged reflow, a faster or slower temperature ramp up, and increased peak temperatures did not result in better solder joints and reduced electrical failures. But, by testing various flux materials one was identified which significantly reduced the number of poor electrical connections in daisy chain test vehicles. However, faulty connections were still present as some components every 2 PCBs still failed after the assembly. At first it was assumed that the poor electrical connections after the flux material exchange were not caused by the soldering process anymore but only by the misalignment of components during assembly because some components were identified with electrical connection failure having a large misalignment. The absolute placement accuracy needed to be in the range of 15 µm to ensure a proper assembled component because the landing pad size is 80 x 80 μm^2 in combination with a CPB diameter of 65 µm. The laboratory pick and place tool and the variations in the solder stop resist of the PCB did not allow to reproducible reach

this accuracy. This challenge was further enforced by the missing self-alignment of components which were slightly misaligned from pick and place assembly when performing the reflow with flux only. Within a limited scope, if the solder volume is large enough, the surface tension of the molten solder can move the component in a perfectly centered position during the reflow.

However, the poor electrical connection was not only caused by component misalignment induced by the pick and place tool, but additionally by the still present poor solderability caused by sporadic non-wetting of the molten solder on the Au layer of the PCB's landing pad. One component which failed the electrical testing already after the assembly (1x reflow) was mechanically pulled from the PCB and revealed the poor solderability as the root cause. The micrographs are shown in Fig. 57. All landing pads in Fig. 57 b) except the number "3" show poor spreading of the molten solder on the Au surface, as large areas still shine golden. Landing pad numbers "6-9" show even only little interface areas between landing pad and the solder. The landing pad number "9" has the smallest interface area and the corresponding CPB in Fig. 57 a) even looks like that a permanent connection might not have formed during soldering. A slight shift of the component to the right can be seen but the mechanical cross-section images through the CPB and the PCB suggests a good mechanical connection for CPB number "1-5" (in contrast to "6-9") as the break plain is inside the solder material and the break plane area is similar to the CPB diameter.

But even if the electrical joint was sufficient for a low electrical resistance measurement, the mechanical connection between the component and the PCB might be weak and not sufficient to reach aspired reliability under thermo-mechanical stress. Fig. 58 shows the mechanical cross-sections of two components which passed the electrical resistance measurement after assembly (1x reflow) and after MSL2a preconditioning (7x reflow). It can be seen in Fig. 58 b) and d) that the solder did not spread on the landing pad. Further the IMC formation is not as pronounced on PCB side as one would expect when comparing to Fig. 56 b) when soldered sufficiently.

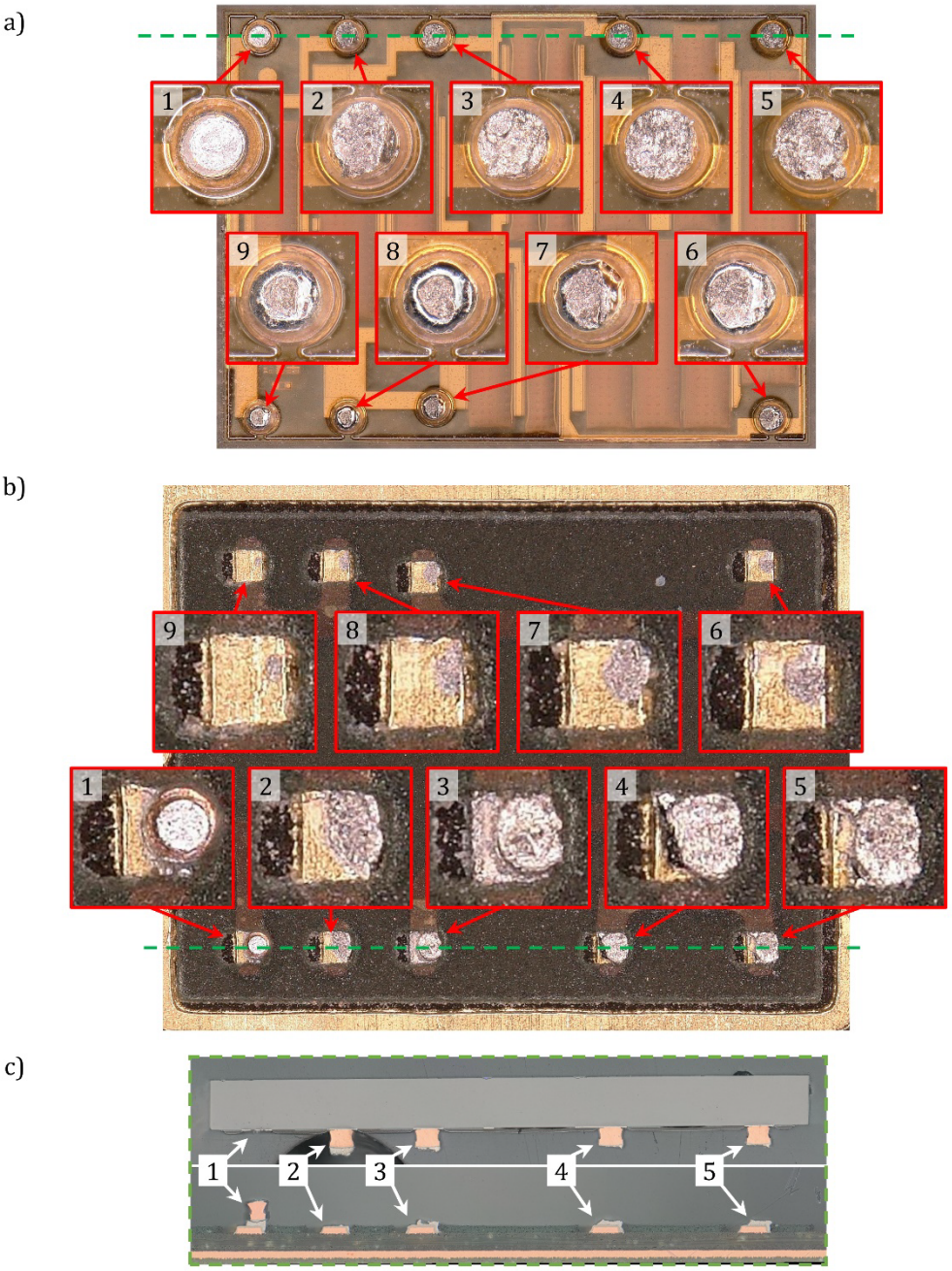


Fig. 57. Micrographs of poorly solder component which was pulled off after assembly. In a) the top view micrograph of the component with magnified inserts of the CPBs. In b) the corresponding top view micrograph of the PCB. c) shows a mechanical cross-section of the component in a) and the PCB in b). The cross-section plains are indicated by the green dashed lines. The CPB named "1" was pulled off the component and stuck to the PCB. CPBs named "2-5" have the fracture inside the solder with a fracture area similar to the CPB diameter. CPBs named "6-9" have the fracture inside the solder but the fracture area is significant smaller than the CPB diameter. Except landing pad "3" the surface the solder did not spread over the whole landing pad.

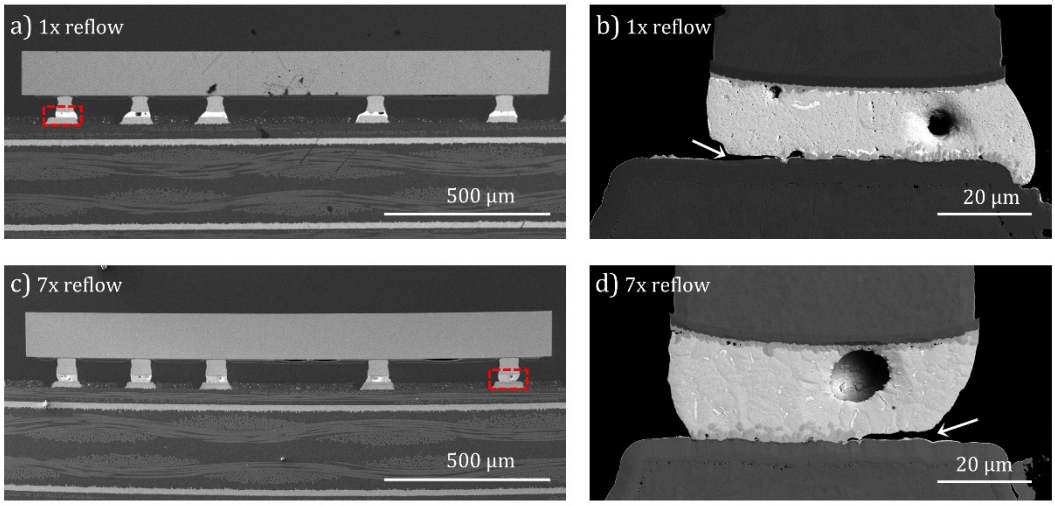


Fig. 58. Mechanical cross-section SEM images of components soldered with flux only. Components passed the electrical resistance test, but poor soldering is apparent. In a) one component after assembly (1x reflow) and in b) the magnified solder joint of the dashed frame of a). b) shows poor soldering of the CPB to the landing pad which is indicated by a white arrow. In c) one component after preconditioning (7x reflows) and in c) the magnified solder joint of the dashed frame of c). d) shows poor soldering of the CPB to the landing pad which is indicated by a white arrow. The components are well centered on the landing pad positions. Contact angle of solder in b) and d) indicate non-wetting on the Au surface of the landing pad. IMCs are developed weakly only on landing pad side.

The IMC formation is a prerequisite for a strong mechanical connection between Ni and Sn. The cross-section analyses and the TC reliability results confirm a weak mechanical connection between CPBs and the landing pads, which then causes a high failure rate only at the beginning of TC testing.

On the other hand, between 384 and 770 temperature cycles 52 % of the components stayed still functional without any further failure. This highly suggests the combination of different failure modes with a significant different MTTF. Fig. 59 shows a cross-section of one still functional component after 770 temperature cycles. The magnified SEM images of each solder joint reveal a sufficient solder wetting took place resulting in a strong mechanical connection. As already discussed, most of the solder is converted into Ni_3Sn_4 IMC after 770 temperature cycles.

In addition, DH, DHSS, and uHAST tests with identical component types and PCB but different solder technique (CPB & solder paste) passed the required test durations. This is a strong indicator that the weak mechanical connection caused also

here the failures leading to missed reliability requirements for flux soldered components.

As already discussed shortly, reflow experiments did not solve the issue of poor solderability. The cause might be a combination of the PCB behavior (surface finish, temperature induced bending), the solder volume of the CPB, the flux (type, volume), and the reflow profile. Unfortunately, the material and tools were limited and it was decided not to go in more detail with flux soldering for the time being. Nevertheless, as the failure rate decreased significant during TC testing and half of the components were still functional, it can be assumed that when components are soldered correctly, a sufficient reliability of CPB components soldered with flux only, can be achieved.

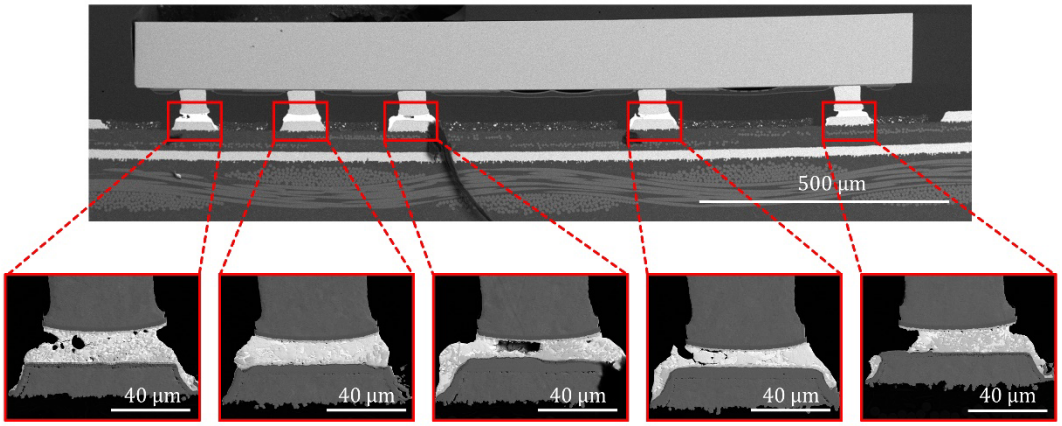


Fig. 59. Mechanical cross-section SEM images of still functional component after 7x reflow and 770 temperature cycles. Each interconnection is shown magnified. The solder has wetted the landing pads well. Solder is almost completely converted to IMC. The slight component bend is an image artefact caused by the SEM.

4.4 Reliability results of Copper Pillar Bump Components (Solder Paste Assembly)

Large parts were already published in [46].

The test vehicles used for reliability testing were preconditioned after solder paste assembly according to JEDEC J STD 020E moisture sensitivity level 2a (MSL 2a) at 60 °C / 60 % RH for 120 h followed by 6 additional reflows in the continuous furnace directly after the moisture soak. Daisy chain test vehicles were characterized by electrical resistivity measurements. Functional test vehicles by measuring and comparing the rf characteristics with a network analyzer (see also chapter 3.5 Component Failure Detection). The characterization measurements were performed after assembly, preconditioning, and defined test durations. Only test vehicles for uHAST reliability were flux cleaned after assembly. A reliability results summary of the designs tested is listed Table 12 and the detailed results are discussed in the following subchapters.

Table 12. Summarized reliability results for CPB components soldered with solder paste to the PCB. Passed or failed reliability requirements related to test and component design.

Design	Reliability test				
	Die shear test	**DHSS** 85 °C, 85 %RH	**uHAST** 130 °C, 85 %RH	**DH** 150 °C	**TC** -40 °C / 125 °C 15 min dwell
A_fc(CPB65/REop38)_sp	pass	pass	pass	pass	pass
A_dc(CPB65/REop38)_sp	pass	pass	pass	pass	pass
B_dc(CPB65/REop47)_sp	n.a.	pass	pass	pass	pass
C_dc(CPB65/REop27)_sp	n.a.	n.a.	n.a.	n.a.	fail
D_dc(CPB55/REop28)_sp	n.a.	n.a.	n.a.	n.a.	fail
E_dc(CPB75/REop48)_sp	n.a.	n.a.	n.a.	n.a.	pass

4.4.1 Die Shear Test (Solder Paste Assembly)

The die shear test provides details of the mechanical interconnection quality between die and PCB. The shear speed of 100 µm/s and the height of 75 µm of the shear arm are constant during testing. The shear tool detects the surface of the PCB close to the measurement position as a reference to set the shear tool height before starting the measurement. The shear distance and the resulting force is monitored. If the measured force drops 90 % compared to the highest value during the running test, an additional shear distance of 50 µm is added, before the test automatically ends.

Compared to the existing solder bump interconnection technology, CPBs do only provide a limited plastic deformation due to the smaller solder volume. The shear tool used did not have a freely rotatable shear arm. Therefore, in most cases the shear arm was not perfectly in parallel with the die at the beginning of the shear test. Hence, during the early stage of the shearing, the die rotates to be parallel to the shear arm. However, here already a plastic deformation of the CPB interconnections take place, which requires a lower force than a shear off without a die rotation. The rotation of the die and the resulting lower maximum force needed to shear off the die caused a broad variation of the detected maximum forces. Possibly the work (physical energy transfer), i.e. force along a displacement, would describe a more meaningful value to evaluate the strength of the interconnection with a fixed shear arm. However, the tool did not support this feature. An alternative is a freely rotatable shear arm to avoid a die rotation during shear off, to support an evenly distributed force transfer into the die resulting in more narrowly distributed measured values. This tool configuration was also not available at this time.

Nevertheless, more important than the detection of the highest possible force value during shear testing is the resulting failure mode. The failure mode or fracture level allows an evaluation of possible design and manufacturing flaws, which might cause a weak mechanical interconnection between the die and the PCB. After shear testing the die and the PCB were investigated via optical microscopy. Two failure modes were detected, first mode was a fracture inside the bulk solder (SnAg) and the second mode was a fracture inside the EP-layer (aluminum) below the CPB Cu base

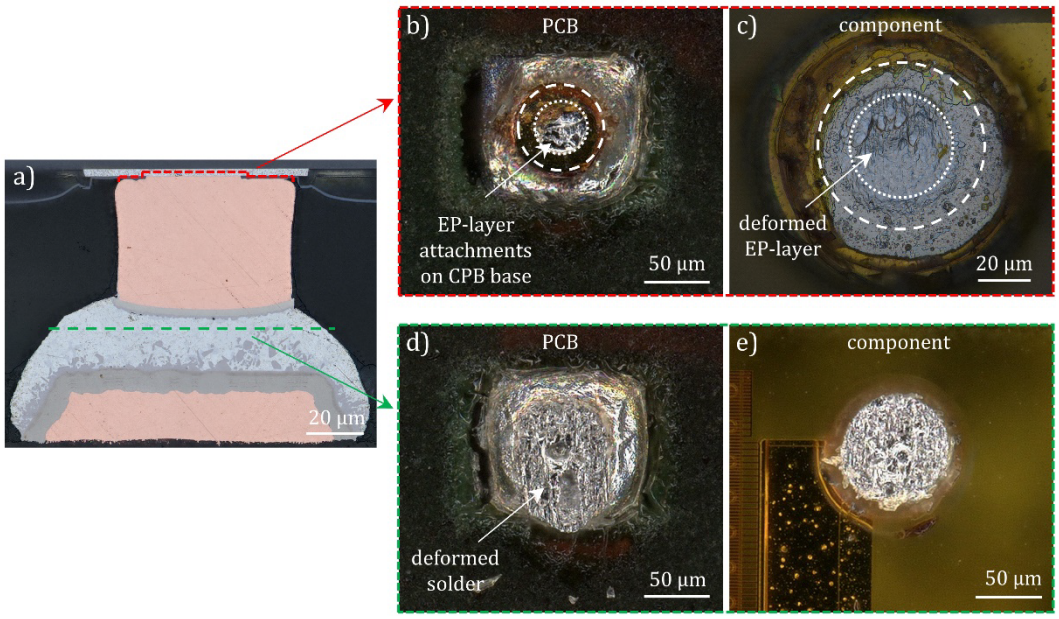


Fig. 60. Failure modes of die shear tests of CPB interconnections. In a) a cross-sectional micrograph of a CPB soldered via solder paste to the PCB. The red dashed line in a) indicates the fracture level inside the aluminum EP-layer and the green dashed line indicates the fracture level inside the bulk solder material. In b) and d) top-view micrographs of one landing pad on the PCB are shown and in c) and e) the corresponding component side. b) and c) show the first fracture mode inside the EP-layer, as the CPB sticks to the PCB after shearing off the die. The dashed circle indicates the CPB diameter and the dotted circle indicates the reinforcement opening, i.e. the contact area of the CPB Cu base to the EP-layer. Ductile fracture of the aluminum can be seen in c). The brittle reinforcement layer sticks to the CPB bottom in b). The second failure mode is shown in d) and e) with a ductile fracture inside the bulk solder material.

as shown in Fig. 60. Both, failure modes showed ductile breakage behavior, as the actual break takes place after a significant deformation of the corresponding material. This deformation can be seen in Fig. 60 c) and d). As expected, delamination between two materials was only detected between the reinforcement layer and the EP-layer in the CPB overlap (compare Fig. 45) region, which is known to have a weak adhesion. Both failure modes detected indicate an excellent mechanical connection between the component and the PCB via CPB interconnections.

The designs A_fc(CPB65/REop38)_sp and X_dc(CPB65/REop55)_sp were tested. The two designs vary only in their reinforcement opening diameter of 38 µm and 55 µm, respectively. However, X_dc(CPB65/REop55)_sp was only used for die shear testing as the overlap of the reinforcement layer with the CPB is only 5 µm. Hence, the risk of an open EP-layer due to CPB misalignment during CPB manufacturing would be high. To avoid damages to the EP-layer during wet-etch processes it must be

covered during manufacturing. Both designs were shear tested after MSL 2a preconditioning. Additionally, the design X_dc(CPB65/REop55)_sp was shear tested after stressing the test vehicles with DH (150°C) for 576h and 2008 h, respectively. Due to the high temperature the formation of inter metallic compounds in the solder region is accelerated. These compounds differ in their mechanical characteristics. This might influence the mechanical interconnection quality which was therefore determined by shear testing.

In Fig. 61 the die shear forces measured after MSL 2a preconditioning of both designs are displayed. In more detail, Fig. 61 shows the shear force and the failure modes detected at the CPBs for each die shear measurement. Each component has 9 CPB interconnections. Therefore, if e.g. the number of solder fractures is stated

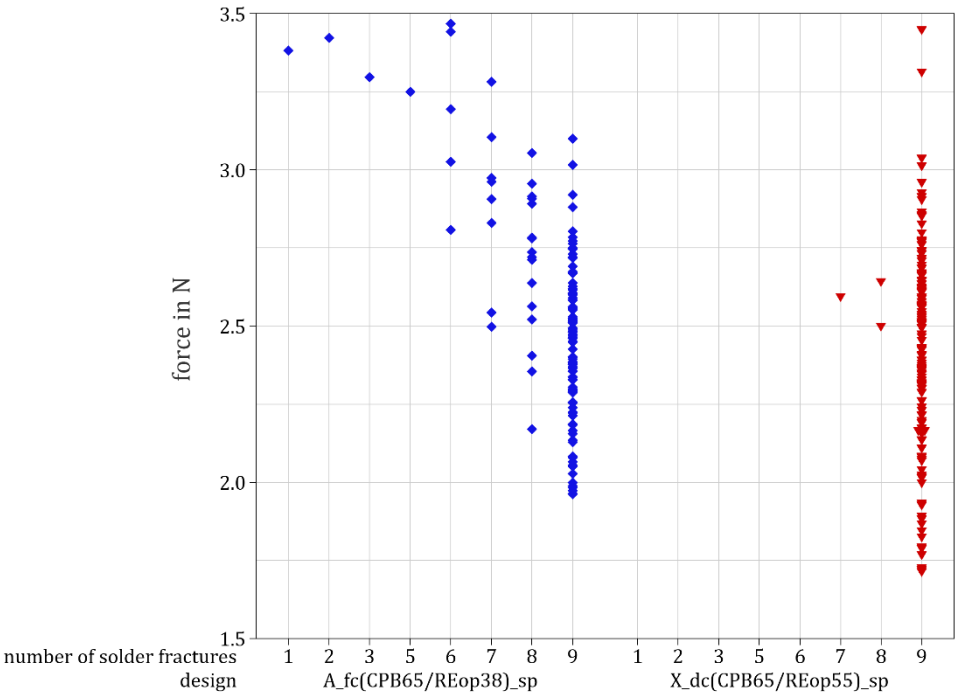


Fig. 61. Shear force results related to failure mode and design after MSL 2a preconditioning. Each die has 9 CPB interconnections in total. After shearing off the die each CPB position on the die and the corresponding landing pads on the PCB were investigated via optical microscopy. The number of solder fractures stands for CPBs sheared off on one die with the first failure mode, which is a fracture inside the bulk solder material. The difference to 9 gives the number of CPBs, which showed the second failure mode, i.e. fracture inside the EP-layer. Two designs were investigated, which vary only with the reinforcement layer opening diameter (38 µm and 55 µm). Larger reinforcement opening diameters show less second failure modes, i.e. inside the EP-layer.

with 8 in Fig. 61, then 8 of 9 CPBs had the fracture inside the bulk solder material and the remaining 1 of 9 CPBs had the fracture inside the EP-layer. However, it can be seen in Fig. 61 that the tendency of a fracture inside the EP-layer is significantly lower for the large reinforcement layer openings of 55 µm diameter. This effect comes from the larger interface area between CPB Cu base and the EP-layer which provides a better mechanical connection compared to the 38 µm reinforcement opening. This assumption is supported by the trend of an increasing shear force with an increasing number of CPBs with a fracture inside the EP-layer for the design A_fc(CPB65/REop38)_sp, i.e. the smaller reinforcement opening. The shear force statistics of both designs are listed in Table 13.

Table 13. Die shear test results of components with CPBs soldered with solder paste to the PCB. Two designs were tested which vary in the reinforcement opening diameter (38 µm and 55 µm). Testing was performed after MSL 2a preconditioning and DH storage at 150 °C. All designes were classified as passed.

Sample	Number of measurements	Mean value of force	Standard deviation	Dies with only solder fracture
A_fc(CPB65/REop38)_sp preconditioning MSL 2a	138	2.5 N	0.3 N	76 %
X_dc(CPB65/REop55)_sp preconditioning MSL 2a	150	2.4 N	0.3 N	98 %
X_dc(CPB65/REop55)_sp 576 h at 150°C Dry Heat	8	2.3 N	0.3 N	100 %
X_dc(CPB65/REop55)_sp 2008 h at 150°C Dry Heat	20	2.8 N	0.4 N	100 %

The analysis of the variance (ANOVA) for each mean shear force value is shown in Fig. 62 with a confidence interval of 95 %. The interval defines the range in where the true mean shear force value is located with a confidence of 95 %. It can be seen that the mean shear forces of A_fc(CPB65/REop38)_sp MSL 2a, X_dc(CPB65/REop55)_sp MSL 2a, and X_dc(CPB65/REop55)_sp 576 h do not differ statistically significantly, because the intervals overlap. The interval of X_dc(CPB65/REop55)_sp 2008 h, however, does not overlap with the other samples

and is therefore evaluated as statistically significantly different. Only fractures inside the solder region were detected for the DH stressed samples. The larger reinforcement opening results in a better mechanical connection of the CPB to the EP-layer which prevents the fracture inside the EP-layer even at higher shear forces. The increase of the mean shear force after 2008 h of DH is caused by the transformation of solder and Ni into IMCs to a significant extend. The large volume of stiff and brittle IMCs inside the solder causes a higher resistance to deformation resulting in a higher mean shear force. The large intervals for sample X_dc(CPB65/REop55)_sp 576 h and X_dc(CPB65/REop55)_sp 2008 h are caused by the small sample size.

The shear testing revealed that the reinforcement opening of only 38 µm diameter is sufficient, because the larger opening of 55 µm diameter did not result in statistically significantly different die shear results after MSL 2a preconditioning and after the minimum required DH storage for 576 h. The extended DH storage of 2008 h resulted in a higher mean shear force value and would therefore probably cause more EP-layer fractures in the design with 38 µm diameter reinforcement openings. However, even then the fracture mode would be still considered positive indicating an excellent mechanical joint between the die and the PCB by the CPB interconnections.

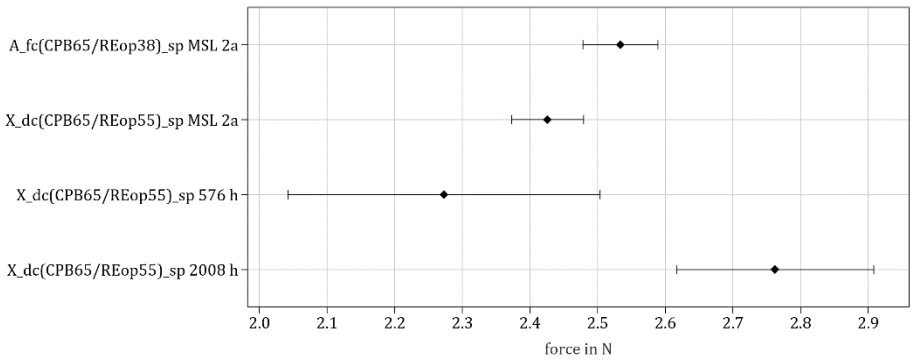


Fig. 62. Variance analysis interval plot of mean shear force values. Two designs tested after MSL 2a preconditioning and after DH (150 °). With a confidence of 95 %the mean value is inside the illustrated intervals. The intervals of A_fc(CPB65/REop38)_sp MSL 2a, X_dc(CPB65/REop55)_sp MSL 2a, and X_dc(CPB65/REop55)_sp 576 h overlap, hence the mean values are not statistically significantly different. The interval of X_dc(CPB65/REop55)_sp 2008 h does not overlap with any interval of the other samples, hence the mean value is statistically significantly different from the others. The higher shear forces of X_dc(CPB65/REop55)_sp 2008 h are due to the IMC formation inside the solder during DH storage.

4.4.2 Damp Heat Steady State & uHAST (Solder Paste Assembly)

The test vehicles for uHAST (130°C / 85 %RH) reliability were flux cleaned after solder paste assembly. The test vehicles for DHSS (85 °C / 85 %RH), however, were not flux cleaned. Additional experiments which are explained in this chapter revealed the mandatory execution of a flux clean prior uHAST to avoid corrosion induced delamination of CPBs. DHSS and uHAST expose the test vehicle to extreme environmental conditions. The high temperature and humidity might promote corrosion at interconnections but also at functional structures when humidity reaches inside the sealed package.

Table 14. DHSS and uHAST reliability test results of components with CPBs assembled with solder paste to the PCB. One functional and two daisy chain designs were tested. Each sample had 49 components soldered to the PCB. All designes were classified as passed.

Sample	Test	Passed components				
		assembly 1st reflow	MSL 2a 7th reflow	96 h	144 h	504 h
A_fc(CPB65/REop38)_sp	uHAST 130 °C 85 % RH	100 %	100 %	100 %	100 %	n.a.
A_dc(CPB65/REop38)_sp		100 %	100 %	100 %	100 %	100 %
B_dc(CPB65/REop47)_sp		100 %	100 %	100 %	100 %	100 %
A_fc(CPB65/REop38)_sp	DHSS 85 °C 85 % RH	100 %	100 %	100 %	100 %	100 %
A_dc(CPB65/REop38)_sp		100 %	100 %	100 %	100 %	100 %
B_dc(CPB65/REop47)_sp		100 %	100 %	100 %	100 %	100 %

The test vehicles were preconditioned prior reliability testing. The minimum requirement to pass uHAST is a test duration without failure of 504 h for daisy chain test vehicles and 144 h for functional test vehicles. For DHSS the minimum requirement for passing is 504 h for daisy chain and functional test vehicles. An overview of the minimum requirements can be found in Table 10. The samples A_fc(CPB65/REop38)_sp, A_dc(CPB65/REop38)_sp, and B_dc(CPB65/REop47)_sp were stressed with DHSS and uHAST. All test vehicles were classified as pass. No failures were detected in any sample during the required test duration. A detailed overview of the results is shown in Table 14. Each test vehicle consisted of 49 components soldered to the PCB. The RF-filter insertion loss against the frequency

is illustrated in Fig. 63 for one representative functional SAW LTE band 26 duplexer component prior and after uHAST. The RF-filter performance did not change according to the specified requirements explained in chapter 3.5 Component Failure Detection after uHAST for any of the functional components tested.

Due to the harsh environment during uHAST corrosion reactions are likely. The CPB interconnections are designed as a stack of multiple metal layers including (starting from bottom to top) the aluminum EP-layer, the sputtered 50 nm Ti adhesion-layer with 200 nm Cu seed-layer, and the electroplated CPB Cu base as shown in Fig. 64 a). A metal layer stack electrically conducting connected will create an electro-chemical contact potential. If an electrically conducting electrolyte (e.g. water with free available ions) is additionally present, chemical oxidation and reduction reactions might take place, i.e. corrosion. If the environment facilitates these reactions to occur, the less noble material according to the electro-potential

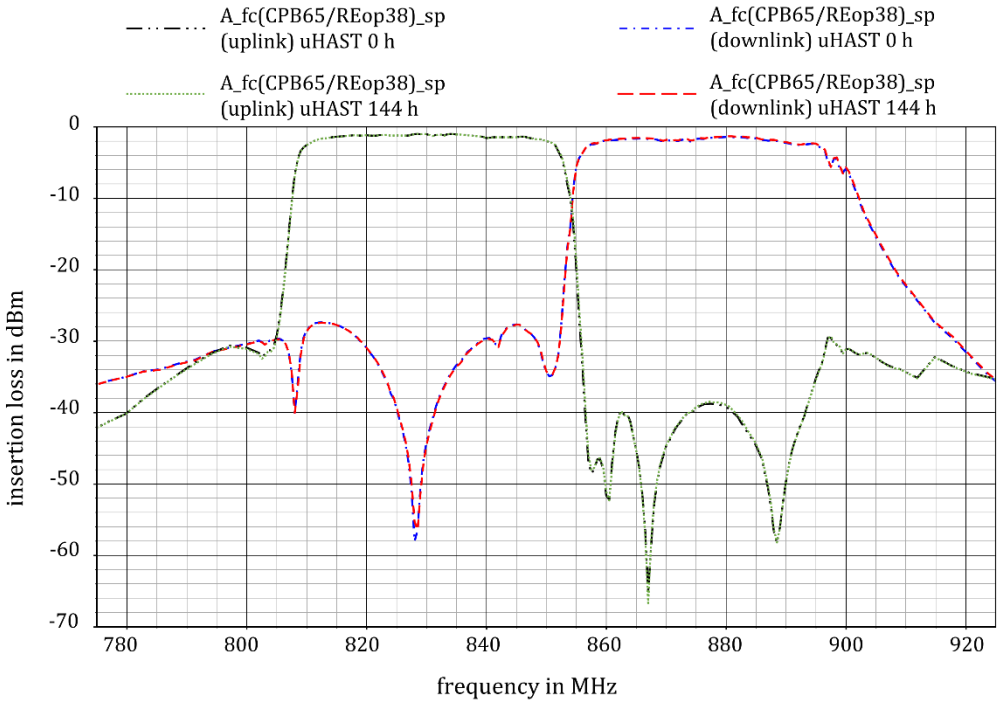


Fig. 63. Insertion loss vs. frequency of one representative A_fc(CPB65/REop38)_sp component measured after assembly (uHAST 0 h) and 144 h uHAST (including MSL2a preconditioning). LTE band 26 duplexer SAW RF-filter components were monitored. The components were only approximately matched to 50 Ω impedance with SMD inductors. The RF-filter characteristic of the shown component did not change after 144 h of uHAST.

series will oxidize, i.e. it will corrode. Al and Ti are less noble than Cu, hence prone to corrosion during uHAST. However, the uHAST did not create any corrosion nor failures at the flux cleaned test vehicles.

But it is known that flux residues from the solder paste can provide free ions and therefore support a corrosion reaction during uHAST. To promote and to understand a potential risk of corrosion during uHAST reliability testing one functional test vehicle with A_fc(CPB65/REop38)_sp components was not flux cleaned prior testing. The test vehicle had one early failed functional component after 144 h of test duration. All 49 components were investigated via C-SAM to detect changes at the interface region between the CPBs and the EP-layer. Approximately 24 % of the components showed significant differences in the size of the interface area within the same component in C-Sam images, which indicates a delamination at some CPBs. The failed component showed an almost white CPB in C-SAM imaging as shown in Fig. 64 b), i.e. a damaged interface of the CPB Cu base and the aluminum EP-layer. For further analyses via optical microscopy, SEM, and EDX the failed component was sheared off from the PCB. During shear off two CPBs were pulled from the component and were still stuck to the PCB. The first CPB investigated showed a ductile fracture mode inside the Al EP-layer, as shown in the micrograph and SEM image in Fig. 64 e) and f), respectively. Hence, the CPB still had a strong mechanical connection. The second CPB investigated did not create a plastic deformation inside the EP-layer or the CPB Cu base. Not even the brittle reinforcement was damaged or pulled off from the EP-layer in the CPB overlap area, as shown in Fig. 64 g) and h). The delamination interface was characterized by elemental EDX analyses in the areas shown in Fig. 64 i) (component side) and j) (CPB/PCB side). On the component side the Al of the EP-layer, the undamaged Si containing reinforcement layer, and the Ti adhesion layer were detected but Cu was not significantly present, as shown in Fig. 64 k). The EDX analysis of the CPB stuck to the PCB is shown in Fig. 64 l) and did not show significant amounts of Al, Si, or Ti but only Cu. The EDX analyses show that the delamination must have took place between the CPB Cu base or more precise between the sputtered 200 nm Cu seed-layer and the sputtered 50 nm Ti adhesion layer (see also chapter 2.2

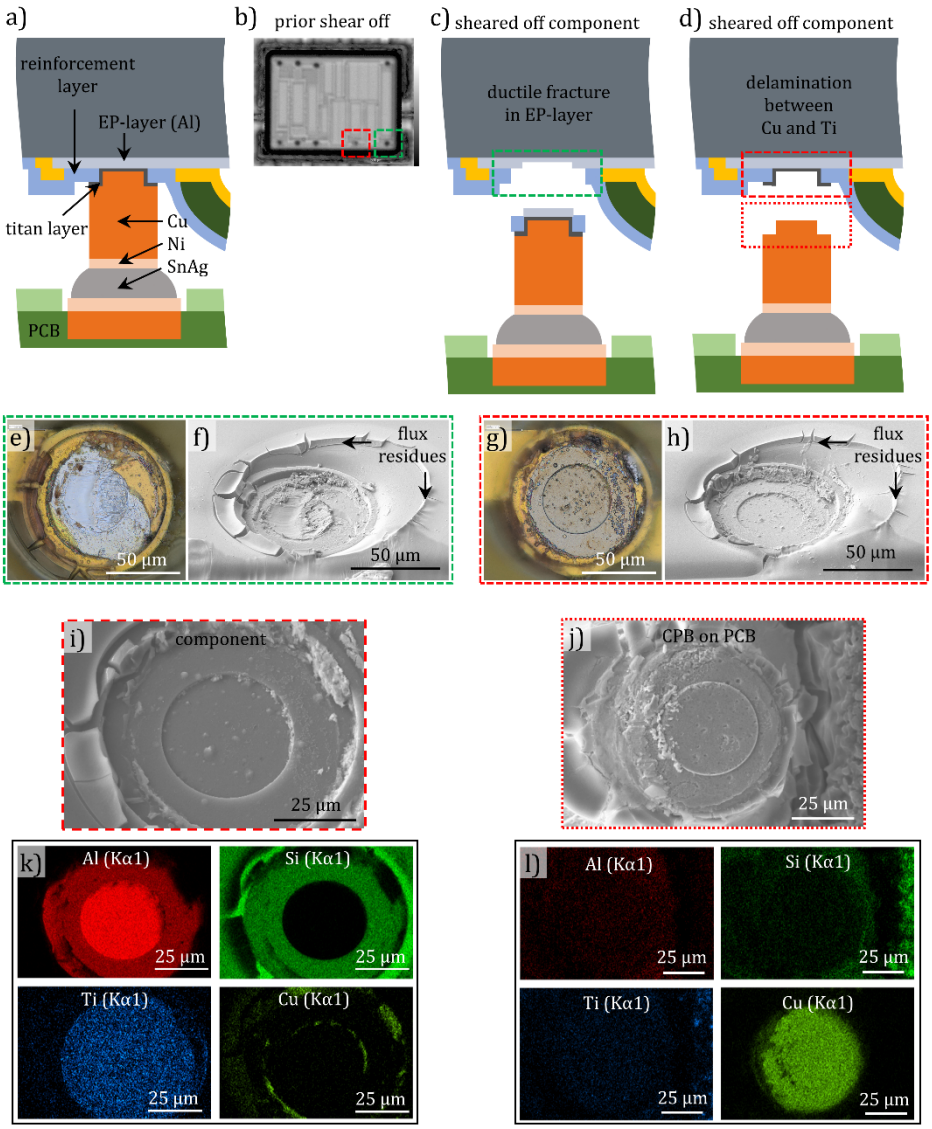


Fig. 64. Corrosion analyses after 144 h uHAST reliability testing of a failed component on a functional test vehicle without flux cleaning after assembly. Flux residues from the solder paste were detected to promote corrosion at the interface between the CPB Cu base and the Ti adhesion layer. In a) the schematic cross-section of the CPB soldered to the PCB. In b) the C-SAM image prior shearing off the failed component for further analysis, showing an almost white CPB (dashed red frame), i.e. delamination is present and an inconspicuous CPB (dashed green frame). In c) the schematic of a fracture inside the Al EP-layer (green dashed frame) after shearing off the component and in d) with a delamination (red dashed frame) between CPB Cu base and the Ti adhesion layer. The corresponding top view micrographs of the sheared off component is shown in e) and g). In f) and h) SEM images of e) and g) are shown, respectively. The missing CPB in e) and f) (green dashed frame) shows a ductile fracture as the Al EP-layer in the reinforcement opening is deformed. The missing CPB in g) and h) shows delamination between the CPB Cu base and the Ti adhesion layer, i.e. no plastic deformation is visible. This is investigated by a EDX analysis of the delaminated CPB. In i) the top view SEM image of the component site and in j) the top view SEM image of the CPB stuck to the PCB analyzed by EDX. The EDX mapping (Al, Si, Ti, Cu) of i) is shown in k) and the mapping of j) is shown in l). The reinforcement layer contains Si. The Ti of the adhesion layer is mainly detected on the component side. Al is not detected on the CPB Cu base. Hence, the interface of Ti and Cu delaminated.

Seed-Layer Deposition). As the Ti is not enclosed at the edges after CPB manufacturing it might be exposed to flux residues and the harsh uHAST environment (see also Ti under-etch in chapter 2.7 Seed-Layer Etch). Hence, Ti might corrode starting from the edges as it is less noble than Cu.

The additional intensified uHAST reliability test conditions revealed that the presence of flux residues originating from the solder paste lead to corrosion of the Ti adhesion layer and therefore a failure of components prior the minimum required test duration. The corrosion of the Ti caused only one component to fail early, but interface changes below the CPBs was detected via C-SAM in approx. 24 % of the components tested without flux clean. However, if the test vehicle was flux cleaned, no corrosion or early failures were detected. C-SAM analyses of the flux cleaned test vehicles which passed the uHAST and the non-flux cleaned test vehicles which passed the DHSS did not show any conspicuous shape change in the C-SAM images nor delaminated CPBs.

4.4.3 Intermetallic Compound Formation by Preconditioning - Multiple Reflows (Solder Paste Assembly)

Large parts of this chapter were already published by Eulenkamp et al. in [48].

IMCs are formed between different metals and are usually hard and brittle. The formation of IMCs was determined inside the solder matrix, which is sandwiched between the ENIG landing pad and the electroplated Ni diffusion barrier of the CPB. This chapter focuses on the IMC formation induced by the preconditioning procedure according to JEDEC J STD 020E moisture sensitivity level 2a (MSL 2a, 60 °C / 60 % RH for 120 h with 6 additional reflows). Therefore, the mechanical cross-section of a component after assembly and another component after MSL 2a preconditioning was investigated via SEM and EDX analysis. The cross-section surface of the preconditioned sample was additionally ion beam etched. The ion beam etch rates differ in dependence of the material and its crystal orientation. This creates a relief like surface showing the IMCs in more detail. The EDX and ion beam etch technique is

described in [48]. The IMC formation rate increases with increasing temperature. Additionally, the liquification of the solder during reflow highly accelerates the IMC formation. In Fig. 65 a) the SEM image of a mechanical cross-section after assembly, i.e. 1 reflow, and in b) after MSL 2a preconditioning, i.e. 7 reflows, is shown. As expected with increasing number of reflows the IMC volume inside the solder increases. Fig. 65 c) shows the ion beam etched cross-section after 7 reflows in where the IMCs are better visible and Ag_3Sn IMC grains are even only visible after ion

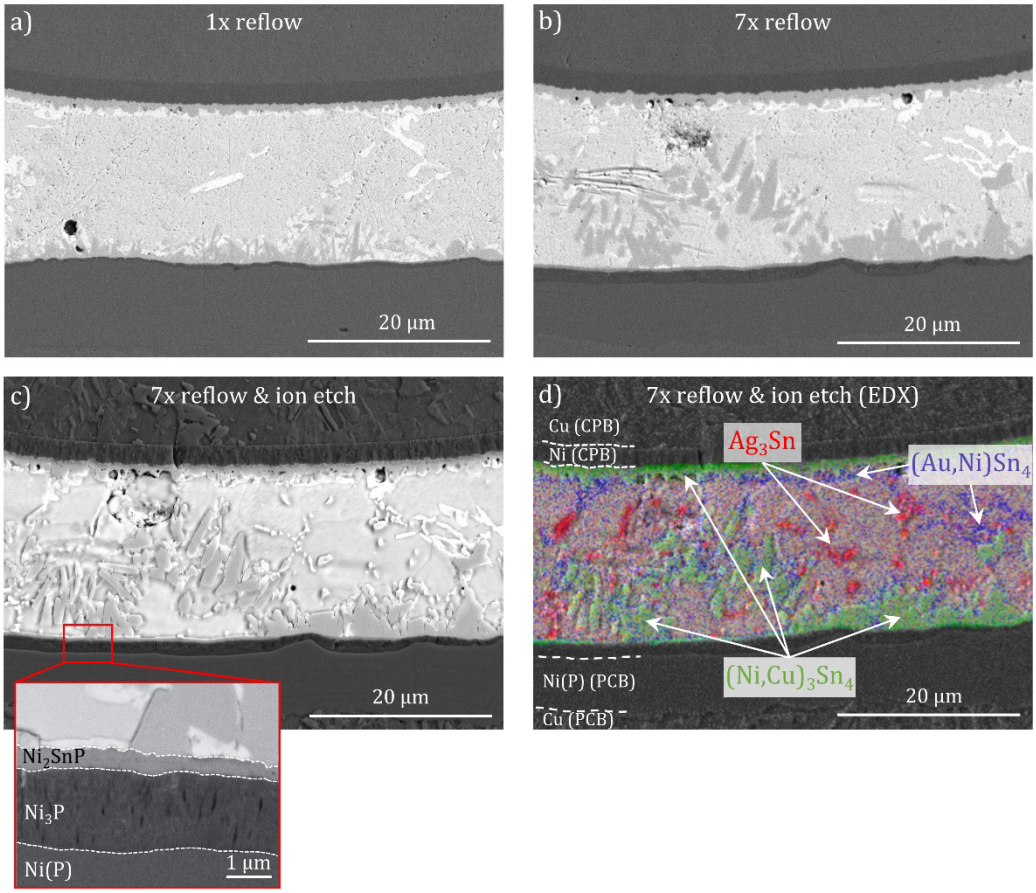


Fig. 65. SEM images of mechanical cross-sections from solder matrix taken with BSE detector. Upper image region corresponds to the CPB and the lower region to the PCB. In a) the IMC formation after assembly, i.e. after 1 reflow is shown. In b) the IMC formation after MSL 2a preconditioning, i.e. 7 reflows is shown and in c) the respective additionally ion etched cross-section image. The IMCs are more visible after ion etching. The inset in c) shows the electroless Ni barrier layer of the PCB and its IMCs detected by EDX. Due to Ni diffusion into the solder a phosphorous enriched Ni_3P layer with laminar voids was formed. A Ni_2SnP layer was identified above the Ni_3P layer. d) shows the cross-section of c) overlayed with an EDX element analysis mapping. Ag containing IMCs grains were only visible after ion etching. Green = $(Ni,Cu)_3Sn_4$, red = Ag_3Sn, blue = $(Au,Ni)Sn_4$. The dashed white lines indicate the interface between different material layers.

etching in the SEM image. In Fig. 65 d) a colored EDX elemental analysis mapping is overlapped with the SEM image in the solder matrix area. The EDX mapping shows Ni in green, Ag in red, and Au in blue. The exact elemental composition of the IMCs was revealed by single spot EDX analysis in the corresponding areas.

The IMCs $(Ni,Cu)_3Sn_4$, Ag_3Sn, and $(Au,Ni)Sn_4$ were identified. The Cu content in the $(Ni,Cu)_3Sn_4$ was found to be between 1-3 w%. The Cu content effects the IMC formation between Cu, Ni, and Sn, as high Cu contents lead to the formation of $(Cu,Ni)_6Sn_5$, which was however, not detected in these samples [59]. The Cu content of 1-3 w% in $(Ni,Cu)_3Sn_4$ matches well with the initial Cu content of 0.5 w% in the solder paste (SAC305) used for assembly. Ag_3Sn grains were identified with EDX mapping evenly distributed in the solder matrix after preconditioning. However, the Ag_3Sn grains were optically visible in SEM images only with additional ion etching of the surface. Prior assembly the Ni(P) of the landing pad is protected by a thin Au layer against oxidation to ensure good wettability during soldering. This Au layer is dissolved into the molten solder during reflow and precipitate as small $(Au,Ni)Sn_4$ grains. Multiple reflows led to a migration of the Au through the solder from the landing pad side towards the CPB as shown in Fig. 65 d).

The formation of $(Ni,Cu)_3Sn_4$ is faster at the electroless deposited Ni(P) layer of the PCB than at the electroplated Ni of the CPB. The electroplated Ni layer at the CPB side has a crystalline structure and the electroless Ni(P) has an amorphous structure as shown in Fig. 65 c). The electroless deposition process embeds P as an impurity from the reducing agent. The content of the co-deposited P impacts if a mixture of crystalline and amorphous, or only amorphous Ni(P) is deposited. The higher the P content, the more amorphous Ni(P) is deposited. With an increasing amount of P also the dissolution rate of Ni into the molten solder increases during the reflow. The higher concentration of dissolved Ni in the solder explains the higher IMC volume at the landing pad side. [60]

The inset of Fig. 65 c) shows the magnified image of the electroless Ni(P) layer at the landing pad side after 7 reflows. The dissolved Ni which formed the IMCs left a phosphorous enriched Ni_3P layer with elongated voids. Above the Ni_3P layer an

additional Sn containing thin Ni_2SnP IMC was detected. The Ni_2SnP is formed by Sn diffusion into the Ni_3P layer. The identified IMCs and the electroless Ni layer formation agrees well with the findings in the literature [61–65].

Significant mechanical deficiencies caused by IMCs or void formation were not observed as shown in 4.4.1 Die Shear Test (Solder Paste Assembly). The analysis revealed that the Ni barriers on both sides as well as the solder volume are considered sufficiently large not to be completely consumed or transformed through MSL 2a preconditioning reflows.

4.4.4 Dry Heat (Solder Paste Assembly)

The test vehicles for DH (150 °C) reliability were preconditioned (MSL 2a) prior testing but not flux cleaned. The minimum required test duration to pass the DH test is 504 h without failures for daisy chain and functional test vehicles. An overview of the minimum reliability requirements is given in Table 10. The samples A_fc(CPB65/REop38)_sp, A_dc(CPB65/REop38)_sp, and B_dc(CPB65/REop47)_sp were stressed with DH. All test vehicles were classified as passed. No failures were detected in any sample during the required and extended test duration. A detailed overview of the results is shown in Table 15. Each test vehicle consisted of 49 components soldered to the PCB.

Table 15. DH reliability test results of components with CPBs assembled with solder paste to the PCB. One functional and two daisy chain designs were tested. Each sample had 49 components soldered to the PCB. All designes were classified as passed. Minimum requiered DH (150 °C) duration without failure is 504 h.

Sample	Test	Passed components				
		Assembly 1st reflow	MSL 2a 7th reflow	144 h	504 h	2016 h
A_fc(CPB65/REop38)_sp	DH 150 °C	100 %	100 %	100 %	100 %	n.a.
A_dc(CPB65/REop38)_sp		100 %	100 %	100 %	100 %	100 %
B_dc(CPB65/REop47)_sp		100 %	100 %	100 %	100 %	100 %

The formation of IMCs in the solder matrix was investigated on mechanical cross-sections via SEM and EDX after various DH time durations. The aim of the analysis was to confirm a sufficient volume of remaining solder material and an

adequate remaining Ni barrier thickness after DH reliability testing. The results are shown in Fig. 66. The images in Fig. 66 a) and b) show the IMC formation after assembly with 1 reflow and MSL 2a preconditioning with 7 reflows. A more detailed IMC analysis of IMCs after preconditioning can be found in the previous chapter 4.4.3 Intermetallic Compound Formation by Preconditioning - Multiple Reflows. In Fig. 66 c), d), and e) the IMC formation until 1008 h of DH at 150 °C is shown. $(Ni,Cu)_3Sn_4$ was identified via EDX as the main IMC with a low Cu content of approx. 1-3 w%. The formation rate of $(Ni,Cu)_3Sn_4$ is high at the electroless Ni(P) layer of the PCB landing pad and low at the electroplated Ni layer at the CPB. After an extended duration of 2016 h DH two IMC phases were identified at the Ni barrier layers in the sample analyzed. Closer to the Ni layers $(Ni,Cu)_3Sn_4$ was detected with a Cu content of already 4-6 w%. Attached to $(Ni,Cu)_3Sn_4$ and closer to the remaining solder matrix $(Cu,Ni)_6Sn_5$ was detected as the second IMC phase by EDX. The $(Cu,Ni)_6Sn_5$ had a high Cu content of 20-22 w%. As already mentioned in the previous chapter, the Cu content inside the solder highly effects the IMC formation. High Cu contents lead to the formation of $(Cu,Ni)_6Sn_5$ instead of $(Ni,Cu)_3Sn_4$ [59]. The high Cu content cannot be explained by the initial Cu concentration of 0.5 w% in the solder paste. An additional Cu source must be present. The PCB landing pad Cu layer is fully enclosed by the Ni(P) layer. However, the CPB Cu base might get in contact with the solder paste if the assembly of the component is strongly misaligned. In rare cases this was observed and is shown in a micrograph of a mechanical cross-section in the inset of Fig. 66 f). Cu can then easily migrate into the solder. The micrograph clearly shows the strongly developed IMC at the side wall of the CPB Cu base. The side wall wetting was not visible in the cross-section plane investigated but side wall wetting might be present in an invisible plane. Manually performed optical microscopy inspections after assembly of all components on the test vehicles should have ensured that side wall wetting is not present. Nevertheless, in rare cases the sidewall wetting might have been still present. Furthermore, a starting crack formation at the interface of $(Cu,Ni)_6Sn_5$ and $(Ni,Cu)_3Sn_4$ is visible after the extended DH duration of 2016 h. However, it cannot be said with certainty if the two IMCs or an insufficient sample handling prior preparation for

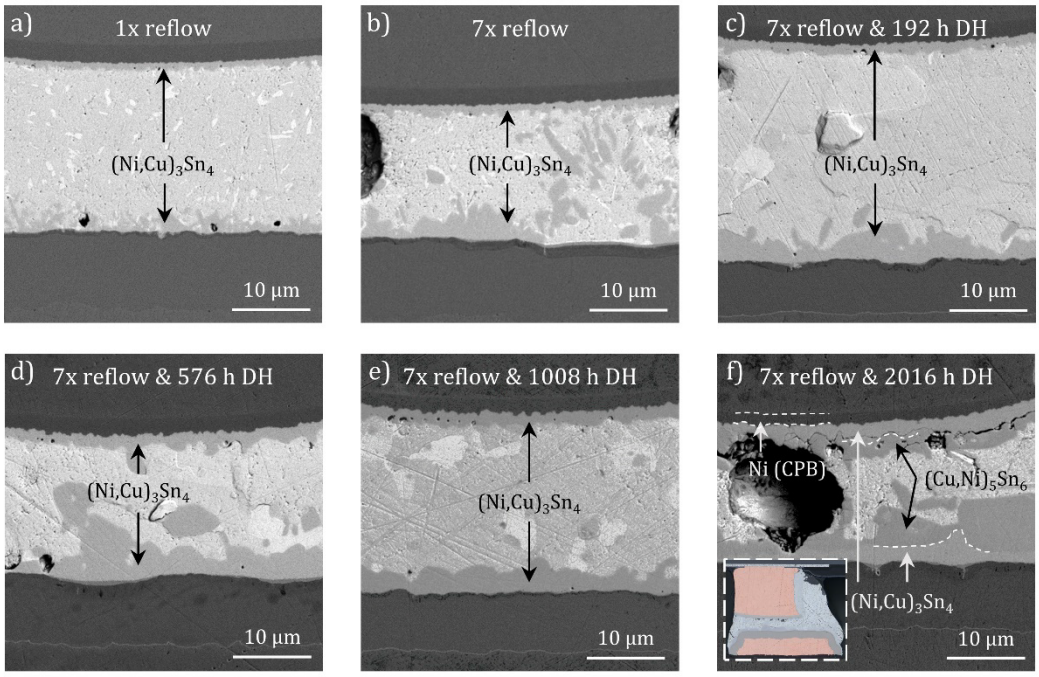


Fig. 66. SEM images of mechanical cross-sections to investigate the IMC growth during DH (150 °C) reliability testing. A large IMC volume forms during the 7 reflows of MSL 2a preconditioning shown in b). The main IMC formed is $(Ni,Cu)_3Sn_4$ in a), b), c), d), and e). The exception is f) where two IMC phases at the Ni barriers are visible. EDX analysis revealed the formation of $(Ni,Cu)_3Sn_4$ and $(Cu,Ni)_6Sn_5$ as labeled in f). $(Cu,Ni)_6Sn_5$ has a high Cu content (20-22 w%), which must come from an additional Cu source. A plausible Cu source would be the CPB Cu base wetted by solder as exemplified in the inset micrograph (dashed white frame) in f). However, even if this CPB side wall wetting was not present in the original examined plane of the cross-section, it might be still present in an invisible plane. The dashed white lines in f) indicate the interface of both IMCs and the remaining Ni thickness.

analysis caused this crack. The daisy chain component was still functional until analysis sample preparation. The Ni barriers at the PCB and the CPB side were still functional with a sufficient remaining thickness. The remaining solder volume was also sufficient to avoid a hard and brittle interface between the component and the PCB. This still enables plastic deformation in the solder joint during thermo-mechanical stress preventing cracks.

4.4.5 Temperature Cycling (Solder Paste Assembly)

This chapter contains TC reliability results of various designs, detected failure modes evoked by extended test durations, and IMC formation analysis of components assembled with solder paste. During TC the test vehicle is repeatedly stressed by an

alternating temperature of -40 °C and 125 °C each for 15 minutes. This induces thermo-mechanical stress especially at the CPB interconnections, which might cause a component failure after a certain number of TCs. The test vehicles were MSL 2a preconditioned and not flux cleaned after assembly. As well as all other test vehicles these components were tested open top, i.e. a mechanically supporting molded underfill was not applied prior testing. To pass the TC reliability test, components on the test vehicle must withstand 480x TCs and in addition the estimated failure probability must be lower than 5 % at 500x TCs. The statistical basics of the distribution analysis to estimate the failure probability are described in chapter 4.2 Statistical Fundamentals for Temperature Cycling Reliability Evaluation. In Table 16 the designs tested, and the respective TC results are listed. The daisy chain test vehicles were constantly monitored, which allowed to detect the exact number of TCs until component failure. The functional test vehicles were measured after a defined number of thermal cycles and compared to the initial reference measurement, which are both described in chapter 3.5 Component Failure Detection.

Table 16. Results of temperature cycling reliability test of components soldered with solder paste to the PCB. The components were repeatedly stressed with an alternating temperature of -40 °C and 125 °C for 15 minutes each, which equals one cycle.

Design (quantity tested)	**Test**	**Passed components**		
		Assembly 1st reflow	MSL 2a 7th reflow	Functional at 480x / failure probability at 500x TCs
A_fc(CPB65/REop38)_sp (146)	**TC** -40 °C / 125 °C 15 min dwell	100 %	100 %	100 % / < 5 %
A_dc(CPB65/REop38)_sp (97)		100 %	100 %	100 % / < 5 %
B_dc(CPB65/REop47)_sp (96)		100 %	100 %	100 % / < 5 %
C_dc(CPB65/REop27)_sp (43)		100 %	100 %	~ 60 % / > 5 %
D_dc(CPB55/REop28)_sp (46)		100 %	100 %	~ 60 % / > 5 %
E_dc(CPB75/REop48)_sp (47)		100 %	100 %	100 % / < 5 %

Two daisy chain designs (marked red in Table 16) with the smallest reinforcement opening diameters failed early during TC reliability because of a crack formation inside the EP-layer, which is described in detail later in this chapter. The remaining four designs passed the TC reliability testing. To estimate the failure probability, first a distribution analysis of the extended TC data was performed to fit the data sets best. The goodness of fit for each data set (design) is described with the AD* value based on the maximum likelihood estimation method for Weibull, Lognormal, Exponential, and Loglogistic distributions as listed in Table 17. The best fit is expected for the lowest AD* value, however, this is only valid for each data set by its own. The MTTF values are also listed in Table 17, i.e. the average time when a component failure is expected. According to the small variation of the AD* values, all distributions fit each data set well. However, the Weibull distribution resulted in the most conservative MTTF values for each data set, i.e. component failures are expected earlier with the Weibull distribution. The stricter MTTF evaluation is preferred and therefore Weibull distribution was used for failure probability estimations.

Table 17. Goodness of fit determination with maximum likelihood method for TC reliability data sets of components assembled with solder paste using Weibull, Lognormal, Exponential, and Loglogistic distributions. Weibull distribution is chosen to describe the components failure probability. Mean time to failure and the adjusted Anderson-Darling (AD*) value are displayed.

		Weibull	Lognormal	Exponential	Loglogistic
A_fc(CPB65/REop38)_sp	AD*	21.035	21.028	21.141	21.022
	MTTF	1961	2244	3063	2275
A_dc(CPB65/REop38)_sp	AD*	114.208	114.272	115.022	114.221
	MTTF	4111	4831	6836	4727
B_dc(CPB65/REop47)_sp	AD*	110.603	110.569	111.503	110.584
	MTTF	4047	4372	7013	4389
C_dc(CPB65/REop27)_sp	AD*	10.435	10.512	10.585	10.451
	MTTF	805	1027	847	1289
D_dc(CPB55/REop28)_sp	AD*	7.573	7.525	7.802	7.542
	MTTF	723	803	759	927
E_dc(CPB75/REop48)_sp	AD*	95.678	95.681	95.819	95.678
	MTTF	2979	3334	9111	3236

In total six different component designs assembled with solder paste to the PCB were stressed by TC. Five were daisy chain designs and one was functional. A detailed description of all component designs can be found in Table 9. The design A_fc(CPB65/REop38)_sp and A_dc(CPB65/REop38)_sp differ only in their functionality. Three CPB diameters (55 µm, 65 µm, 75 µm) and three different reinforcement (27 & 28 µm, 38 µm, 47 & 48 µm) opening diameters were included. The reinforcement design diameter difference of 1 µm is within the manufacturing variance and therefore considered insignificant.

Each data set was plotted in the cumulative failure probability plot shown in Fig. 67. The Weibull probability function is linearized in this graph by scaling the ordinate

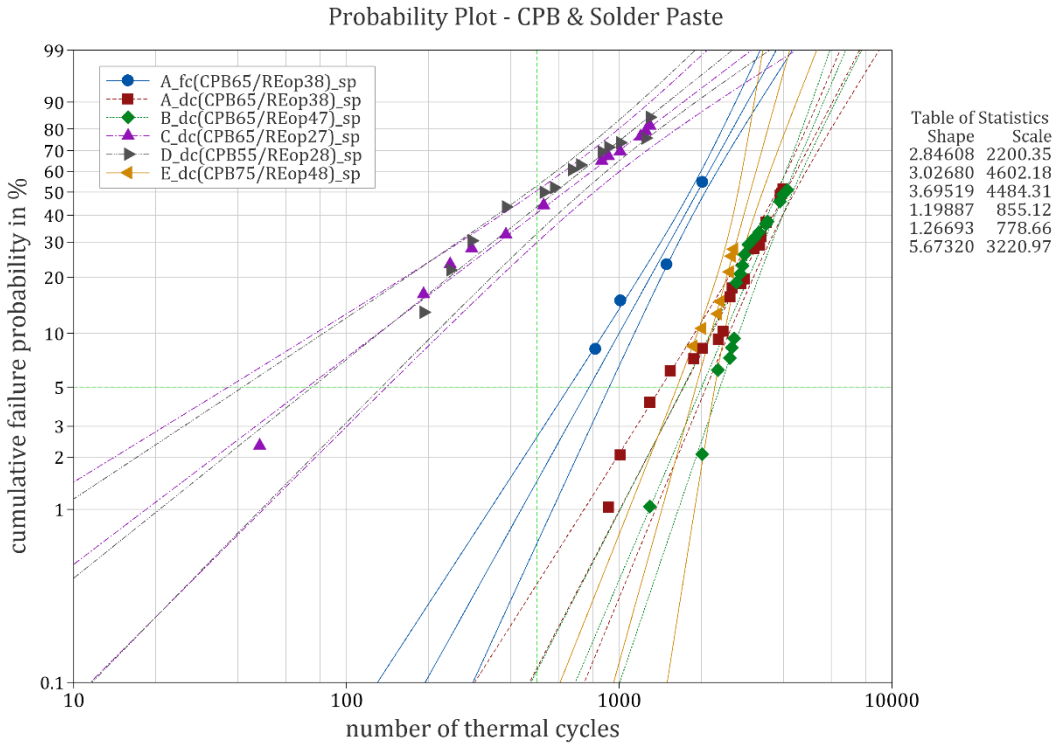


Fig. 67. Results of TC reliability testing as graph of Weibull cumulative failure probability vs. the number of thermal cycles. TC reliability testing was performed at -40 °C / +125 °C with 15 min dwell time each. Weibull distribution estimated using maximum likelihood method. A confidence interval of 90 % is illustrated for each plot. Components were assembled into solder paste. Five different daisy chain designs were tested and additionally one of them as functional test vehicle. Horizontal and vertical dashed green lines indicate the upper left quadrant which classifies a test vehicle as failed (failure probability < 5 % at 500 temperature cycles) if distribution plot passing through it. Sample designs C_dc(CPB65/REop27)_sp and D_dc(CPB55/REop28)_sp are classified as failed for TC reliability testing. The remaining designs are classified as passed including the functional test vehicle.

and abscissa accordingly (compare chapter 4.2). The confidence interval of 90 % is illustrated for each probability function. The designs C_dc(CPB65/REop27)_sp and D_dc(CPB55/REop28)_sp failed the TC reliability test because already approx. 40 % of the components failed at 480x TCs and also because the estimated failure probability is approx. 40 % at 500x TCs which is greater than the allowed maximum of 5 %. The failure modes were identified by C-SAM and mechanical cross-sections and will be discussed later in this chapter. The daisy chain designs A_dc(CPB65/REop38)_sp, B_dc(CPB65/REop47)_sp, and E_dc(CPB75/REop48)_sp passed the TC requirements. The estimated failure probability distributions overlap with their confidence intervals in large areas, which indicates only a slight difference in their TC reliability. The functional design A_fc(CPB65/REop38)_sp also passed the

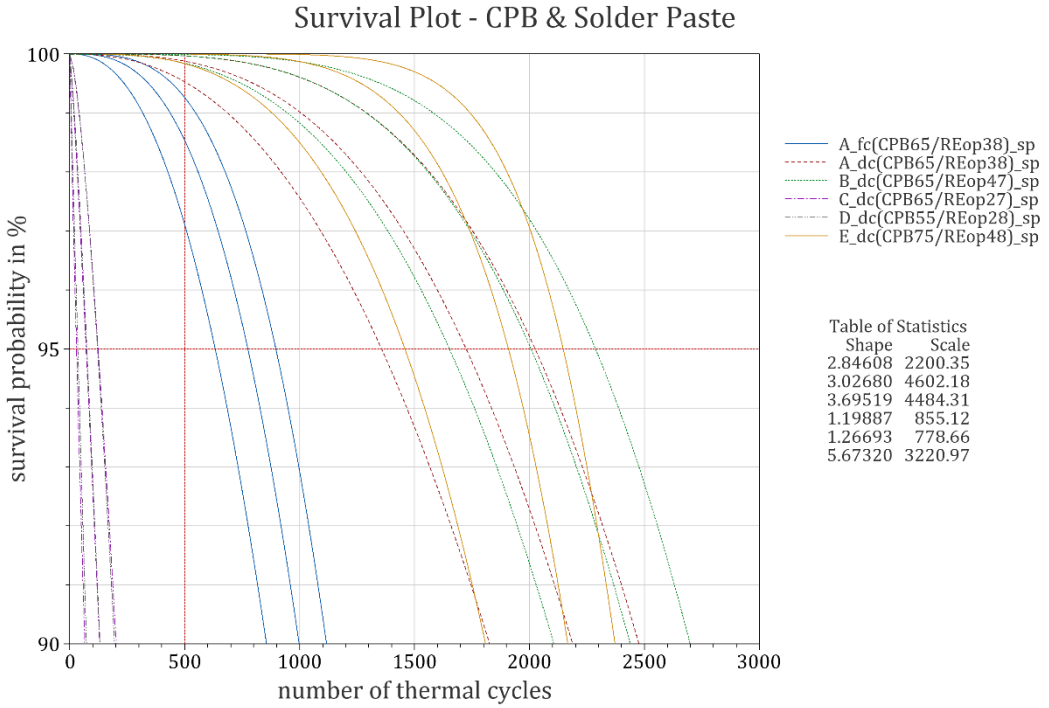


Fig. 68. Results of TC reliability testing as graph of Weibull survival probability vs. number of thermal cycles. TC reliability testing was performed at -40 °C / +125 °C with 15 min dwell time each. Weibull distribution estimated using maximum likelihood method. A confidence interval of 90 % is illustrated for each plot. Components were assembled into solder paste. The data relates to the graph in Fig. 67. Minimum requirement to pass TC reliability testing is a survival probability greater than 95 % at 500 temperature cycles (lower left quadrant in the graph indicated by red dashed lines).

TC reliability requirements but it is more sensitive to component failures as illustrated in Fig. 67. Comparing A_fc(CPB65/REop38)_sp and A_dc(CPB65/REop38)_sp which only vary in their functionality, it can clearly be seen that the failure detection for functional components is more sensitive because the RF-filter characteristics are assessed and not only the electrical resistance.

The requirement of a failure probability of less than 5 % at 500 TCs means the same as a survival probability of 95 % at 500 TCs. Fig. 68 shows the Weibull survival probability plot of all data sets. However, the information which can be retrieved from the cumulative failure and survival probability plot are the same. But the survival probability plot in Fig. 68 has a linear scale and refers only to the survival probability range of 90 % to 100 %, which might make it easier to interpret and compare the results at the early stage of TC reliability testing. The rf characteristic of functional

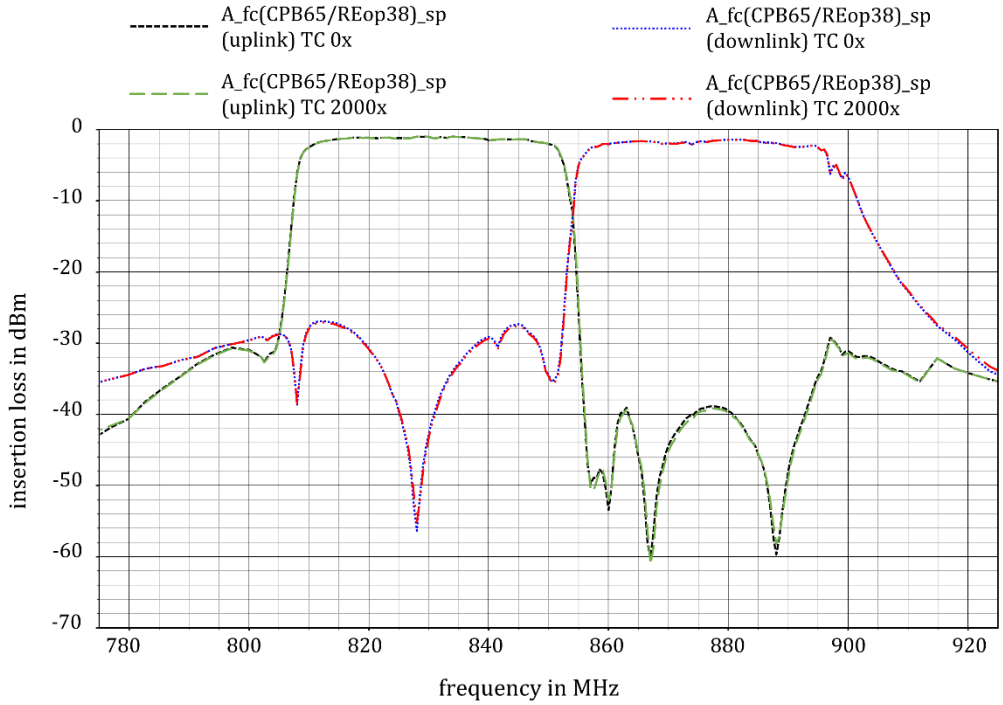


Fig. 69. Insertion loss vs. frequency of one representative A_fc(CPB65/REop38)_sp component measured after assembly (1 reflow) and 2000x TCs (including MSL2a preconditioning). LTE band 26 duplexer SAW RF-filter components were monitored. The components were only approximately matched to 50 Ω impedance with SMD inductors. The RF-filter characteristic of the shown component did not change after 2000x TCs at -40 °C and 125 °C for 15 minutes dwell time each.

components was measured after assembly as the reference and after a defined number of TCs. The rf characteristics were compared to the initial reference measurement according to the defined failure criteria explained in chapter 3.5 Component Failure Detection. In Fig. 69, the initial rf characteristic of one exemplary A_fc(CPB65/REop38)_sp component is compared to the measurement after a prolonged TC reliability stress test of 2000x TCs. The component was still functional.

The test vehicles were tested open top, i.e. no molded underfill mechanically supported the components. The significant and fast temperature change creates thermo-mechanical stress particularly to the CPB interconnection due to the CTE mismatch of the LN substrate and the PCB. The underfill, which is usually used in the final application, would distribute the thermo-mechanical stress to a larger area. The

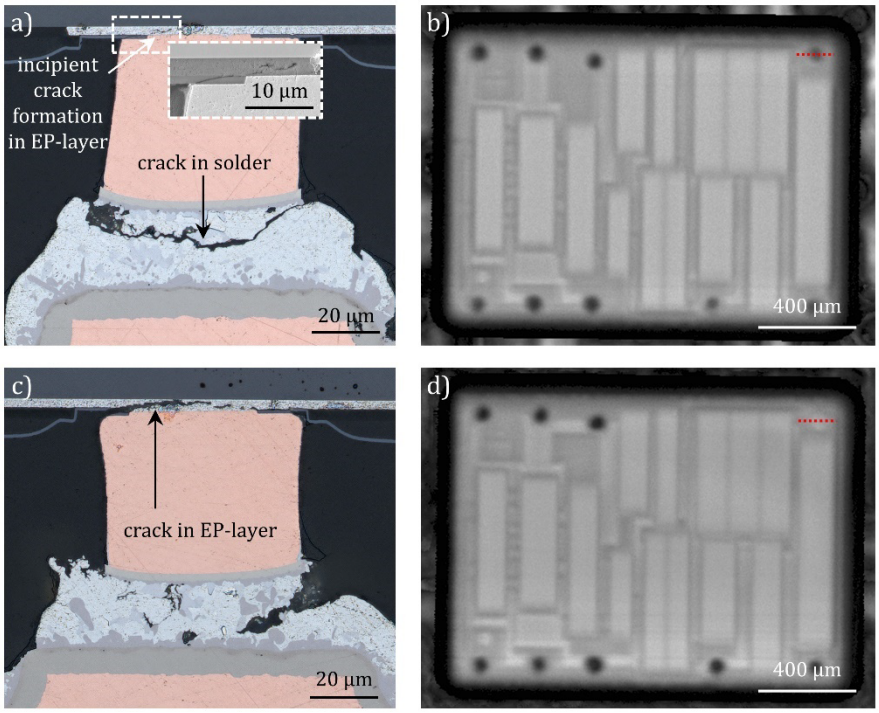


Fig. 70. Failure modes causes by TC reliability testing detected by microscopy at mechanical cross-sections and C-SAM. The first failure is a continuous crack through the bulk solder material as shown in a). In a) an incipient crack formation in the EP-layer and the reinforcement layer is visible and magnified in the SEM image inset. b) shows the corresponding C-SAM image of the component in a) prior mechanical cross-sectioning. The second failure mode is a continuous crack through the reinforcement and EP-layer as shown in c). d) shows the corresponding C-SAM image of the component in c) prior mechanical cross-sectioning. The C-SAM image shows a "white" CPB, which is caused by the crack in the EP-layer and the resulting high reflectance of the ultrasound.

experience with similar built-up test vehicles showed an increased TC reliability of several factors when applying a underfill. However, the missing underfill allows a faster evaluation of the TC reliability.

Two different failure modes were identified during component analyses by C-SAM (C-mode scanning acoustic microscope) and SEM/optical microscopy investigations on mechanical cross-sections of CPB interconnections. First failure mode was a continuous crack through the bulk solder material and the second failure mode was a continuous crack through the EP-layer. Both failure modes are illustrated in Fig. 70. C-SAM allows to create an image by scanning the component with ultrasound. It is a nondestructive method to detect cracks or delamination. Using high frequencies allows to create images with a resolution in the lower micrometer range based on the time-dependent detection of reflected ultrasound signals. The nondestructive method was used to detect cracks and delamination in the electrical path layer and the reinforcement layer at the CBP base. Therefore, the ultrasound was coupled into the component from the top side of the component, which then passed through the LN, and the EP-layer followed by the reinforcement layer or the CPB Cu base in the region of interest. The time-dependent partly reflected ultrasound signal was detected and translated into an image. These are grayscale images, where bright areas indicate a high level of sound reflection and dark areas a low level of reflection. High reflection levels are caused by material change interfaces and most pronounced if the material is not connected to another solid material (almost total reflection) in the direction of the sound. Therefore, cracks or delamination can be spotted very well even in large scan areas in a defined depth by setting ultrasound runtime gates. However, this technique has its limitations and the C-SAM tool used for investigation was unfortunately inappropriate to resolve possible cracks in the solder material, as the signal to noise ratio did not result in a usable image.

C-SAM analyses were further used to investigate which failure mode was the dominant for each design during TC reliability tests. Therefore, test vehicles of every design were scanned by C-SAM after a defined number of TCs and the number of components with “white” CPBs were detected. The results are listed in Table 18.

Table 18. Components detected with "white" CPBs related to the number of thermal cycles in comparison with the component failure probability. Two failure modes were detected, first the crack in the bulk solder (FM 1) and second the crack inside the EP-layer called "white" CPB (FM 2). The comparison of the component failure probability with the number of components with "white" CPBs, i.e. crack in the EP-layer, allows the evaluation of the dominant failure mode for each design.

Design	MSL 2a & number of TCs	Components with "white" CPB	Components failure probability	Dominant failure mode
A_dc(CPB65/REop38)_sp A_fc(CPB65/REop38)_sp	1344x	1 %	4 % (dc) / 22 % (fc)	FM 1
	2016x	1 %	8 % (dc) / 55 % (fc)	FM 1
	4128x	39 %	52 % (dc) / 99 % (fc)	FM 1 & FM 2
B_dc(CPB65/REop47)_sp	4128x	6 %	51 % (dc)	FM 1
C_dc(CPB65/REop27)_sp	1536x	96 %	90 % (dc)	FM 2
D_dc(CPB55/REop28)_sp	1536x	95 %	92 % (dc)	FM 2
E_dc(CPB75/REop48)_sp	2640x	0 %	28 % (dc)	FM 1

With the designs A_dc(CPB65/REop38)_sp and A_fc(CPB65/REop38)_sp, "white" CPBs are visible after more than 2016x TCs. The failure probability is higher for the functional design, which is more sensitive to the failure detection. However, probably below 2016x TCs a crack in the solder is the dominant failure mode and with increasing TCs the crack in the EP-layer additionally causes further components to fail.

The design B_dc(CPB65/REop47)_sp has also a CPB diameter of 65 µm but a larger reinforcement opening diameter of 47 µm. B_dc(CPB65/REop47)_sp has a similar failure probability as A_dc(CPB65/REop38)_sp but shows significantly lower "white" CPBs of only 6 % at 4128x TCs. Hence, the dominant failure mode is a crack through the bulk solder material. This can be explained by the lower mechanical stress caused by the larger interface of the CPB Cu base and the EP-layer due to the larger reinforcement opening. However, for daisy chain components the larger reinforcement opening and the resulting dominant failure mode with a crack in the bulk solder did not result in a lower component failure probability.

C_dc(CPB65/REop27)_sp and D_dc(CPB55/REop28)_sp have the smallest reinforcement opening diameter of 27 µm and 28 µm, and a CPB diameter of 65 µm and 55 µm, respectively. Both designs failed early, and the C-SAM analysis revealed that almost every component had multiple "white" CPBs after 1536x TCs. Hence, a

crack inside the EP-layer was the dominant failure mode. The small interface of the CPB Cu base and the EP-layer caused higher mechanical stress due to the missing stress distribution into the EP-layer. For both designs, the CPB diameter had no significant influence on the failure probability.

E_dc(CPB75/REop48)_sp has a large reinforcement opening diameter of 48 µm and the largest CPB diameter of 75 µm. At 2640x TCs no component with a "white" CPB was detected but a failure probability of 28 %. Hence, the main failure mode was a crack through the bulk solder. The failure probability plot for E_dc(CPB75/REop48)_sp appears steeper than the other daisy chain designs, i.e. the failure probability raises later but faster. Above approx. 2600 TCs the failure probability of E_dc(CPB75/REop48)_sp is higher than for other daisy chain designs.

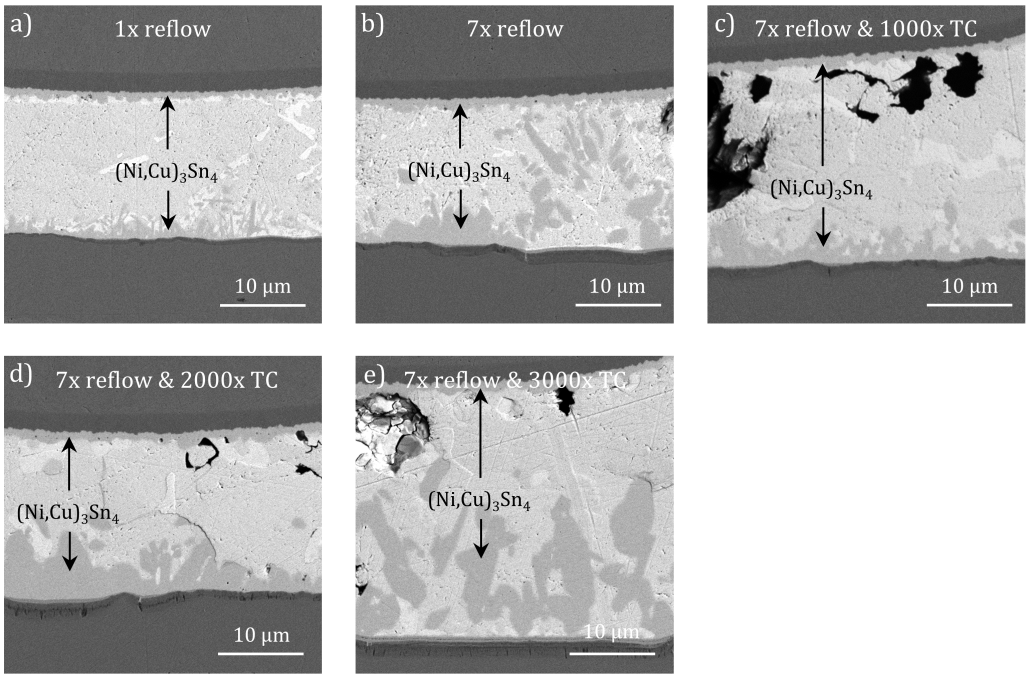


Fig. 71. IMC formation during prolonged TC reliability testing investigated via SEM images of mechanical cross-sections. In a) the IMC formation after assembly and in b) after MSL 2a preconditioning (7x reflow). A large IMC volume increase can be seen after 7 reflows. However, even after 1000x, 2000x, and 3000x TCs still solder and Ni diffusion barriers remain, as shown in c), d), and e), respectively. The main IMC formed was $(Ni,Cu)_3Sn_4$ with a low Cu content of 1-3 w% identified by EDX. $(Cu,Ni)_6Sn_5$ was not detected in the samples investigated. IMC formation at the electroless Ni(P) (landing pad side) is faster than at the electroplated Ni (CPB side). Laminar voiding in the electroless Ni(P) layer is present.

One cause could be the mechanically stiffer structure due to the large reinforcement opening combined with the large CPB diameter of 75 µm resulting in higher mechanical stress and strain in the solder material.

The IMC formation caused by TC was investigated via SEM and EDX analyses on mechanical cross-sections after a defined number of TCs. The investigation of the IMC formation during TC reliability testing is crucial to ensure remaining solder material and Ni diffusion barriers to avoid the formation of exclusively stiff and brittle IMCs in the CPB interconnections to prevent a negative impact on the reliability. Detailed results of the IMC formation after MSL 2a preconditioning including an ion beam etch to make IMCs better visible was discussed in chapter 4.4.3 Intermetallic Compound Formation by Preconditioning - Multiple Reflows. Fig. 71 shows the SEM images of IMCs formed after assembly, preconditioning, 1000x TCs, 2000x TCs, and 3000x TCs. The IMC volume increases with the number of TCs. EDX analysis revealed $(Ni,Cu)_3Sn_4$ as the main IMC with a Cu content of 1-3 w%. It has already been noted in chapter 4.4.3 and 4.4.4 that the IMC formation at the CPB side with the electroplated Ni barrier layer is slower than at the landing pad electroless deposited Ni(P) layer. Laminar voiding was again detected in the electroless Ni(P) layer which, however, did not cause any reliability issues by cracks through the interface.

4.5 Results of Former Solder Bump Components (Flux Assembly)

An identical design but with the former solder bump (SB) interconnection design assembled with flux was also stressed open top, i.e. without underfill, by DHSS, uHAST, DH, and TC with same test conditions for comparison. The SBs had a diameter of 140 µm and the component size was also 1.20 x 1.60 mm^2. Only a functional version was tested. The laminar structure of the PCB for SB components was equally designed to the PCB for CPB components. Beside the exact component dimensions, the thermo-mechanical characteristics of both PCB types were equal and therefore

suitable for a direct reliability comparison. However, the ENIG landing pad was round and in an appropriate size for the 140 µm diameter SBs. A detailed investigation of the SB interconnection technology was not aimed in this work, therefore, a failure analyses was not performed and only a brief summary of the reliability results is given. The test vehicles were flux cleaned prior testing. The functional design with SB interconnections passed the reliability requirements of DHSS, uHAST, DH, and TC. The prolonged TC reliability test of components with SBs revealed a Weibull failure probability in between the functional and daisy chain components with CPB interconnections as shown in Fig. 72. The MTTF was estimated with 2230x TCs using the Weibull distribution and maximum likelihood method. However, above approx.

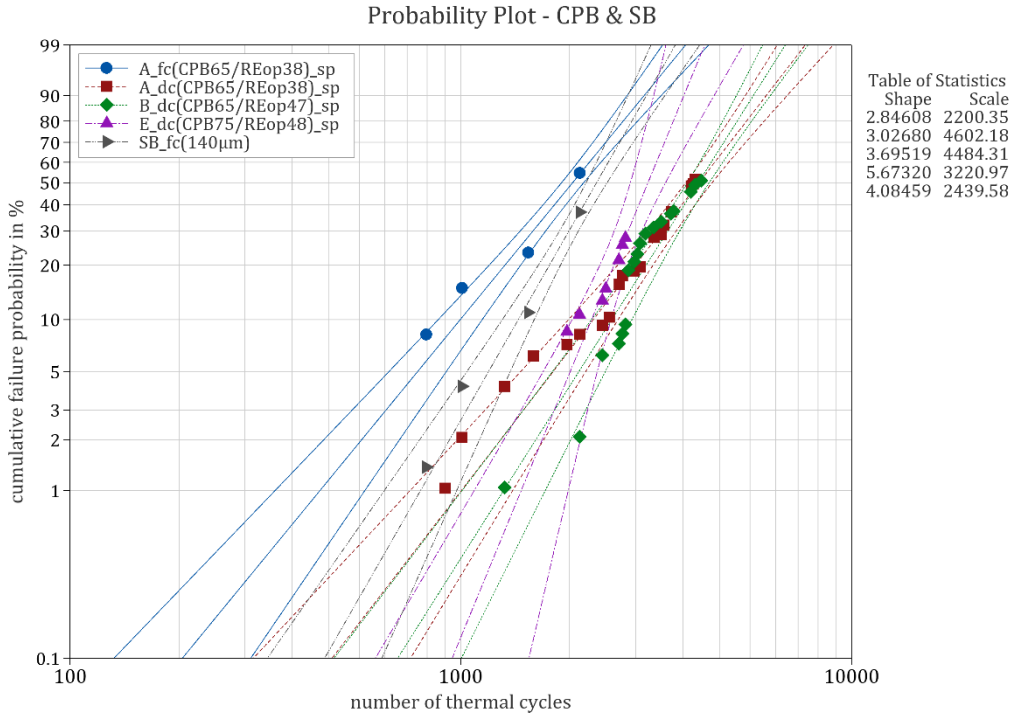


Fig. 72. Results of TC reliability testing with CPBs and SBs as graph of Weibull cumulative failure probability vs. the number of thermal cycles. TC reliability testing was performed at -40 °C / +125 °C with 15 min dwell time each. Weibull distribution estimated by using the maximum likelihood method. A confidence interval of 90 % is illustrated for each plot. Components with CPBs were assembled into solder paste and components with SBs were assembled into flux. Four CPB designs (3 daisy chain & 1 functional) and one functional SB design SB_fc(140µm) is plotted. All designs passed the TC requirements. The SB design SB_fc(140µm) is slightly better in TC reliability than the functional CPB design A_fc(CPB65/REop38)_sp, however, above approx. 2100x TCs the confidence intervals start to overlap.

2100x TC the confidence interval of the functional CPB design and the functional SB design start to overlap. Statistics and failure detection were carried out in the same way as in the previous chapters.

4.6 Summary and Classification of Reliability

Various designs of components with CPBs and two assembly methods (flux & solder paste) were tested by main reliability tests for electronic components. The flux assembly method for CPB components has proven to be unsuitable due to poor solderability and the resulting interconnection failures in various reliability tests. Two CPB designs with small reinforcement opening diameters assembled into solder paste showed early component failures during the TC reliability testing due a continuous crack through the EP-layer induced by thermo-mechanical stress. As expected, the initial interconnection technology with solder bumps assembled with flux passed the requirements on reliability testing.

The same applied to the functional and daisy chain CPB technology target-design A_fc(CPB65/REop38)_sp and A_dc(CPB65/REop38)_sp, and the daisy chain design variation B_dc(CPB65/REop47)_sp, assembled into solder paste as these designs passed all required reliability tests (DHSS, uHAST, DH, and TC). A flux cleaning step prior uHAST testing is mandatory to prevent corrosion below the CPB Cu base. The daisy chain design variation E_dc(CPB75/REop48)_sp was only tested by TC reliability and also classified as passed.

Most critical reliability test performed for the CPB interconnections was the TC test, because of the high thermo-mechanical stress transferred to the CPB interconnection due to the CTE mismatch of the large size component and the PCB. This was further amplified by the open top testing, i.e. without a mechanically supporting underfill. It was shown that early component failures during TC were caused by a too small reinforcement opening diameter (27 µm & 28 µm) and the resulting crack through the EP-layer. However, as of a certain reinforcement opening diameter (38 µm) the TC reliability stayed constant even with a larger reinforcement

opening diameter (47 µm & 48 µm) and independent from the CPB diameter (65 µm & 75 µm). But the distribution of the two detected failure modes shifted. With a reinforcement opening diameter of 38 µm a continuous crack through the solder was the dominant failure mode until approx. 2100x TCs. By further prolonging the TC testing the second failure mode which is a continuous crack through the EP-layer occurs simultaneously. With a larger reinforcement opening (47 µm & 48 µm) and with a larger CPB diameter (75 µm) only the continuous crack through the bulk solder was dominant.

The IMC formation during the MSL 2a preconditioning, DH, and TC was analyzed by SEM and EDX. $(Ni,Cu)_3Sn_4$ was detected as the main IMC with a low Cu content. In case of the prolonged DH storage in one sample the IMC $(Cu,Ni)_5Sn_6$ with a high Cu content was detected. Solder wetting the CPB Cu base is the most likely additional Cu source causing this faster forming IMC. Nonetheless, in the prolonged test conditions of DH and TC there was still enough solder and Ni barrier remaining.

5 Summary, Conclusion & Outlook

In this work SBs on RF-filter components with a TFAP were successfully replaced by CPBs as a new space-saving interconnection technology. The package layout was redesigned to comply with the CPBs. The micro-acoustic structures and the TFAP for RF-filter components were manufactured with already existing wafer-level manufacturing processes. However, the wafer-level processes for CPB manufacturing on TFAPs were newly developed. Each wafer contained various designs.

The following process sequence was developed: After the manufacturing of the micro-acoustic structures and the TFAP a thin 50 nm Ti adhesion layer followed by a 200 nm thick Cu layer was deposited on the whole wafer by PVD. Both layers form the electrically conducting seed layer for the later electroplating process. Photolithography with a chemically amplified positive tone thick-film resist defined the position of the intended CPBs. The liquid photoresist was applied by spin coating and dried (softbake) on proximity hotplates. A minimum film thickness of 80 µm was achieved even on the distinctive TFAP topology. The photoresist was exposed by UV-light through a photomask in a mask aligner tool. The sidewall shape of the positive tone photoresist openings depends on the softbake duration. An almost vertical sidewall shape was achieved by a softbake duration of 480 s at 135 °C. The impact of the exposure dose, the post exposure bake duration, and the number of development puddles on the photoresist opening diameter was investigated by a DoE. The DoE allowed to set the lithography parameters inside a well understood process window to achieve a stable photoresist opening diameter. The exposure dose was set

to 1200 mJ/cm^2 followed by the PEB for 100 s at 100 °C. Five puddles with aqueous TMHA solution for 60 s each developed the openings in the photoresist. The smallest achievable structure for a film thickness of 80 µm was a diameter of 25 µm and a feature-to-feature distance (pitch) of 20 µm.

A plasma cleaning process after photolithography ensured a good mechanical connection of the electroplated CPBs to the Cu seed-layer. The cleaning efficiency was evaluated by shear tests of electroplated Cu posts. Excellent results were achieved with the commercial plasma tool B using a gas composition of O_2/CF_4, an IC power of 500 W, and a CC power of 50 W. The active wafer cooling was set to 16 °C with a plasma time duration of 45 s. The plasma process had no negative impact on the positive tone photoresist. Cu, Ni, and SnAg were subsequently deposited via electroplating using commercial electrolytes and tools. Afterwards the photoresist was removed in a batch spray cleaner tool.

The 200 nm Cu seed-layer was wet-etched in a spray tool with a potassium iodide (KI) and iodine (I_2) solution. The formed copper iodide (CuI) was removed by an aqueous ammonia solution. The 50 nm Ti layer was etched by an aqueous ammonium bifluoride solution. The over-etch at the CPB Cu base was only 0.7 µm. The Ti under-etch was detected to be 1.5 µm via FIB-SEM analysis. Sufficient results for the solder cap reflow were achieved by wafer fluxing, a reflow in a continuous furnace, and a wafer flux residue clean. The components were singularized by DBG. First the front side was half-cut diced followed by a backside grind until reaching the grooves from the topside which singularized the wafer. The components were transferred to a frame. Specific components were picked from the frame and placed into a standard tape & reel.

The RF-filter components with CPBs and their passive SMDs were assembled by a pick & place tool on either functional or daisy chain test PCBs for reliability testing. The failure detection during reliability testing was based on RF-characteristic changes measured by a network analyzer for functional components or on a simple electrical resistance monitoring for daisy chain components.

The components with CPBs were assembled into flux or into solder paste. The components with CPBs which were assembled into flux failed the reliability test requirements. Particularly during TC reliability testing many components failed early which was caused by poor soldering of the CPBs to the PCB.

However, components with CPBs assembled into screen printed solder paste showed excellent solderability. Die shear testing confirmed via the detected failure modes that the target design A_fc(CPB65/REop38)_sp had a sufficient mechanical connection to the PCB. The failure modes detected were a shear off within the bulk solder or within the EP-layer. A shear off within the EP-layer resulted in higher shear forces than within the bulk solder. The shear forces related to the failure modes prove an excellent mechanical connection of the components with CPBs to the PCB. A prolonged DH storage at 150 °C until 1008 h did not result in a significant shear force chance. However, after 2008 h DH a moderate shear force increase was detected.

The requirements of the main reliability tests DHSS, uHAST, DH, and TC were fulfilled with the functional target design A_fc(CPB65/REop38)_sp and the daisy chain designs A_dc(CPB65/REop38)_sp, and B_dc(CPB65/REop47). After the prolonged TC reliability testing two failure modes were detected by component analyses. The first failure mode was a continuous crack through the bulk solder and the second failure mode was a continuous crack through the EP-layer. The dominant failure mode caused by prolonged TC testing dependents on the reinforcement opening diameter. The smaller the opening the likelier is a crack inside the EP-layer. However, the minimum reinforcement opening diameter of the components tested was 38 µm to prevent early failures during TC reliability testing.

The main IMC formed after MSL 2a preconditioning, prolonged DH and TC was $(Ni,Cu)_3Sn_4$ with a Cu content of approx. 1-3 w%. However, $(Cu,Ni)_5Sn_6$ with a high Cu content was found to be the main IMC in one DH (2016 h) sample. Solder wetting on the sidewall of the CPB Cu base was identified as additional Cu source causing the $(Cu,Ni)_5Sn_6$ IMC formation. The IMC formation at the landing pad's electroless Ni(P) is faster than at the electroplated crystalline Ni layer at the CPB side due to the higher solubility of the amorphous Ni(P) into the molten solder during preconditioning.

Nonetheless, even after seven reflows (preconditioning) and the prolonged testing, enough solder material and Ni diffusion barrier remained.

The target design A_fc(CPB65/REop38)_sp already fulfilled the main reliability and performance requirements for RF-components and the other design variations tested led to an understanding of vulnerabilities and possible improvements. However, to accelerate the evaluation of possible new designs and improved material combinations it is recommended to implement reliability simulations by e.g. finite elements method and adapt the simulation models to components already tested. The simulations would allow the most promising designs and material combinations to be selected from a large number of options in order to manufacture and test them. The simulations would be particularly suitable to improve TC reliability.

In summary, this work proved that CPBs are a suitable replacement of SBs as interconnection technology on micro-acoustic RF-components with a TFAP in terms of wafer-level manufacturing as well as component reliability and performance. CPBs not only promote a significant component size reduction and a new RF-filter design freedom but also associate a significant cost of ownership advantage over the previous SB technology. Therefore, RF-filter components with a TFAP and CPBs are a further step towards component miniaturization and cost reduction still meeting the high performance and reliability standards.

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List of Abbreviations

AD*	Anderson-Darling
Ag	silver
Al	aluminum
ANOVA	analysis of the variance
ANT	antenna
Au	gold
BSE	back scattered electron
CC	conductively coupled
cdf	cumulative distribution function
CPB	copper pillar bump
CSSP	chip sized SAW (surface acoustic wave) package
CTE	coefficient of thermal expansion
Cu	copper
DH	dry heat (reliability test)
DHSS	damp heat steady state (reliability test)
DMSO	dimethyl sulfoxide
DoE	design of experiment
DSSP	die sized SAW (surface acoustic wave) package
EBR	edge bead removal
EDX	energy dispersive X-ray
ENIG	electroless Ni, immersion Au
EP	electrical path
ESD	electrostatic discharge
FDD	frequency division duplexing
Fe	iron
FMEA	failure mode and effects analysis
H	hydrogen
HCOOH	formic acid
HMDS	hexamethyldisilazane
HTCC	high temperature cofired ceramic
I	iodine
IC	inductively coupled
IEF	impedance element filter
IMC	intermetallic compound
JEDEC	joint electron device engineering council
KI	potassium iodine

LCR	longitudinal coupled resonators
LN	lithium niobate, $LiNbO_3$
LT	lithium tantalate, $LiTaO_3$
LTCC	low temperature cofired ceramic
MSL 2a	moisture sensitivity level 2a
MTTF	mean time to failure
N	nitrogen
Ni	nickel
P	phosphorus
PAG	photoacid generator
PCB	printed circuit board
PEB	post exposure bake
PGMEA	1-methoxy-2-propanol acetate
prepreg	pre-impregnated fibers with polymer matrix
PVD	physical vapor deposition
redox	reduction and oxidation
RFFE	radio frequency front end
RH	relative humidity
RX	receiver signal
SAC	Sn-Ag-Cu, tin-silver-copper alloy
SB	solder bump
SB	solder bumps
SEM	scanning electron microscopy
Si	silicon
SMD	surface mounted device
Sn	tin
TC	temperature cycling (reliability test)
TCR	transversely coupled resonators
TFAP	thin film acoustic package
TFSAW	thin film surface acoustic wave
Ti	titan
TMAH	tetramethylammonium hydroxide
TX	transmitter signal
uHAST	unbiased highly accelerated stress test (reliability test)
UV	ultraviolet
XRF	X-ray fluorescence

LIST OF PUBLICATIONS

5) C. Eulenkamp, J. Schober, and G. Feiertag, "Analysis of copper pillar bump interconnects for RF-filters," *Microelectronics Reliability*, vol. 138, p. 114642, 2022, DOI: https://doi.org/10.1016/j.microrel.2022.114642.

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APPENDICES

Table 19. Shear force values in [mN] of Cu posts after different plasma cleaning treatments.

Shear forces in [mN] of Cu posts after different plasma cleaning treatments											
A-1.1-O2-25s	A-1.2-O2-50s	A-1.3-O2-75s	B_1.1-Ar/O2-30s	B_1.2-Ar/O2-60s	B_1.3-Ar/O2-90s	B_2.1-O2/Ar-30s	B_2.2-O2/Ar-60s	B_2.3-O2/Ar-90s	B_3.1-O2/CF4-30s	B_3.2-O2/CF4-60s	B_3.3-O2/CF4-90s
116	74.98	177.29	778.13	669.13	817.86	392.42	885.17	848.63	811.92	844.85	804.83
101.07	106.25	133.3	773.83	702.7	782.71	389.7	863.16	852.37	801.79	829.06	812.52
80.58	86.64	138.59	783.76	717.86	777.22	394.6	860.01	854.71	817.27	827.65	817.61
83.55	58.48	140.41	797.2	689.69	785.49	386.52	859.52	849.38	811.8	831.06	813.99
91.42	59.11	115.8	778.27	678.8	780.71	393.18	864.03	859.24	812.37	819.59	816.23
78.42	81.22	123.95	785.8	719.42	773.67	400.97	860.73	844.89	804.16	813.76	797.36
87.78	60.45	120.25	788.23	685.54	767.77	388.05	868.16	849.45	796.04	810.82	804.97
78.00	72.54	132.92	775.13	676.1	770.41	400.51	867.56	856.91	793.19	819.12	811.95
80.01	92.22	152.08	772.25	688.43	778.29	382.83	859.58	849.57	796.68	797.87	801.17
84.13	172.77	124.88	772.01	711.12	778.55	400.46	857.24	838.76	801.11	801.84	797.26
78.87	74.38	123.82	775.94	695.02	774.7	420.38	866.42	850.88	790.53	810.76	795.09
85.5	66.08	93.41	778.29	691.77	766.6	425.47	868.69	842.48	792.91	823.02	801.17
80.41	91.5	116.61	775.94	695.02	780.82	421.33	823.93	758.43	789.78	802.68	801.99
79.44	174.59	98.86	780.64	691.23	778.69	434.44	832.58	846.13	799.72	801	796.81
76.79	182.17	99.1	776.15	720.92	773.93	448.29	828.94	851.03	795.53	802.03	801.78
95.39	88.18	114.35	771.37	730.48	771.33	437.01	847.03	852.57	789.21	795.85	806.29
79.16	40.29	150.26	777.93	712.14	773.96	425.19	851.11	861.11	799.03	808.09	803.09
102.84	41.86	109.83	777.42	725.03	782.65	424.58	858.81	843.32	810.96	808.18	813.28
51.7	41.23	56.79	750.1	657.25	754.34	566.03	846.97	841.49	780.26	807.97	831.13
75.55	43.73	49.84	746.51	645.26	761.13	580.18	870.09	842.14	789.77	812.16	825.65
84.35	55.66	48.96	753.02	664.26	763.43	575.22	857.17	836.84	766.64	820.84	822.5
62.97	42.41	47.27	763.04	685.45	761.33	567.11	862.4	839.56	777.12	821.76	840.6
86.45	58.22	40.66	752.5	659.17	764.62	550.11	847.35	837.57	778.81	831.59	858.11
54.5	41.42	49.05	751.27	687.9	761.11	559.1	861.71	840.26	781.2	812.78	856.47
48.05	42.01	52.11	749.45	651.84	760.45	563.62	862.62	832.26	777.73	821.04	846.84
44.98	52.79	38.5	748.11	687.95	761.44	588.53	860.46	843.79	788.6	814.38	858.11
85.37	33.58	61.13	758.72	661.34	766.13	568.8	859.98	860.24	785.31	819.92	812.28
71.36	46.98	40.4	757.48	699.36	765.19	572.15	853.47	824.89	783.4	824.12	802.72
41.03	83.69	55.61	754.03	673.65	769.96	524.38	858.47	830.65	786.86	820.09	816.48
57.42	91.44	53.08	742.32	679.9	767	524.98	848.54	828.9	783.32	822.85	814.95
66.25	154	44.16	749.12	687.03	768.28	536.42	858.41	833.15	795.93	812.34	808.88
45.33	186.69	50.39	806.59	675.54	769.62	531.67	854.07	844.94	800.18	828.62	793.56
39.42	195.96	46.51	806.36	688.33	747.18	526.54	859.25	841.96	791.6	824.38	802.31
61.46	62.2	44.91	820.05	666.92	757.05	524.89	854.11	841.04	796.13	817.85	815.57
59.25	69.63	64.72	810.93	653.51	773.04	543.23	856.53	831.94	802.4	822.06	802.85
14.41	74.88	56.1	792.66	663.66	766.65	541.28	862.66	832.39	789.06	833.36	808.32
73.9	67.79	115.61	700.51	604.11	727.11	359.62	817.14	821.68	733.02	802.02	762.67
62.43	84.66	97.19	700.94	604.88	733.76	378.48	822.77	831.08	746.74	771.07	767.13
63.46	92.83	92.06	700.21	600.08	729.91	375.07	819.48	815.71	745.84	779.12	768.08
95.32	47.37	113.19	689.82	630.41	730.26	372.82	819.32	831.7	761.3	776.41	776.85
84	50.75	98.41	696.16	599.46	732.52	378.6	809.45	817.64	758.33	785.24	794.35
49.64	54.34	98.33	699.53	583.8	760.85	365.21	810.51	823.33	776.18	799.44	803.02
87.01	94.67	89.12	693.33	589.19	768.29	368.71	801.91	831.55	738.85	805.31	786.36
51.21	99.53	111.87	710.8	577.16	765.69	364.1	808.84	823.99	747.92	801.62	801.14
88.44	72.69	109.98	701.61	575.95	724.93	365.46	813.57	820.63	758.29	795.12	787.91
80.8	67.58	102.85	693.09	591.05	742.08	379.24	814.4	820.81	746.84	793.81	770.28
83.27	86.48	77.4	754.53	610.25	729.49	367.04	813.87	818.57	749.48	776.55	772.09

46.84	106.55	100.42	713.22	604.47	731.1	373.73	817.06	821.7	747.9	776.59	766.61
76.29	92.74	80.43	697.06	593.88	749.68	369.42	824.5	827.8	747.96	785.76	779.62
78.66	50.67	70.05	705.37	586.38	756.12	367.77	814.23	823.22	737.63	784.87	776.67
61.04	60.9	89.17	700.74	608.33	761.77	370.37	811.03	815.14	745.29	779.34	776.64
76.68	64.21	97.69	751.16	635.01	769.49	371.41	813.8	824.2	757.46	795.38	774.79
79.34	74.96	86.4	752.16	587.35	774.61	385.13	814.1	815.04	771.24	783.12	781.18
58.63	69.93	115.86	695.91	586.98	766.82	370.22	813.85	819.48	760.28	804.56	805.74
60.92	67.14	73.51	755.93	709.82	775.44	460.03	848.3	875.84	821.85	823.93	804.94
44.47	47.22	99.56	754.01	686.27	778.5	478.02	846.16	872.1	795.66	828.33	817.81
31.99	65.5	62.65	756.94	714.08	781.01	467.8	850.92	871.5	799.64	822.47	833.16
39.31	66.13	76.83	772.41	684.92	779.29	469.86	845.89	865.2	814.87	806.34	822.22
63.86	73.26	78.8	753.7	680.92	778.46	453.23	867.83	876.04	801.19	804.87	851.31
49.94	67.86	82.36	751.91	677.78	780.3	436.98	851.37	869.3	808.04	806.29	854.01
55.51	70.72	90.4	745.52	685.39	776.05	441.37	858.9	879.24	803.08	812.99	819.89
29.97	77.79	109.85	757.89	722.31	779.33	434.18	863.72	867.29	828.53	826.17	837.08
60.15	58.4	90.84	760.06	713.55	778.28	437.67	868.32	877.94	806.94	829.82	826.63
40.91	61.68	76.27	751.85	722.36	772.71	438.18	850.87	858.52	818.5	808.57	827.05
22.71	68.81	91.36	756.05	701.29	780.18	443.92	861.05	866.07	818.21	826.92	794.26
50.18	105.33	91.87	743.03	706.55	775.8	442.07	847.05	853.09	812.91	828.38	813.91
33.38	90.93	77.16	746.35	705.28	779.16	447.44	851.74	855.1	803.96	826.89	811.65
66.58	92.23		749.47	687.77	779.67	432.27	858.46	857.69	811.14	827.69	816.49
64.14	97.48		741.84	700.12	768.04	449.45	858.28	869.21	822.06	830.73	824.91
51.75	95.86		748.25	693.2	793.94	441.63	824.31	857.54	826.95	831.49	830.58
75.84	86.03		753.9	714.76	776.28	422.09	813.77	863.43	809.02	813.8	834.9
85.77	91.11		750.59	694.21	774.05	435.29	837.13	906.66	800.39	804.61	824.56
78.77	96.54		722.55	642.54	751.67	547.06	855.58	813.36	766.87	782.76	776.76
89.38	102.21		708.43	634.33	775.18	548.95	834.36	810.95	778.73	787.51	794.77
90.93	65.85		719.43	625.2	760.83	558.03	844.28	817.78	781.94	783.24	792.73
70.62	91.47		723.76	625.85	758.8	560.75	854.44	824.05	779.1	790.76	803.01
79.82	88.7		778.37	626.32	764.71	569.47	851.12	819.56	788.16	792.69	793.13
86.59	103.85		711.31	621.32	765.29	564.7	838.45	822.95	779.18	788.52	794.05
77.48	91.18		697.94	628.54	773.78	545.66	850.75	819.19	783.75	788.56	794.31
81.11	82.73		705.67	605.86	766.86	571.02	846.67	816.41	782.75	793.67	789.96
67	83.95		705.28	665.4	780.86	569.78	856.09	826.35	782.85	790.25	793.74
83.21	84.03		711.02	639.02	763.62	556.04	842.67	826.47	785.83	783.97	801.19
81.37	87.43		714.92	614.12	763.51	573.84	855.36	819.82	781.02	786.08	797.99
81.88			715.38	608.92	774.66	564.59	855.32	811.42	785.62	788.74	801.75
77.23			703.44	634.86	771.83	529.5	861.5	817.67	781.27	788.08	793.77
74.14			699.31	630.91	769.97	578.2	847.36	825.07	790.09	797.65	797.79
79.04			696.71	605.92	764.49	594.64	852.68	811.85	785.67	789.32	792.87
			710.04	616.69	763.15	600.42	842	819.09	787.91	792.28	794.28
			709.63	637.09	774.82	609.94	851.99	820.19	786.83	791.63	797.39
			714.6	604.77	773.05	588.87	853.1	818.49	783.3	788.96	790.69