

DC-DC Converter Concepts for Multi-Megawatt EV Charging Parks

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Kurzfassung

Die Elektrifizierung des Straßenverkehrs als wesentlicher und grundlegender Schritt in Richtung Klimaneutralität bringt nicht nur fahrzeugseitig, sondern vor allem auch infrastrukturseitig neue Herausforderungen mit sich. Die Elektrifizierung betrifft nicht nur, wie es auf den ersten Blick erscheinen mag, den Pkw-Verkehr, sondern auch die für den Güterverkehr notwendigen Klein-, Mittel- und Schwerlastkraftwagen sowie die Fern- und Nahverkehrsbusse. Insbesondere der hohe Leistungsbedarf für die Schnellladung dieser schweren Fahrzeuge stellt neue Herausforderungen u.a. an die leistungselektronischen Wandler, die im Fokus dieser Arbeit stehen. Hohe Wirkungsgrade bei gleichzeitig niedrigen Kosten sind dabei die zentralen Kriterien.

In dieser Arbeit werden DC-DC Wandler anhand eines beispielhaften zukünftigen Ladeparks hinsichtlich dieser Kriterien untersucht und optimiert. Dazu werden, nach einer kurzen Einführung in die aktuelle und einem Ausblick auf die zukünftige Ladetechnik, verschiedene Szenarien von Ladeparks an Autobahnraststätten insbesondere hinsichtlich des Verteilnetzes und der leistungselektronischen Wandler beleuchtet. Die daraus resultierenden Rahmenbedingungen wie Spannungs- und Leistungsniveaus bilden dann die Grundlage für die folgende Auslegung und Optimierung der DC-DC Wandler für die Ladegeräte. Vier verschiedene Topologien von isolierten DC-DC Wandlern, die für diese Hochleistungsanwendung geeignet sind, werden in dieser Arbeit analysiert: Phase Shift Full Bridge (PSFB) Wandler, LLC Wandler, Dual Active Bridge (DAB) und der hier als Two Stage Converter (TSC) bezeichnete zweistufige Wandler (Isolation und Leistungsflussregelung sind voneinander getrennt ausgeführt). Diese werden vorgestellt und im Detail betrachtet, so dass eine skriptbasiertes Auslegung für die einzelnen Komponenten und schließlich auch für das Gesamtsystem durchgeführt werden kann. Diese Art der Auslegung bietet die Möglichkeit, für ein breites Spektrum von Eingangsparametern alle gültigen Lösungen zu identifizieren. In einem zweiten Schritt erfolgt dann eine Bewertung hinsichtlich der genannten Kriterien Effizienz und Kosten. Durch diese multi-objektive Optimierung kann schließlich eine Lösung gefunden werden, die ein globales Optimum darstellt. Die Arbeit schließt mit der Untersuchung, Auslegung und Implementierung einer abgewandelten PSFB Wandler Topologie ab, bei der eine Umschaltung zwischen Parallel- und Serienschaltung zweier Sekundärseiten mittels Halbleiterschaltern realisiert wird. Dies ermöglicht eine flexiblere Abdeckung verschiedener Batterietypen und durch geeignete Ansteuerung einen höheren Wirkungsgrad als bei mechanischen Schaltern.

Abstract

The electrification of road transport, as an essential and fundamental step towards climate neutrality, poses new challenges not only on the vehicle side, but also on the infrastructure side. Electrification affects not only passenger cars, as might be expected at first glance, but also the small, medium and heavy-duty vehicles needed for freight transport, as well as long-distance and local buses. In particular, the high power requirements for rapid charging of these heavy vehicles pose new challenges, including for the power electronic converters that are the focus of this work. High efficiency at low cost are the key criteria.

In this thesis, DC-DC converters are investigated and optimized with respect to these criteria using an exemplary future charging park. After a brief introduction to current charging technology and an outlook on future charging technology, different scenarios for charging parks at highway service areas are examined, in particular with regard to the distribution grid and the power electronic converters. The resulting constraints, such as voltage and power levels, then form the basis for following design and optimization of the DC-DC converters for the chargers. Four different isolated DC-DC converter topologies suitable for this high power application are investigated in this work: Phase Shift Full Bridge (PSFB) converter, LLC converter, Dual Active Bridge (DAB) converter and the converter referred to here as the Two-Stage Converter (TSC, isolation and power flow control are implemented separately). These are presented and examined in detail so that a script-based design can be carried out for the individual components and ultimately for the overall system. This type of design makes it possible to identify all valid solutions for a wide range of input parameters. In a second step, these solutions are evaluated against the efficiency and cost criteria mentioned above. Through this multi-objective optimization, a solution can be found that represents a global optimum. The thesis concludes with the investigation, design and implementation of a modified PSFB converter topology in which the switching between parallel and series connection of two secondary sides is realized by means of semiconductor switches. This allows a more flexible coverage of different battery types and a higher efficiency than with mechanical switches through suitable control.

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1 Introduction

As early as 1847, Werner von Siemens dreamed of an all-electric, reliable vehicle that would not depend on rails: "When I have time and money, I will build myself an electro-magnetic cab, which will certainly not leave me sitting in the mud" (original: "Wenn ich mal Muße und Geld habe, will ich mir eine elektro-magnetische Droschke bauen, die mich gewiss nicht im Dreck sitzen lässt"). This dream came true on April 29th 1882, with the operation of the world's first trolleybus. Siemens built a modified Landau carriage, powered by 550 V DC overhead lines and driven by two electromotors, and operated it on a 540 m test track in Berlin [1]. The first battery was presented in 1800 by Alessandro Volta [2] and was further developed in the following years, setting a milestone in electrification. The combination of these two inventions led in 1888 to the first electric car, the *Flocken Elektrowagen* [3, p. 174]. Electric vehicles (EVs) became very popular in the following years and captured a significant share of the transportation market until the 1910s, when internal combustion engine (ICE) vehicles increasingly displaced EVs. However, the desire to reduce CO₂ emissions to slow global warming has led to a comeback of EVs.

This comeback is contributing to the development of a wide range of new applications for power electronics. In the vehicle itself, these applications include drive inverters, on-board chargers (OBC) and HV-LV DC-DC converters, while on the infrastructure side, power electronic converters are needed in fast chargers. The goal for power electronics in the EV sector is to become more efficient and cost effective. This thesis focuses on future high power DC-DC converters in EV charging applications. The EVs to be charged include not only cars, but also trucks up to long-haul semitrailers requiring high charging power and therefore efficient power distribution.

This chapter first introduces the challenge of electrifying the transportation sector. Following this introduction, the chapter explores the critical role of power electronics in this process, especially with respect to the charging of such battery-electric vehicles. Finally, the chapter concludes with an outline of the thesis, detailing the content of the following chapters.

1.1 The big challenge

Electrification of the road transportation system is essential for the global decarbonization needed to mitigate the impacts of the climate change. In 2015, the Paris Agreement was signed to slow the effects of climate change by reducing greenhouse gas (GHG) emissions [4]. The global average temperature increase should be kept well below 2 °C, with the aim of keeping it below 1.5 °C, compared to pre-industrial levels. The goal is to achieve net-zero CO₂ emissions by 2050. To achieve this, the EU is aiming for a 55 % reduction in emissions in 2030 compared to 1990 [5]. Road transport accounts for about one-fifth of the EU's total

GHG emissions, thus the EU has announced that from 2035 only zero-emission new passenger cars and light commercial vehicles will be allowed for sale [6].

For now, EVs appear to be the way forward for zero-emission vehicles. The big challenge, therefore, is not only to electrify road transport, but also to generate the necessary electrical energy without emissions.

1.1.1 Electricity generation in Germany

The first step is to examine the development of the process of electricity generation in Germany. Figure 1.1 shows the total net electricity generation from 1990 to 2023. While there were no significant renewable energy sources other than hydropower installed in 1990, the installed capacity of renewables has significantly increased since the turn of the millennium. Due to the decommissioning of nuclear power plants, Germany has not produced any nuclear power since April 2023. 2022 marks the year from which more than 50 % of the electricity comes from renewable sources, and the trend is rising. However, a large portion of Germany's electricity is still generated from fossil fuels such as lignite and coal.

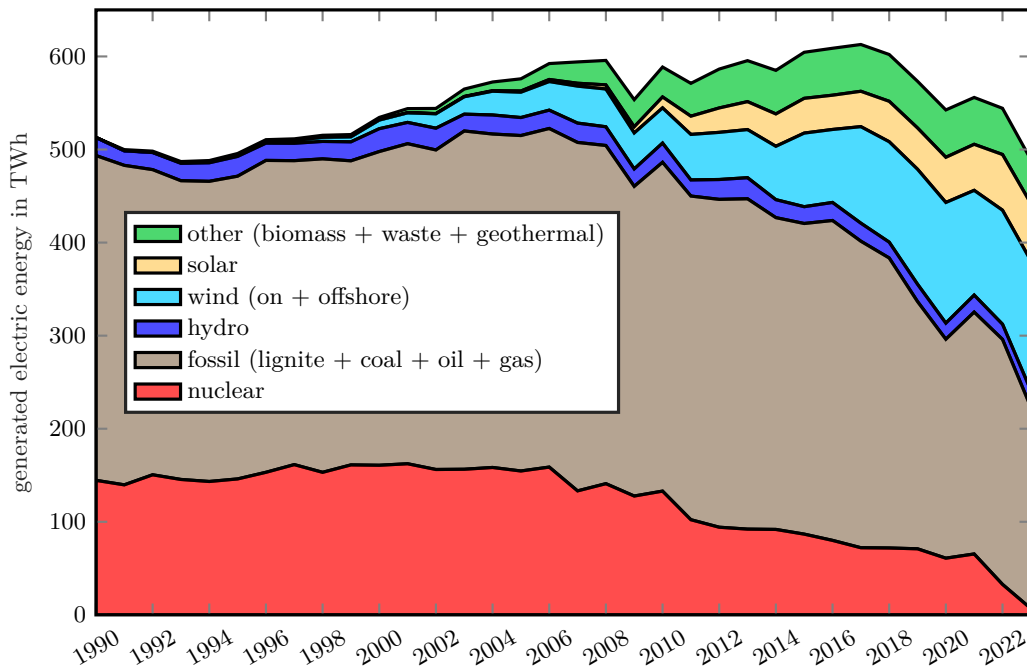


Figure 1.1 – Total net electricity generation in Germany from 1990 to 2023. Data source: [7]

As wind and solar power generation depend on wind and sunshine, respectively, generation is highly fluctuating, especially when these sources account for a large share of total installed capacity. This can be seen by looking at the actual power generated. Fig. 1.2 shows the distribution of the generated power in Germany during the week for the weeks 29 and 41 in 2024, as well as the demand. In week 29, a high share of solar power is generated during the day. Week 41 shows a higher share of wind power. However, the difference between demand and production must be imported from or exported to other countries (storage is already

taken into account). Only one day (13.10) in these two weeks shows a production surplus, mainly due to the high amount of wind power and the lower demand on Sundays.

The problem of this fluctuation is part of the challenge to achieve CO₂ neutral power generation, since during periods of low production, high-emitting fossil sources are currently used to compensate for the production deficit. One way to solve this is to try to match the demand as closely as possible to production, another is to store energy during times of excess production and release it during times when demand exceeds production. The best way is probably a combination of the two.

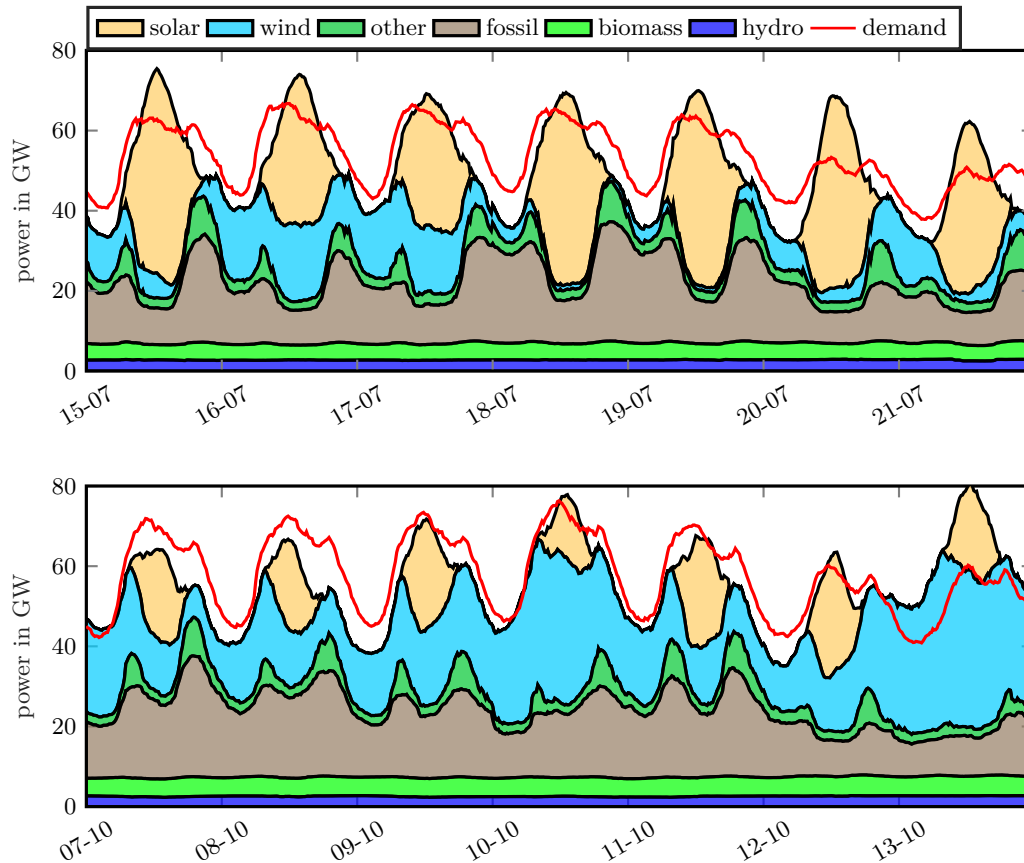


Figure 1.2 – Total net generated power in Germany in the weeks 29 and 41 of 2024 (data source: [8]). It can be seen that the renewable energy sources wind and solar have a high fluctuation. On sunny days solar power reaches up to 70 % of the total generated power. On days (and nights) with sufficient wind power, the whole day can be covered with renewable energy.

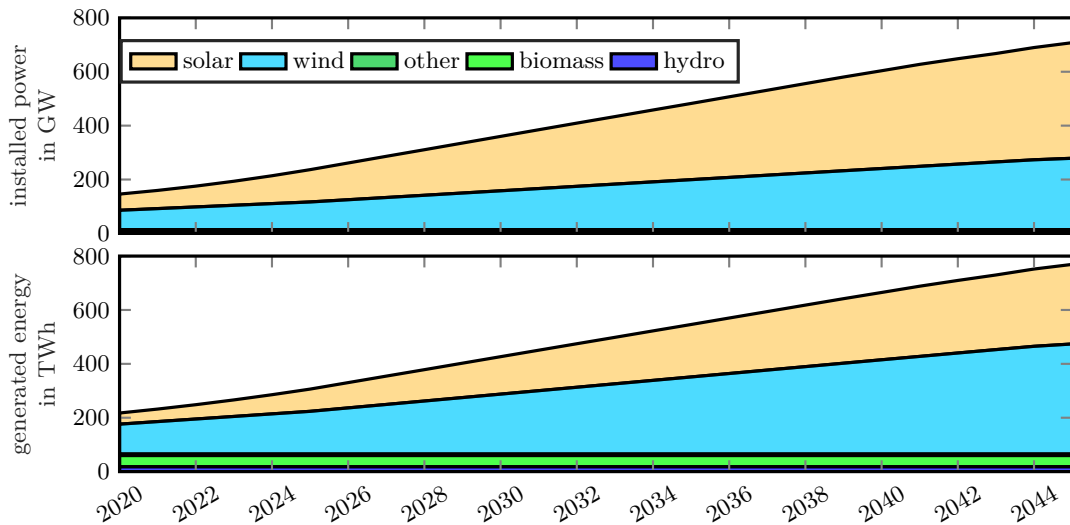
1.1.2 Only electric vehicles - what happens?

Another part of the challenge is the complete conversion of the transportation system to battery-electric drive. For this purpose, a scenario is assumed in which all vehicles are electric. The publicly available data on total kilometers traveled in 2023, broken down by vehicle type, can be found at [9]. Table 1.1 shows these kilometers traveled, from which the total energy consumption is calculated using an assumed average consumption for the different vehicle types.

Table 1.1 – Energy consumed by different types of vehicles in Germany in 2023, assuming all vehicles were battery electric.

vehicle	mileage in mln. km [9]	consumption [10–12]	total energy
cars	591 132	0.15 kWh/km	88.67 TWh
trucks ≤ 3.5 t	57 520	0.42 kWh/km	24.16 TWh
trucks ≤ 7.5 t	4181	0.71 kWh/km	2.97 TWh
trucks > 7.5 t	14 519	0.85 kWh/km	12.34 TWh
long-haul trucks	19 799	1.23 kWh/km	24.35 TWh
busses	4292	1.21 kWh/km	5.19 TWh
total:			157.68 TWh

These approximately 160 TWh of additional electric energy required by road transportation would mean an increased energy demand of about 30 % (total demand 2023: 495 TWh [7]). As of today, this would only be possible using even more fossil energy sources and would therefore not contribute to CO₂ reduction (compared to continued use of conventional vehicles). Therefore, the renewable sources must be expanded. Fig. 1.3 shows a scenario reference of the installed capacity of wind and solar power [13] and today's (2023) capacity in hydro, biomass and other (e.g. geothermal and waste) renewable sources. With the assumptions of this scenario and a comparable energy demand as in 2023 (total, including transportation ≈ 660 TWh), an exclusive supply with renewable sources could be possible from 2040 on.

**Figure 1.3** – Top: installed capacity of renewable energy sources, scenario reference. Data for wind and solar: [13]. Power and energy for hydro, biomass and others is from 2023 and assumed to remain constant. Bottom: generated solar and wind energy, scaled from the installed power with the ratio from the generated energy to the installed power of 2023 ($E(x) = E(2023)/P(2023) \cdot P(x)$).

However, this would require an ideal transmission grid and sufficient storage capacity to smooth out fluctuations. Moreover, this does not take into account limited resources, e.g. for the production of the batteries needed for the electrification of the transport system.

The further development of more efficient processes and devices in industry, commerce, trade, the service sector and households, together with more efficient EVs, can further reduce the energy demand. Intelligent load and charging management and the simultaneous use of EV batteries can help to balance generation or load peaks. With these facts and the use of current and future technologies, this huge challenge seems solvable.

1.2 Power electronics

When it comes to bringing the (ideally renewable) energy from the source to the EV, power electronics is an important player. High efficiency is the key to keeping the energy losses to a minimum. A quick example calculation using the EV energy demand calculated in the previous section results in annual cost savings

$$\begin{aligned} C_{\text{saving}} &= (\eta_{\text{high}} - \eta_{\text{low}}) \cdot E_{\text{charging}} \cdot c_{\text{energy}} \\ &= (98\% - 95\%) \cdot 160 \text{ TWh} \cdot 21 \frac{\text{ct}}{\text{kWh}} > 1 \text{ bn } \text{€}, \end{aligned}$$

showing that over one billion €/year can be saved on losses with an efficiency of 98 % compared to 95 % (assuming an average energy cost of $21 \frac{\text{ct}}{\text{kWh}}$).

1.2.1 Electric vehicle charging

The basic function of charging an EV battery is as follows: The energy is drawn from the grid, which in Europe is a single-phase (for low power) and a three-phase (for high power), 50 Hz AC grid. A power electronic converter, converts this AC voltage into a DC voltage. In a second stage this DC voltage is galvanically isolated to provide an isolation between the EV battery and the grid to ensure electrical safety. Other configurations, such as isolation on the AC side or integrated isolation in the AC-DC converter, are also possible [14]. Fig. 1.4 shows the structure of such a charging system with the power grid, AC-DC converter, isolated DC-DC converter, and the EV with the battery. This structure shows a stationary (DC) charger, the different types of charging are presented in the next chapter.

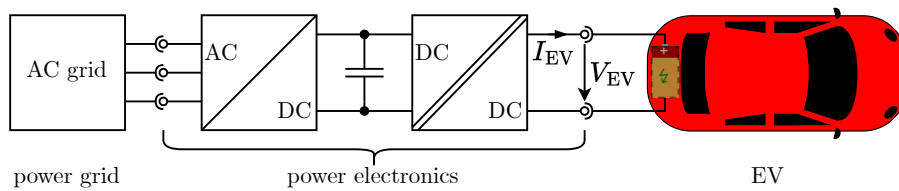


Figure 1.4 – Structure of a charging system: energy drawn from the grid is converted from AC to DC and isolated with the power electronics and charges the EV’s battery

This thesis is mainly concerned with the analysis and design of high power DC-DC converters. The application under consideration is the charging of EVs, in particular the fast charging of these vehicles (cars and trucks).

1.2.2 Technology

The power electronics industry is evolving rapidly. This is mainly due to the increasing demand for AC-DC, DC-DC and DC-AC converters in the applications EV, EV charging and integration of renewable energy sources such as solar and wind. The quest for higher switching frequencies and power densities is inspiring new technologies, especially for semiconductors. Wide bandgap materials such as silicon carbide (SiC) and gallium nitride (GaN) enable higher switching frequencies and higher efficiencies compared to the conventional silicon (Si) devices. SiC MOSFETs are increasingly replacing Si IGBTs in EVs and in EV chargers; in fact, most of the new DC chargers and fast chargers use SiC MOSFETs due to their high efficiency.

1.2.3 Sustainability

Even though it is not the direct focus of this thesis, sustainability in power electronics is more relevant than ever [15]. With the rapid increase in the number of power electronic converters, the question arises as to what to do with those that have reached the end of their service life. Some components, such as heatsinks and cases are relatively easy to recycle, while others, such as PCBs or ferrites are not. The production of the power electronic converters is energy intensive, resulting in CO₂ emissions, especially in the production of the components. Two essential key parameters to increase the sustainability of these converters from development are to increase the efficiency (lower losses and therefore less energy wasted during lifetime) and to increase the lifetime (production emissions are less significant compared to the saved emissions during operation), the former also being part of the optimization later in this thesis.

1.3 Thesis outline

The thesis starts with an overview of the state of the art of EV charging in chapter 2. This includes the current standards, including voltage, current and power range of today's EVs and EV chargers as well as an overview of the installed charging infrastructure in Germany in 2024. Finally, an introduction to current EV batteries is given, highlighting the importance of a high voltage range for the charger and high efficiency over this range.

In chapter 3, a case study of a charging park in a highway service area is considered for the year 2035. An analysis for the power distribution is carried out to determine the optimal distribution grid type and the system voltage for the subsequent calculations of this thesis.

Chapter 4 provides an overview of DC-DC converters in general and introduces four specific DC-DC converter topologies. These are presented and analyzed in detail by calculating all the currents and voltages and dimensioning the passive components required for the automated design process.

In chapter 5 a multi-objective optimization is performed for the different topologies in different system configurations. In a first step, Matlab-based design routines are created and presented in detail. In a second step these routines are employed to generate a set of valid solutions for each topology. The best solutions in terms of cost and efficiency are found by selecting the

Pareto optimal designs. Finally, the results of the optimization and further potential of these converters are discussed.

The last chapter, chapter 6 deals with the design and implementation of a DC-DC converter with a solid state switch. This topology is able to instantly change its output configuration from parallel to series and vice versa, thus achieving high efficiency over the entire output voltage range. In the first step, this topology is presented and analyzed. In a second step the components are dimensioned analytically. A simulation is performed to demonstrate the operation of the topology. The chapter concludes with the realization and the testing of a hardware prototype.

2 EV charging - state of the art

The goal of this chapter is to provide a comprehensive introduction to the various types of electric vehicle (EV) charging systems. It begins with an exploration of the different charging methods currently available, highlighting the state-of-the-art technologies that define today's EV charging landscape. The chapter also looks ahead, providing insights into emerging and future technologies that will shape the evolution of EV charging infrastructure. Given the central focus of this work on high-power DC charging, special attention is given to this particular topic.

2.1 Charging Types

Three different types of charging are considered in this context: wired charging with alternating current (AC), direct current (DC), and wireless charging [16]. The different types and their underlying standards are presented in the following. According to the conductive charging standard IEC 61851 [17], the stationary charging point is referred to as Electric Vehicle Supply Equipment (EVSE), while the battery electric vehicle is called EV. For the different types of charging, there are different functional blocks of electronics located in the EVSE and in the EV.

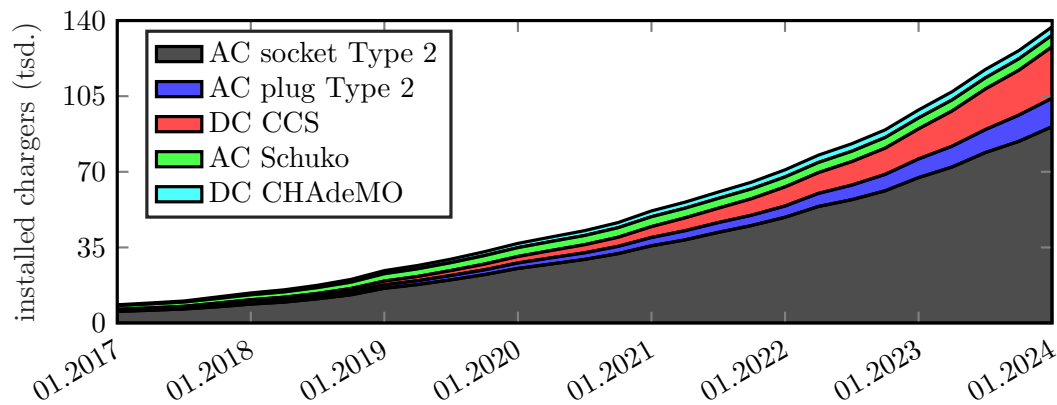


Figure 2.1 – Evolution of the different types of chargers installed in public spaces in Germany over the years from 2017 to 2024. Data source: Bundesnetzagentur [18]

Fig. 2.1 shows the evolution of public chargers in Germany over the last seven years, broken down by charging type. The data for AC chargers is divided into Schuko (single phase), socket and plug, with the three-phase Type 2 AC socket charger accounting for the largest share of public chargers. For DC charging, the two types installed in Germany are CCS and CHAdeMO. The different types of charging are explained more in detail below.

2.1.1 AC charging

The concept of AC charging is that the power is drawn directly from the either single-phase or three-phase AC grid (230 V/400 V in Europe) to charge the EV. The power electronic AC-DC converter and the charge management system are located inside the EV (on-board charger). It is the most used type of charging in terms of charging events and charging points installed in Germany [19] (as it can be seen in fig. 2.1 about 75 % of the public chargers are AC chargers). AC charging points are installed not only in public places, but also in semi-public areas such as workplaces or in private places (at home), which further increases their overall share. Usually AC chargers come in the form of a charging station or a wallbox.

Connectors for AC chargers vary from country to country. In the European Union, the Type 2 connector is established and described in the IEC 62196-2 standard [20]. The connector consists of five power and two communication contacts. The power contacts are L1-3, N and PE and allow both single-phase and three-phase charging. With the communication contacts control pilot (CP) and proximity pilot (PP) status and maximum charging power for EVSE and EV is communicated.

The maximum power levels for AC charging come from the different current capacity standards (10 A, 16 A and 32 A) and are 2300 W (single phase), 3.7 kW/11 kW and 7.4 kW/22 kW (for single/three phase). For the current standard the highest maximum charging current for AC EVSE is 63 A and allows a maximum three-phase charging power of 44 kW. While only very few EVs support 44 kW AC charging, most manufacturers opt for lower charging power due to the weight and cost of the on-board charger. Therefore, the most common power levels for AC charging are 11 kW to 22 kW.

2.1.2 DC charging

DC charging is used to achieve faster charging with typically higher power levels compared to AC charging, resulting in shorter charging times. The power electronics is located in the EVSE and is connected to the vehicle battery via the charging cable. Typically, such DC fast chargers are installed at gas stations, highway service areas or in industrial sites. A distinction is made between fast chargers and ultra-fast chargers. As of 2024, fast chargers can charge with a power of 50 kW to 150 kW, while ultra fast chargers provide a charging power of 150 kW to 350 kW. The international standard IEC 61851-23 [21] describes the requirements for DC charging EVSE. High power DC charging is described in more detail in section 2.2. Since the standard requires an isolation between the grid and the EV battery for electrical safety reasons, non-isolated chargers such as in [14] are not considered in this work.

CHAdemo

CHAdemo is a DC fast charging standard originally developed in Japan, but also used in Europe, particularly for older EV models. As CHAdemo is losing relevance in Europe (only <5 % new chargers with CHAdemo installed in Germany from 2023 to 2024, while CCS chargers increased by over 70 % in the same period), this charging standard will not be discussed further in this work.

Combined Charging System CCS

In Europe, the established standard for conductive charging is the Combo 2 variant of the Combined Charging System (CCS2) by CharIn [22]. It combines AC and DC charging in one connector on the EV (described in the IEC 62196-3 standard [23]). On the EVSE side, the connector is different for AC and DC charging: a smaller connector is used for AC charging (without the DC pin extension), while the full connector is used for DC charging (the AC-specific pins are usually not populated). The voltage range for CCS2 DC charging is 200 V to 920 V and the originally intended maximum charging power is 350 kW. By using water-cooled charging cables, higher currents of 500 A and more are possible, increasing the maximum charging power to 400 kW or more.

Bidirectional DC charging

Although bidirectional AC charging is also possible (requiring a bidirectional on-board charger), the bidirectional DC charging is described here. There are many possible applications for bidirectional charging where the direction of the power flow is from the vehicle to the respective application V2X, $X \in \{G(\text{grid}), H(\text{home}), V(\text{vehicle}), L(\text{load})\}$ [24, 25]. By using the energy stored in the battery of the EV the grid can be supported (V2G) by providing the energy during periods of high demand and recharging during off-peak times. Greater energy independence can be achieved with V2H by allowing homeowners to manage their energy use more effectively by storing excess solar energy in their EV and using it during off-peak hours. Therefore, more and more DC chargers with lower power than the fast chargers (11 kW to 22 kW) are becoming available in the form of a wallbox.

The European standard [26] defines the required behavior for generating plants and the grid codes, that also apply to bidirectional chargers feeding the grid. The guidelines for Germany are VDE-AR-N 4105 and 4110, where the overall installed power on any given POC (point of connection) defines if the low voltage (<135 kW in Germany) or the medium voltage (≥ 135 kW) standard has to be considered. The standard for the EVSE to the EV communication for bidirectional charging is the ISO 15118 [27] standard. An increasing number of EV and EVSE manufacturers are implementing this standard. Although there are no technical and normative barriers to bidirectional charging, as of 2024 there is still no EV that officially supports it (same for bidirectional AC charging). The main reason for this is the lack of fiscal and financial regulations. This is expected to change in the next few years [28].

2.1.3 Wireless charging

Wireless (inductive) EV charging is an emerging technology that provides a cable-free alternative to the conductive methods. The principle of operation is based on electromagnetic induction between two coils, where the EVSE consists of a stationary ground pad with an energy transmitting coil. The receiving coil is located on the floor of the EV, where via an AC-DC converter the battery is charged. There are two types of wireless charging, static and dynamic wireless charging. For the static charging the ground pad is installed in a parking lot and the vehicle does not move during charging, while for the dynamic wireless charging the ground coil is built into the road and allows charging also while driving. The standard

that governs wireless charging is IEC 61980 [29]. However, because this standard is still in development, there are no production vehicles supporting wireless charging in 2024.

2.2 Fast charging with high-power DC

The remainder of this thesis is devoted exclusively to the study of high-power DC charging, given its central role in the future of fast EV charging infrastructure. This section provides an overview of three different high-power DC charging systems, including existing technologies and those expected to emerge in the near future. These systems will serve as key reference points for the discussion and analysis that follows in this thesis.

2.2.1 HPC - High Power Charging

High Power Charging (HPC) systems are DC chargers with a charging capacity of 150 kW or more. In Europe almost all HPC chargers use the CCS2 standard. The purpose of HPC is to reduce the charging time of EV batteries by utilizing high power. This allows the battery to be charged from 20 % to 80 % in about 15 to 30 minutes. This is crucial to making EVs more practical, especially for long-distance travel, and to overcome one of the biggest barriers to EV adoption by making the experience more like refueling a conventional vehicle. For HPC a voltage range from 200 V to 1000 V and a maximum charging power of 350 kW are considered in this work. Moreover, HPC is considered the charging standard for electric cars, while the upcoming MCS is the standard for electric trucks.

2.2.2 MCS - Megawatt Charging System

The Megawatt Charging System MCS is a fast charging system for electric trucks and heavy-duty vehicles. It is currently being developed by the CharIn committee [30] and is based on the CCS2 system. However, the voltage range and the connector are different, allowing for a higher current capability and a megawatt power level. The maximum charging current is estimated to be 3000 A, while the voltage range is enlarged on the upper limit to 500 V to 1250 V, allowing a theoretical maximum charging power of 3750 kW. Although the voltage range is still preliminary, it is the range considered in this work. The first version of the corresponding standard, the IEC 61851-23-3 [31] is to be published in 2025.

2.2.3 NCS - Night Charging System

The term Night Charging System NCS is not yet widely recognized, but it is introduced in [32] and used here to describe the charging of electric trucks during the night or extended rest periods. In terms of voltage range, plug, and communication, NCS corresponds to the MCS standard. The only difference is the lower charging power, as the charging time is long enough to fully charge the battery even at lower power. It would also be possible to charge slowly at high-power MCS chargers, but this would potentially be inefficient for the EVSE and require a very large number of charging points with high installed power and large charging cable cross-sections, which is not economical. In addition, the location for MCS and NCS is

different. NCS chargers should be located in the quieter parking lot and not at the noisy and busy "electricity gas station" MCS. The power level considered here for NCS is 100 kW.

2.3 State of the art charging infrastructure in Germany

The charging infrastructure in Germany has been widely expanded in recent years. As of March 2024, there are more than 100 000 public chargers and >25 000 public fast chargers installed in Germany (data from the German Bundesnetzagentur [18]). Figure 2.2 shows the evolution of the installed chargers over the last years and the share of the different power levels. The evolution of the total installed charging power (power that can be drawn at the same time) is also shown, where as of 01.01.2024 almost 4.4 GW of charging power is installed and still growing strongly.

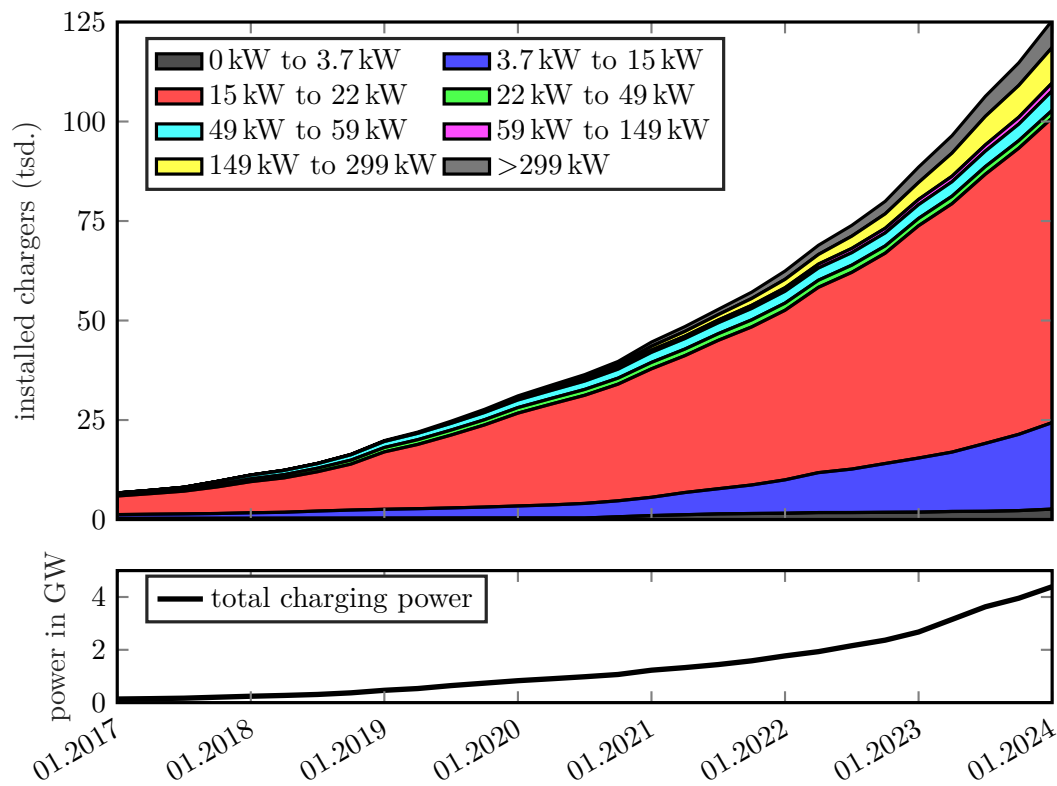


Figure 2.2 – Evolution of the different power levels of the installed chargers in Germany (top) and the installed total charging power (bottom) from 2017 to 2024. Data source: Bundesnetzagentur [18]

Fig. 2.3 shows the number of chargers and fast chargers installed in the German federal states as of 2024. The highest power for one charging point installed is 400 kW, as of July 2024 around 70 400 kW CCS chargers are installed in Germany.

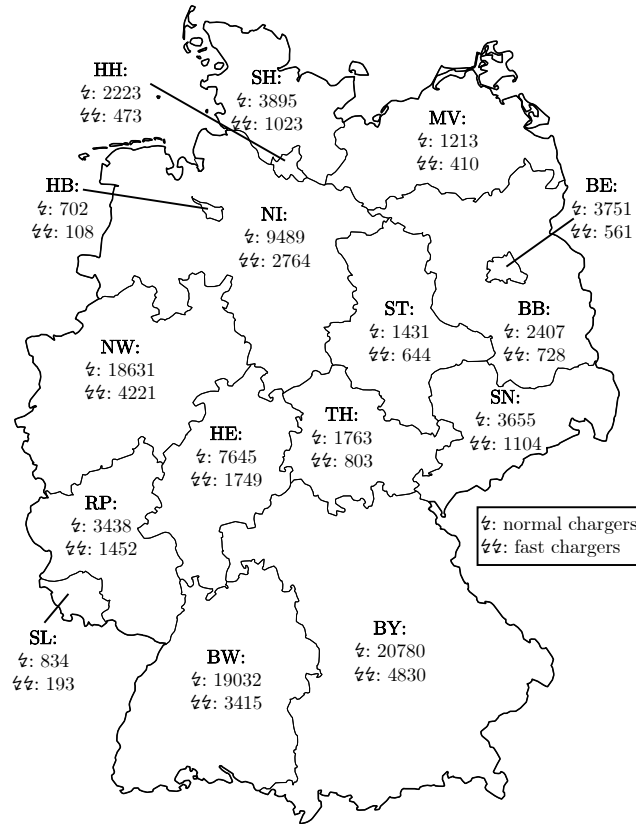


Figure 2.3 – Map of Germany with the number of chargers and fast chargers in the federal states as of 01.2024. Data source: Bundesnetzagentur [18]

2.4 EV Batteries

EV batteries are the heart of modern electric vehicles, serving as the primary source of energy to power the vehicle's motor. These batteries, typically made of lithium-ion, are designed to store large amounts of energy to provide the power and range needed for driving. Advances in battery technology have led to improvements in energy density, charging speed, and overall durability, allowing EVs to travel longer distances on a single charge and reducing the time needed to recharge. In addition, as battery costs continue to decrease, electric vehicles are becoming more affordable, as the battery is one of the most expensive components in the EV. To understand the challenges facing EV chargers, a brief introduction to modern EV batteries is provided.

2.4.1 Battery cells

The battery cells used in EVs are typically lithium-ion based and consist of a positive electrode (cathode), a negative electrode (anode), a separator, and an electrolyte. The cathode is typically made of materials such as lithium nickel manganese cobalt oxide (NMC) or lithium iron phosphate (LFP), while the anode is typically made of graphite. During charging, lithium ions move from the cathode to the anode through the electrolyte, where they are stored. When power is drawn from the battery, these ions flow back to the cathode,

generating an electric current. The efficiency, energy density, and longevity of these cells are critical factors that determine the overall performance of the EV. As the technology advances, research is focused on improving cell chemistry to increase energy density, reduce cost, and improve charging speed.

2.4.2 Battery packs

The battery in an EV consists of an interconnection of many individual battery cells. A certain number of cells are connected in series to achieve the required nominal voltage. For a higher total capacity, several of these series-connected cells are then connected in parallel (as it can be seen in fig. 2.4a). A battery management system (BMS) monitors the battery pack for temperature, voltage and state of charge (SOC) and manages the balancing of the individual cells. The correlation between the SOC and the cell voltage, and thus the total battery voltage seen by the charger, is highly complex [33, 34]. In fig. 2.4b this relationship can be seen for an example battery cell. The range of the theoretical usable SOC of the battery is reduced by the BMS in order to extend the lifetime and not to fall below a certain voltage level.

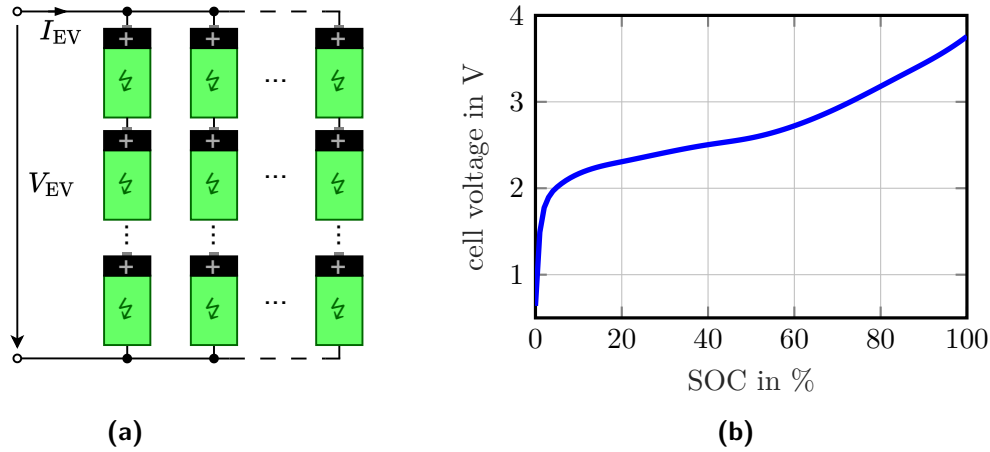


Figure 2.4 – a) EV battery pack consisting of series and parallel connected battery cells b) voltage over SOC for a Li-ion battery cell. Data source: [35]

2.4.3 Battery voltages

With the number of series connected battery cells in the pack, the voltage for the EV battery is defined. Currently, most EVs use battery packs with nominal voltages typically in the range of 300 V to 400 V, which balances energy storage and power delivery for standard passenger cars. However, high-performance and long-range EVs are increasingly using higher voltage systems, such as 800 V or higher, to enable faster charging, reduce current for a given power level, and improve overall efficiency. In addition to the charging infrastructure, the higher voltage levels also affect the design of the drivetrain and inverter, as the higher voltages require different components such as semiconductors. The trend toward higher voltage levels is likely to continue, especially for heavier electric vehicles with higher battery capacity, such as trucks. Since the battery is one of the most expensive components and its price scales

with capacity, low-cost or urban EVs will continue to be equipped with smaller battery packs in the future. To ensure that the number of cells connected in parallel in the pack does not become too small (reduced current carrying capacity, lower reliability) and cannot be lower than one, the 400 V voltage class will continue to be available for EVs, and future chargers must also be able to handle it. Due to the different voltage levels of the different EV models, the voltage range of the EVSE must be very wide. As the battery is charged, the voltage increases, and as with the single cell, the voltage range that the charger must cover during one charging session is also not negligible.

2.4.4 Charging power

The maximum charging power depends on the charger and the vehicle. Current electric cars can charge with up to 350 kW. The maximum charging power also depends on the SOC. In most cases, charging is done at full power in the lower range and the power is reduced as the SOC increases, in order to prolong the life of the battery. Figure 2.5 shows the charging power in dependency of the SOC for different EV models.

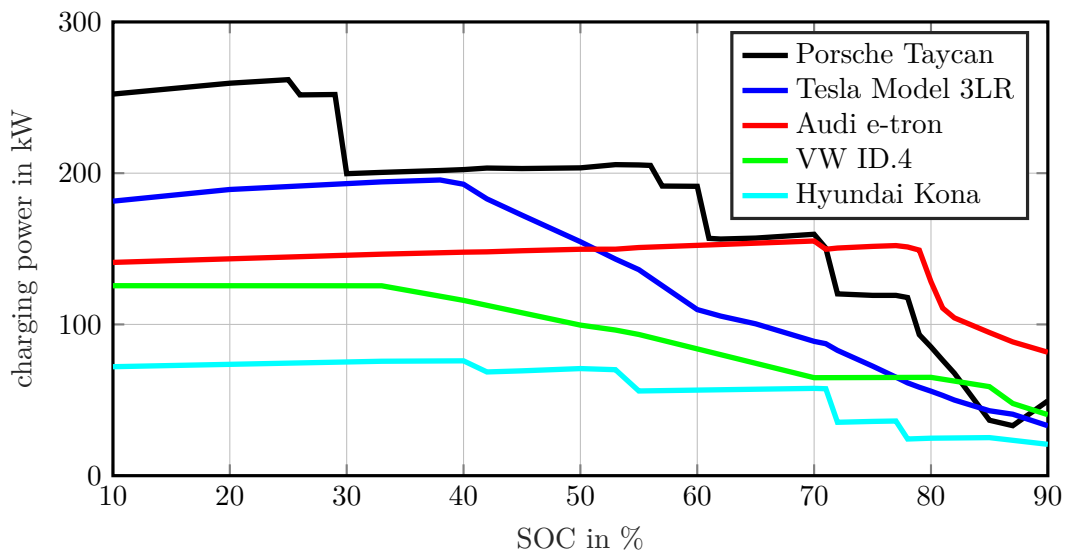


Figure 2.5 – Charging power in dependency of the SOC from 10 % to 90 % for different EV models [36]

2.5 Conclusion

In this chapter an overview of the different charging systems AC and DC charging is provided. High-power DC charging and the underlying standards are discussed in detail, as it forms the basis for the subsequent chapters. The three DC charging standards HPC, MCS and NCS are introduced. A brief insight into the development of the charging infrastructure in Germany highlights the increasing demand for EVSE. The chapter concludes with a short introduction to EV batteries and the different battery pack voltages, emphasizing the importance of a wide voltage range of the EVSE.

3 System considerations of a charging park

This chapter deals with the system considerations of a high-power charging park to determine the requirements for the power electronic converters. For this purpose, a case study is used to illustrate the possible applications of high-power chargers within the charging park in a highway service area. The year considered is 2035 - about ten years after the writing of this thesis. Studies are used to estimate the number and power requirements of charging points for that year. By creating different layouts for the charging park, three different types of power distribution within the charging park are analyzed and compared based on different scenarios.

3.1 Highway service area in 2035 - a multi-megawatt charging park

By 2035, highway service areas are expected to evolve into advanced, multi-functional hubs to serve not only internal combustion engine vehicles, but also electric cars and trucks. With electric vehicles expected to dominate the roadways (or at least equal the number of conventional vehicles), these service areas will be equipped with ultra-fast charging stations and likely integrate renewable energy sources. For the system considerations an example of such a service area is set up and investigated.

3.1.1 Battery-electric vehicles in 2035

By 2035, electric vehicles (EVs), both cars and trucks, are likely to be highly advanced, with long-range batteries and ultra-fast charging capabilities. As described in section 1.1, the CO₂ reduction requirement will lead to a high percentage of EVs in this year.

Electric trucks

In the course of the electrification of vehicles, electric trucks are increasingly replacing conventional combustion-engine trucks. Starting from small trucks (≤ 3.5 t) to medium duty (≤ 18 t) and semitrailers (≤ 40 t), battery-electric trucks are already available. Well-known manufacturers have already announced the discontinuation of the internal combustion engine as the EU mandates a 90 % reduction in CO₂ emissions by 2040 [37]. Battery-electric long-haul trucks are expected to hold a share of up to 50 % in 2035 on high traffic volume routes (<10 % on less frequented routes but increasing rapidly for 2040) [38].

A driving time interruption of 45 minutes every 4.5 hours for the driver is currently required by law in Germany. During this time the driver is not allowed to move the truck from the MCS charging area. With a speed limit of 80 km/h on the highway a maximum distance of 360 km can be covered during one 4.5 hour shift before the driving interruption is required

(only one driver assumed). The energy consumption is assumed to 1.23 kWh/km [11] for long-haul trucks, including the charging losses. This results in an maximum energy demand of about 450 kWh before the mandatory break. Therefore a MCS charging power of 720 kW to 1000 kW [39] or 1100 kW [40] is sufficient to recharge the truck within the driving interruption. Autonomous driving trucks are not considered in these two referred studies and are therefore also not included in this work. These self-driving trucks do not need to observe the driving time interruption, which could result in a higher maximum fast charge power for the MCS chargers. Whether and how widespread autonomous trucks will be in 2035 is an uncertainty in the assumptions of this work, but the methodologies shown in the further course of this thesis are well scalable to higher power.

Electric cars

According to EU law, newly registered cars must no longer emit CO₂ from 2035. Studies show that the share of battery-electric cars will then be about 50 % to 80 %. The different battery pack types (e.g 400 V or 800 V) will continue to exist because of the different ranges for urban and long-range vehicles. It is therefore expected that the current CCS standard for charging will be retained. A comprehensive study on the expansion of charging infrastructure required for electric cars by 2030 with an outlook to 2035 has already been carried out in [41].

3.1.2 Different scenarios of service areas

In 2022, a study on the grid integration of charging stations for battery electric trucks was conducted by NOW GmbH on behalf of the German "Nationale Leitstelle Ladeinfrastruktur" [32]. The study examines three different scenarios in the form of prototypes: small, medium and large charging parks. The increasing number of charging points over the years due to the increasing share of battery electric vehicles is taken into account. Specifically, the years 2027, 2030 and 2035 are considered. The main aspect of the study is the power requirement (also taking into account simultaneity factors) of such a charging station and what it means in terms of cost and time to integrate it into an existing medium or high voltage grid. The scenarios are described below and consider the charging infrastructure of one highway service area, while assuming that a similar service area is located on the other side of the highway, for the opposite direction of travel. Some numbers of chargers in this work are rounded to an even integer compared to the study, in order to make them easier to divide into lanes with the same number of chargers. The three charging systems MCS, HPC and NCS are considered, covering the whole range of battery-electric vehicles. Congruent to the previously shown numbers of the estimated charging power required, a power of 900 kW is assumed for MCS.

Scenario 1

Scenario 1 represents a heavily used service station with a charging hub on a busy highway, and thus the upper end of the power requirement. This scenario assumes a power demand (power of the grid connected transformer) of approximately 30 MW in 2035. The estimate is for more than 280 900 kW MCS charging sessions per day. Therefore, the number of installed

MCS chargers required is 24. The number of 200 kW and 350 kW HPC chargers needed is eight and 24 respectively, while there are 80 100 kW NCS chargers required for the overnight charging lots.

Scenario 2

Scenario 2 represents a medium-sized highway charging park, which is assumed to be the average size of a highway charging station in Germany. A total power requirement for the chargers of about 20 MW per direction in 2035 is estimated. Scenario 2 assumes the same power levels for the MCS, HPC and NCS chargers. The number of chargers is 14 for MCS, 36 for NCS and 24 for HPC (four 200 kW and 20 350 kW chargers).

Scenario 3

Scenario 3 considers a small charging hub on a secondary highway route with a grid connection capacity of 10 MW. It is not a service area, just a rest area for trucks and a small number of cars. Therefore, the number of 100 kW NCS chargers is higher compared to MCS and HPC chargers and it is estimated to be the same as in Scenario 2. Five MCS and twelve (four 200 kW plus 350 kW) HPC chargers are assumed for this scenario.

Overview

A relatively high amount of required charging power is already predicted for 2035 and it is expected to increase even further for the years after until the share of 100 % for electric vehicles is covered by the charging infrastructure. The number of the chargers required in the

Table 3.1 – Number of charging points per direction of travel considered in the different scenarios for the year 2035 (some figures have been rounded compared to the study in [32] in order to divide them by the respective number of lanes).

Charger type	Scenario 1	Scenario 2	Scenario 3
MCS 900kW	24	14	5
NCS 100kW	80	36	36
HPC 200kW	8	4	4
HPC 350kW	24	20	8

different scenarios for the each power level is summarized in table 3.1. These figures are used in the following assumptions and calculations.

3.1.3 Example layouts for charging hubs

Based on the previously presented numbers from the study, the chargers are divided into a layout to ensure that the charging points are appropriately distributed within the charging park. Two different layouts will be set up in the following and be compared in terms of required conductor material for the distribution grid, feasibility and functionality.

Charging point arrangement - Layout 1

In Layout 1 one technical building (substation) is considered. This medium-voltage substation contains the medium-voltage transformer and, depending on the type of distribution grid chosen, the power electronic converters. The different types of distribution grids are discussed in section 3.2. Conductors (cables or busbars) lead from the substation to the charging points, where a double charging unit is located between two double lanes. The arrangement of the chargers is such that the distance to the substation increases as the power decreases, in order to keep line losses as low as possible. Fig. 3.1 shows the arrangement of the charging units and the cable lengths from the substation assumed in Layout 1 with the maximum number of chargers, divided into four lanes (as in Scenario 1). Scenarios 2 and 3 assume two lanes and one lane, respectively.

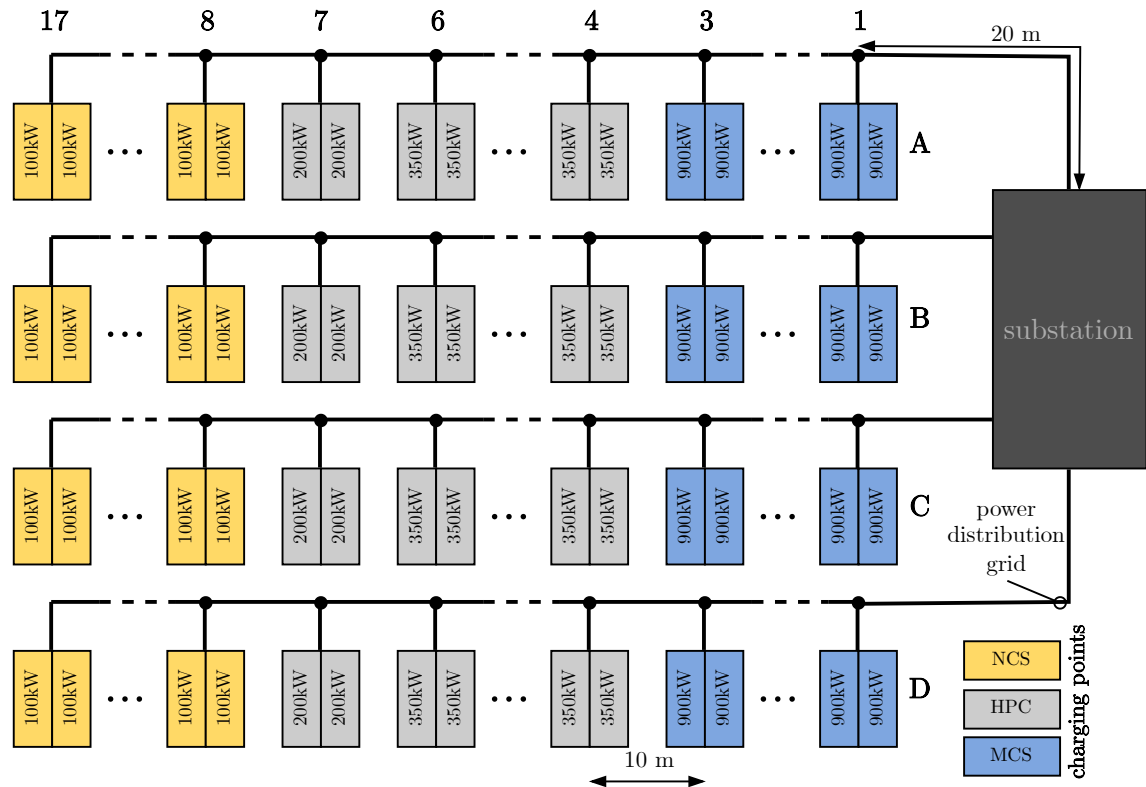


Figure 3.1 – Example layout (Layout 1) for the charging points of Scenario 1 in 2035 with a single substation. The charging power is decreasing with increasing distance to the substation.

Charging point arrangement - Layout 2

In Layout 2, the charging infrastructure is integrated into an existing example service station. Since there will still be vehicles with internal combustion engines in 2035, the service station will still have a gas station. Therefore, there will also be parking spaces without a charging unit for both trucks and cars. In this layout, the different types of charging - MCS, NCS and HPC - are physically separated. In the MCS area, each lane has its own charger, while in the HPC and NCS areas, one double charging unit serves two parking spaces. For reasons of

clarity and noise pollution caused by constantly changing vehicles, the NCS area is separated from the MCS chargers. For this reason, the MCS + HPC and NCS are supplied from a separate substation. In fig. 3.2 the arrangement of the chargers in Layout 2 can be seen. The number of chargers and lanes depends on the scenario: for Scenario 1 the chargers are distributed over four lanes, in Scenario 2 over two lanes, and in Scenario 3 a single lane is assumed.

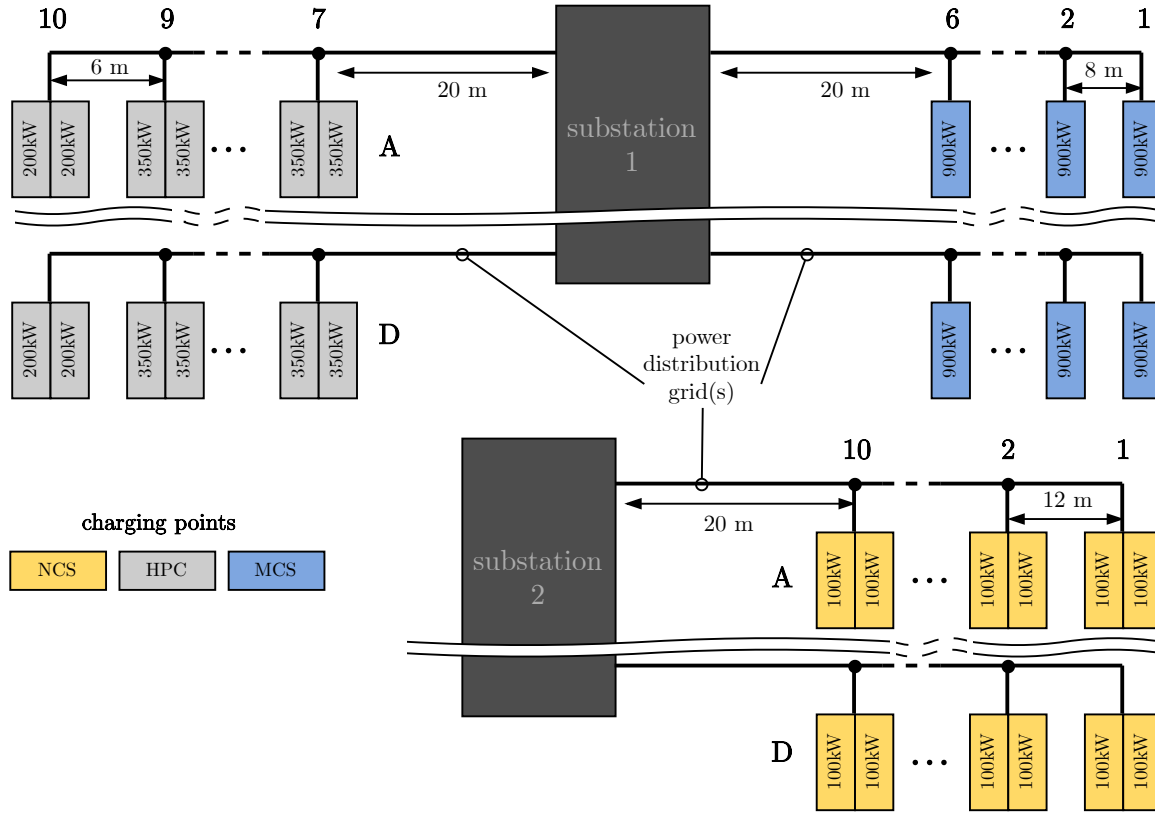


Figure 3.2 – Layout 2 of the charging points of Scenario 1 in 2035 with a divided substations. Here: double MCS and HPC and single MCS charging points.

Fig. 3.3 shows a true to scale example model of the service area with HPC, MCS and NCS charging areas, as well as parking facilities for conventional vehicles for Scenario 1 and Layout 2.

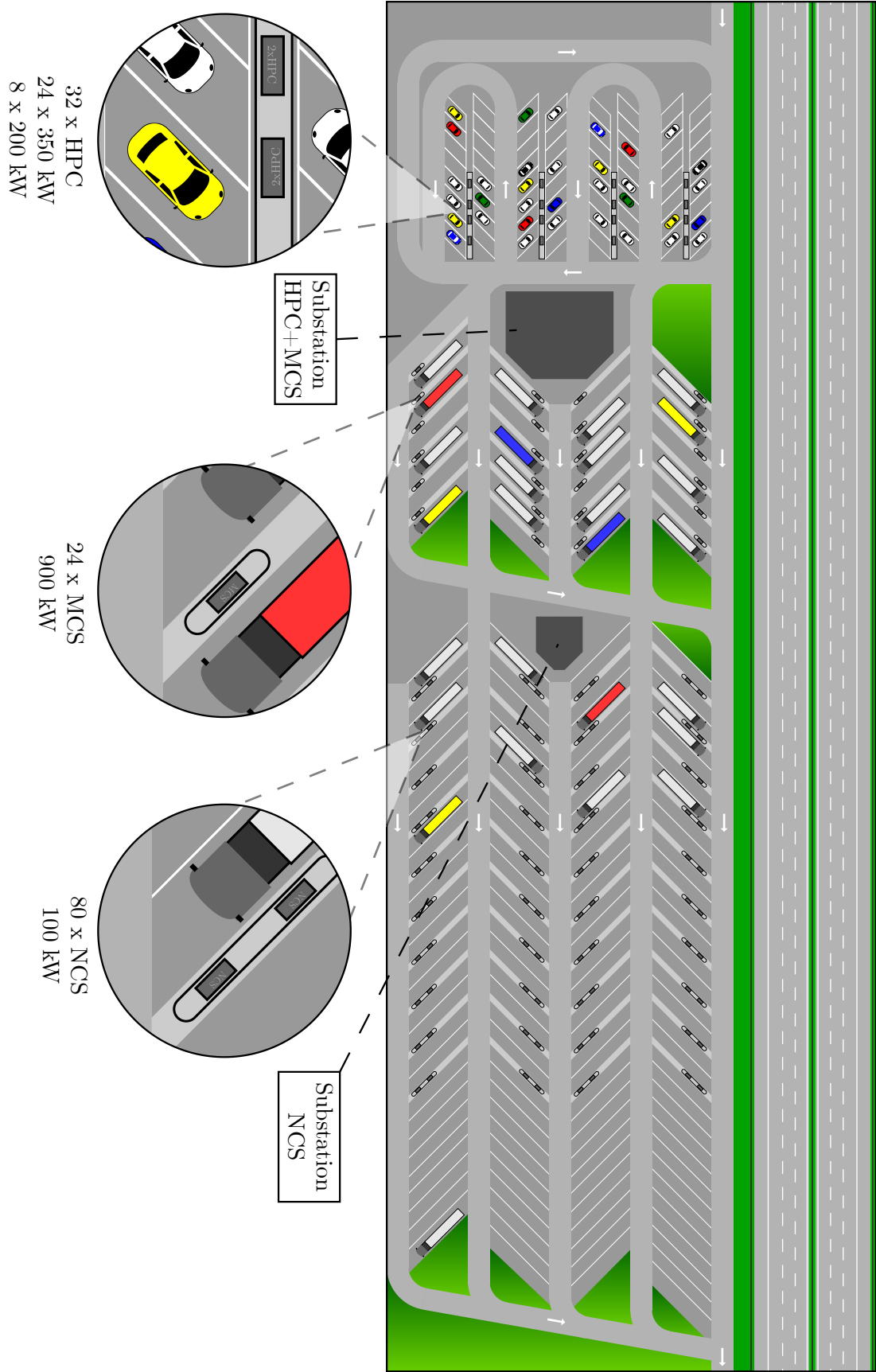


Figure 3.3 – Example layout (Layout 2) for a charging park in a highway service area in 2035 for Scenario 1. The three different charging systems MCS, HPC and NCS are physically separated and supplied by two substations. As conventional vehicles will still be in use, parking areas without chargers are also considered.

3.2 Power distribution within the charging park

Due to the high number of charging points and the defined size of the vehicle parking spaces, the distances from the substation to the charging points are relatively long. Since very high power levels have to be transmitted, the choice of distribution grid plays an important role in terms of the amount of conductor material required, relative cost and overall efficiency.

3.2.1 Distribution grid types

Three different types of power distribution grids are considered in this work: AC grid, cables connecting centralized chargers to dispensers on the charging port and DC distribution grid. Fig. 3.4 shows an overview of the different types. The substation is connected to the

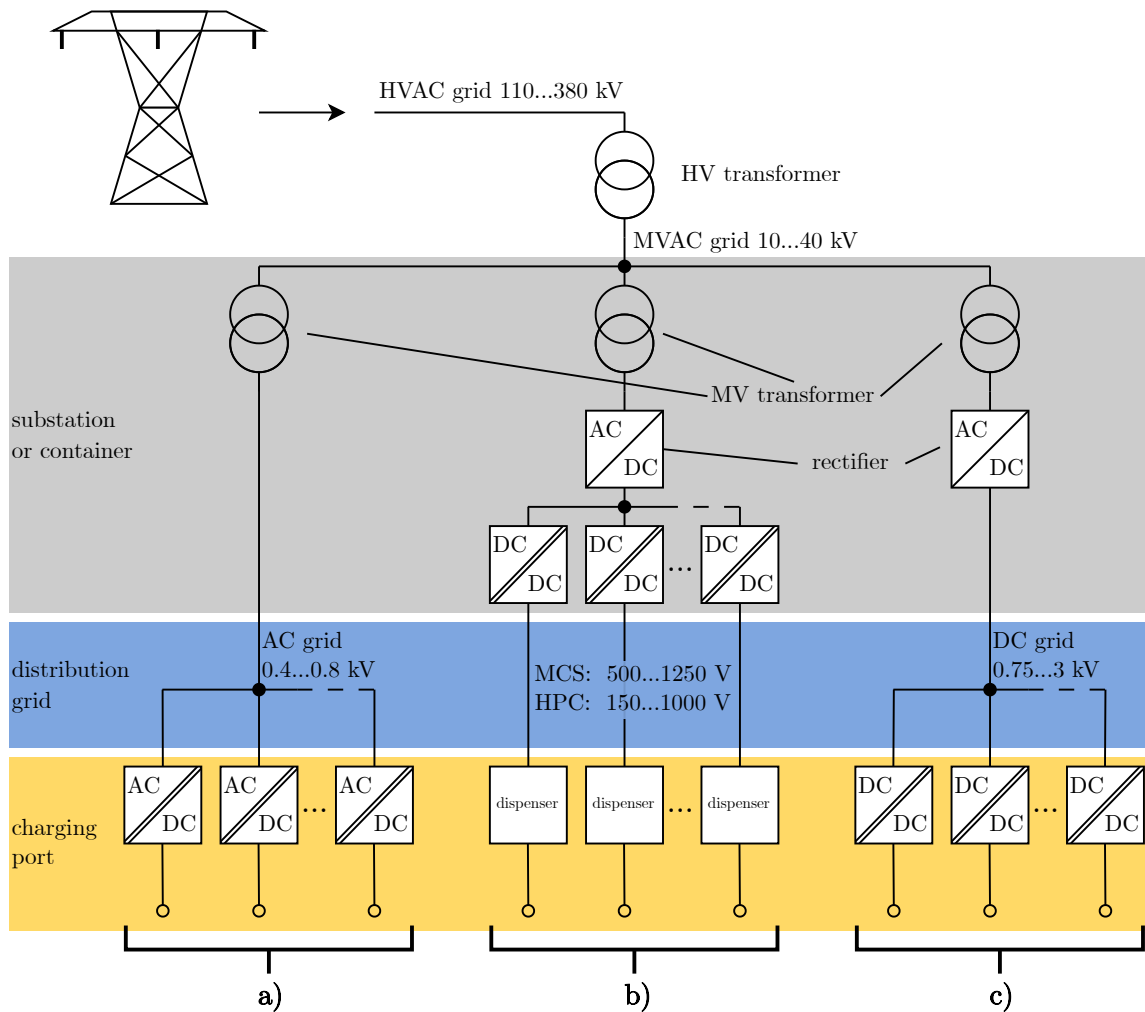


Figure 3.4 – Block diagram for the different power distribution concepts for the power coming from the high voltage grid via the chargers going to the EVs. The different distribution grid types are: AC grid (a), dispenser solution (b) and DC grid (c).

three-phase medium-voltage (MV) AC grid, therefore all of the three different types have a

50 Hz MV transformer to bring the voltage down to the required level. The power electronic converters and their position differ between the concepts, while the last component in the chain, the charging cable, is again the same for all three types.

a) AC distribution grid with AC-DC converters at the charging port

The first type of the considered distribution grids is a three-phase AC grid. Here, only the medium voltage transformer is located in the substation, from which cables (or bus bars) lead to the charging points where the chargers are located. Each charger consists of an AC-DC converter and an isolated DC-DC converter and is then connected to the EV via the charging cable. The advantages of the AC distribution grid are the well-known concept of AC grids and the availability of the widely used components such as cables and protection devices. Another advantage is, that most of the state-of-the-art fast chargers for the EU market are designed for three-phase 400 V AC and could be directly integrated. In this case the demand for copper would be high, due to the high power and relatively low voltage (which is why higher AC voltage levels are also being investigated). Another disadvantage is that this decentralized charger solution requires the space for the converters to be on the charging point, which could result in a lower density of charging lots and even longer distance to the substation. For a better comparison between the grid types it is assumed for the further investigation, that the latter is not the case and that the distances are the same for all three distribution grid types.

b) Central charging units with dispensers at the charging port

In this concept a central rectifier unit (AC-DC converter) converts the incoming AC voltage to a DC voltage. This DC link supplies the DC-DC converters of the chargers, one converter per charging port is needed. Cables run from the substation to the dispenser modules on the charging port. The dispensers consist of, among other things, one or more charging cables (each connected to the chargers in the substation) and devices to communicate with the EV and the charger. Central charging units with long charging cables to the vehicle are already common for power distribution in bus depots. In the remainder of this work, this type of power distribution will be referred to as dispenser solution. Since the converters are centrally located, the system is easy to maintain and monitor. Cooling can be kept simpler, because the converters are indoor and do not have to withstand external environmental conditions. Furthermore, there are already existing solutions (as a slightly different solution also current 400 V AC input fast chargers could be used, since the low voltage cables can be kept short). The cables from the substation to the dispensers are relatively long due to the distance and since the voltage cannot be increased (the voltage on the cables equals the battery voltage of the EV), the cross section and therefore the amount of conductor material needed is higher for longer distances.

c) DC distribution grid with DC-DC converters at the charging port

The third type of distribution grid considered in this work, is a DC grid (with different voltage levels taken into account). As with the dispenser solution a central rectifier is located in the substation after the MV transformer. From there, a DC grid leads to the individual charging

points, where one DC-DC converter per EV performs the voltage and power conversion and is connected to the EV through the charging cable. The advantage over the AC grid is, that the space requirement on the charging port is lower due to the single converter stage and compared to the dispenser solution that the voltage can be increased to reduce conductor material. A further advantage of the DC grid is that the integration of renewable energy sources such as solar power is easier, since the need for multiple conversion steps (DC to AC and back to DC) is eliminated [42, 43]. There are currently no off-the-shelf solutions available, especially for higher DC voltages and the availability of protection circuitry for DC grids is less than for AC grids.

3.2.2 Central AC-DC converter

A large central rectifier is assumed for the two distribution grid types dispenser solution and DC grid. The exact implementation of this converter is not discussed further here, but there are two different basic concepts with for converting the AC output voltage of the MV transformer to a DC voltage. The first concept is an active rectifier with power factor correction, which actively suppresses the mains harmonics and can actively regulate the DC voltage. The second, usually less expensive solution for the AC-DC converter is a passive diode rectifier. By adapting the MV transformer to multiple secondary windings, 12- or 24-pulse rectification can also be realized for lower grid harmonics compared to the 6-pulse rectifier [44, 45]. 12- and 24-pulse rectifier are usually standard in unidirectional high power industrial applications.

3.2.3 Reduction of the maximum total power

In [32] different approaches to reduce the maximum total power of the charging park drawn from the supply grid have already been investigated. The aim is to keep the power rating of the MV transformer as low as possible and, if possible to avoid the installation of a new HV transformer. The greatest potential is shown by an intelligent charging management of the MCS chargers (schedule charging sessions so that not all chargers are running at the same time, which is possible, because the charging power is sufficient to charge the required energy in 30 minutes during the 45-minute break). A second option to reduce the installed grid connection is to eliminate temporary peaks by using a battery storage. For the presented distribution grid types, an integration of such a storage would be relatively simple for the dispenser solution and the DC grid by using a DC-DC converter to integrate the batteries into the respective DC link. For the AC grid, an additional (bidirectional) AC-DC converter would be required. Another possible solution could be the use of bidirectional chargers. In this case the charge management could be further improved by also allowing negative charging power (using the energy from one EV battery to charge another). For example, this could be accomplished by using the truck batteries on the NCS chargers when their SOC and the charging time are sufficient. For the AC grid, the AC-DC and DC-DC converters must then be bidirectional. For the other two grid types, only the DC-DC converter needs to be bidirectional, since the total power consumption for the charging park is assumed to be always positive.

3.3 Comparison of the different distribution grids

This section examines the three different distribution grids presented previously. The evaluation is done on the basis of the charging park of the highway service area in the three different scenarios. For each scenario, the two different layouts are investigated. A very important criterion for comparing the different grid types is the cost. Since the power electronic converters are not taken into account in this first step, they are mainly driven by the conductor material, insulation and protection. For the sake of simplicity, only the cost of the conductor material is considered here. For this purpose, the conductor lengths and the voltage-dependent cross sections must be determined.

3.3.1 Distribution grid voltage

Since the power is fixed for the three charging park scenarios, the voltage of the distribution grid is a key parameter in determining the required cross section and therefore the amount of conductor material needed. Different voltage levels are considered for the different distribution grid types.

AC grid

For the three-phase AC grid three voltage levels are considered: 400 V, 690 V and 800 V. The 400 V voltage level is the most common standard voltage for low to medium power distribution grids and industrial applications. Most state-of-the-art chargers rely on a 400 V AC front end and the protection devices are readily available. For higher power industrial equipment the three-phase 690 V AC voltage level is standard. The cross section for the cables in the 690 V grid can be reduced by a factor of three compared to the 400 V grid for the same power. Although the 800 V grid is not yet standard, it is already being used for high power applications and for collection grids within large scale photovoltaic installations [46]. Current AC-DC (and DC-AC) converters are mostly available for these three voltage levels. Converters for higher AC voltages are usually designed for higher power (>1 MW) and therefore not feasible for this application, since the relatively low power NCS chargers will also be connected to this distribution grid.

Dispenser solution

Since the voltage of the distribution grid for the dispenser solution is the same as the battery voltage, it is not possible to vary the voltage levels. The cross section of the conductors is calculated for a voltage of 800 V. This voltage is chosen because it is in the range for the MCS standard and it is assumed that the full power for MCS and NCS is usually not required at the very low end of the voltage range. In that case higher cable losses and temperature rise (boost charging) could be accepted. Since the maximum current for CCS2 is limited to 500 A, the maximum power for a HPC charger can be reached at 700 V (for the 350 kW power level considered here). Therefore, the chosen voltage of 800 V for dimensioning the cable cross section is also assumed to lead to useful results.

DC grid

The voltages considered for the DC grid are 750 V, 1500 V and 3000 V. The 750 V voltage level is already widely used in industrial applications and in urban transportation systems. 1500 V DC represent the maximum value for low voltage DC applications in Germany and is already used in solar parks. The 3000 V level is also widely used for railway systems throughout Europe. Therefore, protective devices are already available for these voltage levels.

An overview for the different voltage levels considered for the three distribution grid types is shown in table 3.2.

Table 3.2 – Voltage levels investigated for the different distribution grid types

Grid type	Voltage 1	Voltage 2	Voltage 3
AC grid	400 V	690 V	800 V
dispenser solution	800 V		
DC grid	750 V	1500 V	3000 V

3.3.2 Combined length of the conductors in the distribution grid

The second parameter needed to determine the amount of conductor material required is the length of the conductors. This is largely determined by the geometry of the different charging park scenarios and layouts. As described above, Layout 1 has a single substation and the distance between the charging units and the substation increases as the charging power decreases. This means that the MCS chargers are closest to the substation, followed by the HPC chargers, and the NCS chargers are furthest away. Layout 2 has two substations, one for the MCS and HPC fast charging systems and a second for the NCS chargers. The layout is designed for the shortest possible distance from the substation to the chargers. The arrangement of the charging points differs for the different scenarios. In Scenario 1, which requires the highest number of charging units, the charging park is divided into four lanes. For Scenarios 2 and 3, the number of lanes is assumed to be two and one, respectively. This lane division is already shown in fig. 3.3 for Scenario 1.

Layout 1 assumes a distance of 10 m between two charging points, with two chargers at each charging point. For simplicity, no distinction is made between the charging systems, i.e. the distance between two charging points for HPC is the same as for MCS and NCS. The distance from the substation to the first charging point is estimated with 20 m, the same for all lanes. These distances are shown in Fig. 3.1.

For Layout 2, which is probably more realistic, the arrangement of the charging points is different. Here, there is one charger per charging point for MCS and again two each for HPC and NCS. The first substation is placed between MCS and HPC. The distance between two charging points are 8 m for MCS, 6 m for HPC and 12 m for NCS, while the distance from the first charging point to the substation is again assumed to be 20 m (see fig. 3.2).

The type of distribution grid used also plays a large role in calculating the total length of conductors required. For the three-phase AC grid, three conductors must be considered. For the dispenser solution, two conductors are required, but here each conductor must be routed

from the substation to the respective charging point, which means that the total length of the conductors significantly exceeds that of the other grid types. The two conductors DC+ and DC- are required for the DC grid. Protective conductors, neutral conductors (possibly needed for the AC grid) and cables for communication (with the dispenser) are not taken into account. The charging cables (on the EV side) are also assumed to be the same for all three distribution grid types and therefore not considered in this comparison.

3.3.3 Demand for conductor material

Copper is considered the conductor material here, but other materials such as aluminum are also conceivable. The basic idea behind the calculation of the copper requirement is that the losses per unit length are kept constant. For this purpose, a distribution grid efficiency of $\eta_{\text{distr}} = 0.997$ for maximum charging power is assumed for all grid types.

For all chargers i of the different distribution grid types $x \in \{DC, disp, AC\}$, the required cross section for the conductor is calculated. For the AC grid, it is assumed that the conductors are implemented in such a way, that the skin effect and other AC-specific loss effects are reduced to a negligible level (e.g. by using multiple isolated and twisted parallel conductors). The permissible loss of the conductor depends on the power $P_{\text{ch}}(i)$ of the respective charger and is calculated to

$$P_{\text{cu}} = \frac{l_x(i)}{\sigma_{\text{cu}} A_x(i)} \cdot I_{\text{ch},x}^2(i) = (1 - \eta_{\text{distr}}) P_{\text{ch}}(i), \quad (3.1)$$

with the specific conductance for copper σ_{cu} and $I_{\text{ch},x}(i) = P_{\text{ch}}(i)/V_x$. For the three-phase AC grid, $V_x = \sqrt{3} \cdot V_{\text{LL}}$ to get the current for one phase. The length of the conductor $l_x(i)$ is the distance from the substation to the respective charger.

Solving 3.1 for $A_x(i)$, the required cross section

$$A_x(i) = \frac{n_{\text{ph},x} \cdot l_x(i) \cdot I_{\text{ch},x}^2(i)}{\sigma_{\text{cu}} \cdot (1 - \eta_{\text{distr}}) P_{\text{ch}}(i)} \quad (3.2)$$

can be calculated. The number of phases $n_{\text{ph},x}$ for the respective grid type increases the cross section, because the permissible losses are assumed for all phases together. Since these equations calculate the mass of the copper by assuming that each charger is directly connected to the substation, they are only valid for this purpose. For the AC and DC grid, there would be only one bus per lane connecting the chargers and the cross section would decrease as the distance to the substation increases. By summing up the resulting copper volume for all chargers, the total mass of the required copper for the type of distribution grid

$$m_{\text{cu},x} = \rho_{\text{cu}} \cdot n_{\text{ph},x} \cdot n_{\text{lanes}} \cdot \sum_i A_x(i) \cdot l_x(i), \quad (3.3)$$

with the density of copper ρ_{cu} and the number of lanes n_{lanes} for the different scenarios are calculated.

Figure 3.5 shows a simplified illustration of how the total copper required is calculated. With a total number of n charging points and the distance between the charging points $l_{\text{CP-CP}}$ (different for MCS, HPC and NCS in Layout 2) the total length can be calculated. As already described the cross section results from the maximum allowed losses in the conductor (0.3 % of the installed power of the charging point).

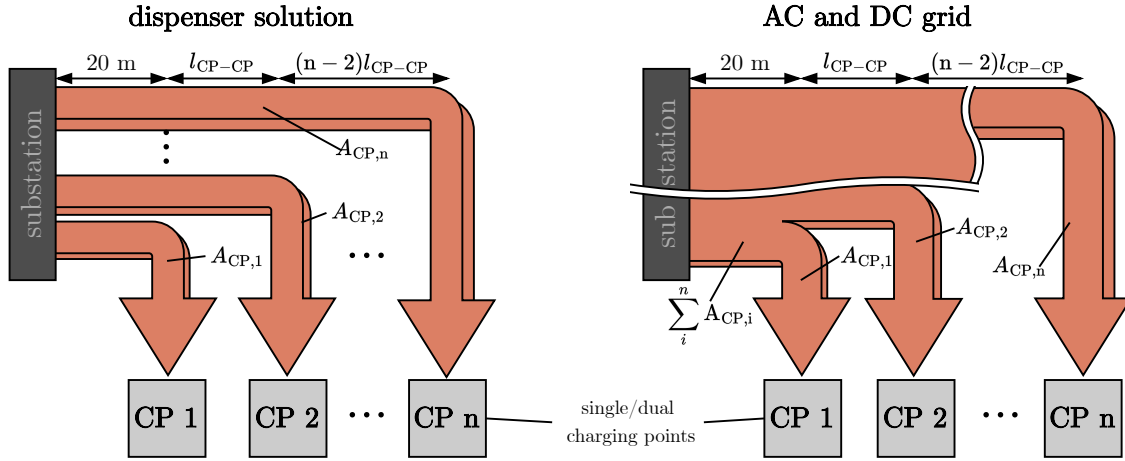


Figure 3.5 – Simplified illustration of the conductors from the substation to the charging points for the different distribution grid types. While for the dispenser solution each charging point has an individual connection to the substation with a constant cross section, for the AC and DC grid the conductors are combined. However, this aggregation does not affect the resulting copper demand.

Comparison of the copper demand in the different types of distribution grids

To compare the different distribution grid types, the mass of copper required is calculated for each voltage level in each scenario. Fig. 3.6 shows the different amounts of copper required in the different distribution grids for the voltage levels and scenarios considered (the calculation steps can be found in the appendix in A.3). Layout 2 is optimized for conductor length and therefore the copper demand is lower in each case. It can also be seen, that it is higher for Scenario 3 than for Scenario 2, even though the installed charging power is only half of that of Scenario 2. This is due to the fact, that the same NCS power has to be covered with a single lane. Therefore a different layout for Scenario 3 might be a better solution, e.g. moving the position of the substation to the center of the NCS lane.

Due to the quadratic dependence of the losses on the current, the mass of copper for the AC and DC grid is quartered when the voltage is doubled. Therefore, the difference between best and worst case is more than a factor of 50. If the only consideration was the mass of the copper required, the voltage could be chosen as high as desired. However, due to the cost of the insulation and possible shielding material required for EMC (not considered here), this voltage is limited upward. Another factor is the transformer in the power electronic converter, whose cost increases with higher isolation voltages.

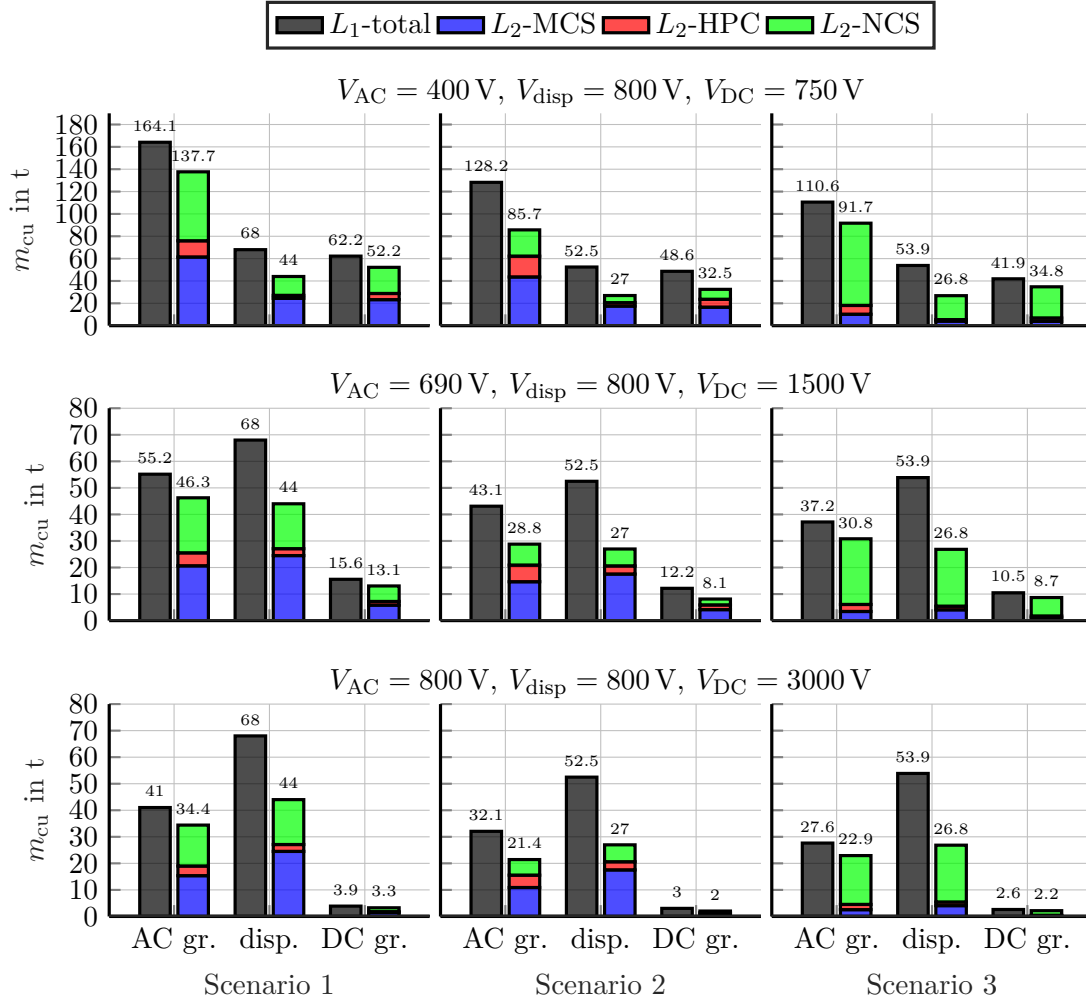


Figure 3.6 – Copper demand m_{cu} of the distribution grid for the different grid types (AC gr., disp., and DC gr.), scenarios and voltage levels. For the dispenser solution the voltage and therefore the copper mass remains the same, while for the other two grid types the voltage increases from top to bottom. For Layout 1 (L_1) only the total copper mass is shown, while for L_2 also the share between the different charging systems is shown.

3.3.4 Power electronics in the different distribution grids

If only the need for conductor material is considered, the decision as to which distribution grid to use is strongly biased towards higher voltages. However, there are other factors that influence the overall cost of the charging system, so the power electronic converters are considered here in a second step.

AC-DC converter

In [32] the simultaneity factor is assumed to be 0.5 for the MCS chargers and one for HPC and NCS. Taking advantage of this, the AC-DC converter for the dispenser solution and for the DC grid can be designed for lower power. Depending on the scenario, this results in a

reduction of the AC-DC converter power rating by 19 % to 27 %. This fact, together with the high demand for copper, is the reasons for excluding the AC distribution grid for the remainder of this work.

DC-DC converter

Using the modular approach presented in the next chapter, the DC-DC converters could be the same for all three distribution grid types, since the installed power is the same. Therefore, the cost of the DC-DC converters would be the same for all three types.

However, for the dispenser solution, as for the AC-DC converter, it is possible to reduce the installed power by taking the advantage of the simultaneity factor for the MCS chargers. This could be achieved with a matrix of contactors inside the substation. As it is not possible to define which MCS chargers will be used simultaneously, this does not apply to the other two types of distribution grid.

DC-DC converter transformer and protection in the DC grid

The transformer in the DC-DC converter needs to isolate the EV battery from the DC grid. According to [21], a double or reinforced insulation is required between these two voltages. This requires a guaranteed partial-discharge-free operation, which increases the amount of insulation material required and therefore the cost, especially at higher voltages. Partial discharge is the most common reason for insulation failures in transformers [47]. Special attention must be paid to high frequency transformers in power electronic converters [48]. Even with the modular approach (series connection of two or more DC-DC converters), the isolation capability must withstand the full voltage between the primary and secondary side resulting from this connection. Therefore, the cost of the transformer in the DC-DC converter increases as the DC grid voltage increases. The main reason for this is size, and therefore material requirements in the core and winding, due to the increasing distance required between the two windings, rather than the cost of the insulation material itself. This dependence of the transformer cost on the insulation voltage is considered negligible compared to the overall cost of the DC-DC converter and is therefore not included in the comparison. An overview of the required test to ensure partial-discharge-free operation is given in A.1.

In general, the cost of protection for DC grids depends on the protection scheme used and on the required reliability of the grid [49, 50], a comparative review and analysis is done in [51]. Due to the star topology of the DC grid in this work and the assumed unidirectional power flow, the protection for the DC grid can be simplified. Because the cost of protection devices for different voltage ratings varies widely (mostly due to the number of units sold of today's standard voltages), prices are not truly comparable. If melting fuses are used for protection, the cost is again negligible compared to the cost of the DC-DC converter and is not considered further in this work.

3.3.5 Comparison of the dispenser solution and the DC grid

The AC distribution grid cannot compete with the other two types in the considered aspects. Therefore, the two types of distribution grid dispenser solution and DC grid are compared in terms of total costs.

Figure 3.7 shows the combined cost of the DC-DC converters and the copper in the distribution grid for the three scenarios in dependency of the DC grid voltage. It can be seen that above a certain voltage the DC grid has a cost advantage over the dispenser solution, even though the absolute cost of the MCS DC-DC converters is twice as high (the cost of the HPC and NCS DC-DC converters is the same for the two grid types). For this assumption, the specific costs $c_{\text{cu}} = 10 \text{ €/kg}$ and $c_{\text{DC-DC}} = 23 \text{ €/kW}$ are assumed for copper and the DC-DC converters, respectively. This simplification does not include the cost of the additional contactors and any protection circuits and is highly dependent on the specific costs assumed. Further, the potentially lower lifetime of the DC-DC converters compared to the grid is not taken into account. It is worth noting, that the savings differ for the different scenarios, e.g. for Scenario 2 the two types of distribution grid are almost equal in terms of total cost from a DC grid voltage of around 1500 V.

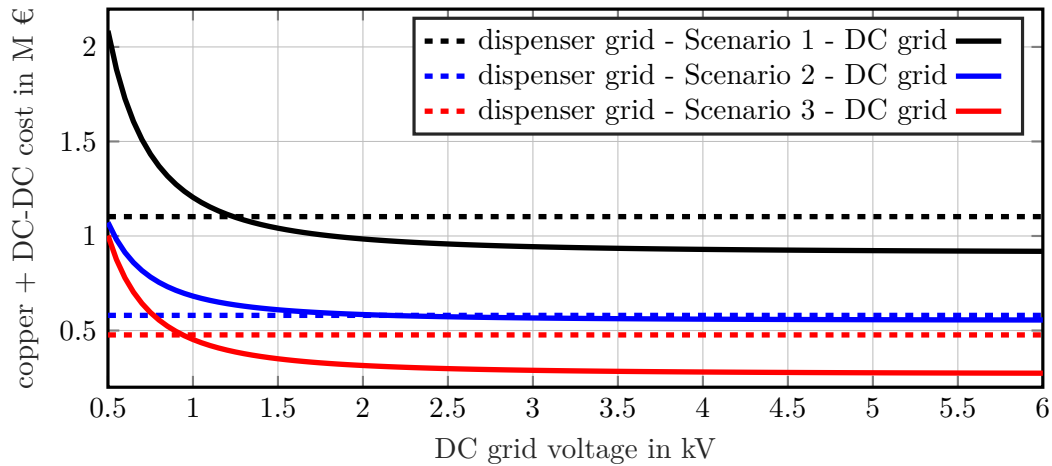


Figure 3.7 – Combined cost of the copper in the distribution grid and the DC-DC converter for the two types DC grid and dispenser solution in the three different scenarios with the cost assumptions $c_{\text{cu}} = 10 \text{ €/kg}$ and $c_{\text{DC-DC}} = 23 \text{ €/kW}$. Due to the simultaneity factor for the MCS chargers the number and therefore the cost of the DC-DC converters is lower for the dispenser solution. As the DC grid voltage increases, the savings in copper costs outweigh this cost advantage.

The 750 V DC voltage level is inferior to the dispenser solution and can only compete with the 400 V AC grid in terms of copper demand. It is therefore sub-optimal for this high power application and most likely for MCS charging at all. The only advantage over the dispenser solution could be in HPC charging for 400 V battery type EVs.

This leaves the three options of dispenser solution, 1500 V, and 3000 V DC grid. As it can be seen in figure 3.7, the DC grid offers higher total cost savings compared to the dispenser solution for both voltage levels in two out of three scenarios. This, together with the scalability

in voltage for higher power levels and longer distances between the substation and the charging point, leads to a decision in favor of the DC grid.

There are several practical reasons for using the 1500 V DC grid. On the one hand, there are the current technical standards. Since the upper limit for low voltage in Germany is 1500 V, the low voltage standards still apply for this voltage and are clearly defined in terms of protection. Furthermore, the electrical charging standard for conductive DC systems IEC 61851-23 [21], also only applies to EV supply equipment with a maximum supply network voltage of 1000 Vac or 1500 Vdc. This also means that the voltage of 1500 V must not be exceeded in the real application, resulting in an effectively lower voltage on the grid. On the other hand, a wide power range of chargers (NCS, HPC and MCS) is to be integrated into the DC grid, and chargers with higher input voltages are only economical from a certain power level, because the share of fixed costs (e.g. the auxiliary circuits) for the converter and thus c_{DC-DC} increases (this effect will also be visible in the results of chapter 5).

These points lead to the choice of the 1500 V DC grid for further calculations in this work.

3.4 Conclusion

In this chapter a system analysis is performed based on the study of [32], considering charging parks on different scenarios of highway service areas. With the power levels for the chargers from this study, two different layouts have been studied for three different types of distribution grids: AC grid, dispenser solution, and DC grid. To compare them, the conductor material requirements are calculated for different voltage levels and an assessment is made for the power electronics (AC-DC and DC-DC converters).

The results show that the AC grid is the least suitable distribution grid type for these high power levels. A more detailed comparison between the dispenser solution and the DC grid is performed, resulting in the decision to proceed with the DC grid in this work. This is due to its advantages in terms of cost effectiveness and scalability compared to the dispenser solution. Mainly due to practical reasons such as technical standards, the 1500 V DC grid is chosen, which makes the 1500 V the system voltage considered in this work.

Outlook

In the future, it is expected that the limits of the low voltage standard will shift upward, or that there will be a separate standard for a "low" medium voltage, as medium voltage is currently understood to be up to 60 kV (AC) [52]. This adaptation of the current standards can enable a more resource efficient power distribution not only for EV charging applications, but also for grid integration of high power renewable energy sources.

For longer distances and/or higher power (e.g. increased number of chargers or higher power MCS chargers), voltage levels of 3000 V or more may be reasonable. As electrification continues beyond 2035, especially for trucks, power levels will continue to increase. A possible application can be the direct integration of the chargers into an existing urban or rural future medium voltage DC grid.

4 Analysis of high-power DC-DC converters

Starting from this chapter, the focus of this thesis will be exclusively on the DC-DC converters (shown in fig. 4.1) connected to the 1500 V DC grid on the input side and to the EV on the output side. First, a brief introduction to DC-DC converters and system configurations for multiple connected converters is given. Then the topologies that will be studied in this work are introduced and the analysis methods for each topology are presented. For each topology, the procedure for dimensioning the active and passive components is described, providing the basis for the automated DC-DC converter design in the next chapter.

In this work, the naming of the system variables is chosen so that V_{DC} describes the voltage of the DC grid and V_{EV} the voltage on the vehicle side. The same index is used for currents and power. For the individual DC-DC converter modules, only the unidirectional power flow (charging of the vehicle) is considered, therefore the variables are referred to as input and output (e.g. V_{IN} and V_{OUT}).

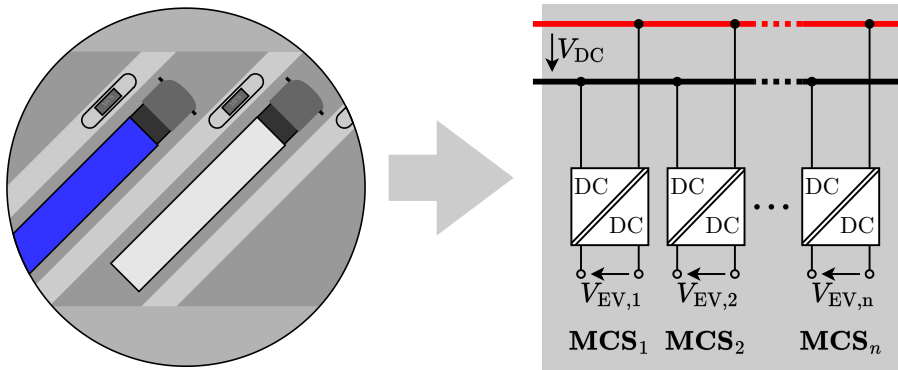


Figure 4.1 – MCS charging lane (left) and the high-power DC-DC converters connected to the DC distribution grid with $V_{DC} = 1500$ V (right)

Figure 4.1 shows the MCS charging lane from the highway service area from chapter 3 and the block diagram for the DC-DC converters, connected to the DC distribution grid.

4.1 Isolated DC-DC converters in a modular system

As the name implies, DC-DC converters either convert one DC voltage or current to another DC voltage or current, and/or are used to provide galvanic isolation between the two DC connections. Accordingly, DC-DC converters are divided into isolating and non-isolating converters [53]. As an isolation between the DC grid and the EV is required for safety (see section 2.1), the focus is on isolated DC-DC converters. The concept common to all isolated DC-DC converters is DC-AC - Transformer - AC-DC. Fig. 4.2 shows the block diagram

and an unidirectional realization example of this operating principle. The frequency of the square-wave voltage of the DC-AC converter (inverter) for high-power DC-DC converters is usually within a range of 1 kHz to 500 kHz, sometimes even higher. Due to this medium frequency the transformer of the DC-DC converter can be realized many times smaller compared to a 50 Hz mains transformer, saving weight, volume and cost [54, chapter 5].

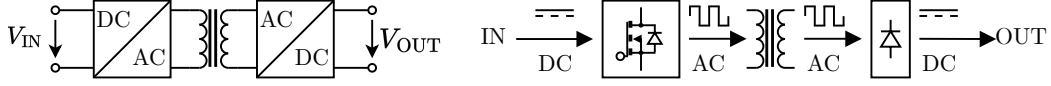


Figure 4.2 – Isolated DC-DC converter: block diagram on the left and unidirectional realization example on the right

Four different isolated DC-DC converters for high-power applications are presented and analyzed in the following sections. These are: Phase Shift Full Bridge (PSFB) converter, LLC converter, Dual Active Bridge (DAB) and Two-Stage Converter (TSC).

4.1.1 System configuration

An important advantage of isolated DC-DC converters is the possibility of a independent modular interconnection of the primary and secondary sides of multiple converters. This allows a higher voltage capability in the case of series connection and a higher current capability in the case of parallel connection. Fig. 4.3 shows a general block diagram of DC-DC converter units with primary sides connected in series and secondary sides connected in parallel. This system can be used for example to charge an electric vehicle from a DC grid. Since the topologies in this work are to be investigated with semiconductors with different blocking voltages, several system configurations are considered.

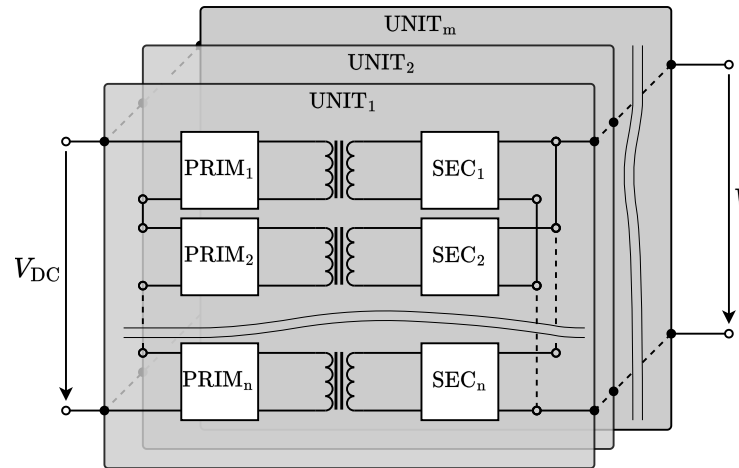


Figure 4.3 – Example for a modular interconnection of isolated DC-DC converters to achieve higher power levels. Parallel connected units containing DC-DC converters with series connected primary sides and parallel connected secondary sides.

4.1.2 Switchable secondary sides

A common state-of-the-art concept for DC-DC converters for EV charging is to have a variable switchable configuration of the secondary side. For this purpose, two isolated secondary sides are connected either in parallel or in series using controllable switches (e.g. relays). This enables a high current capability in the case of parallel connection and a high voltage capability in the case of series connection. Fig. 4.4 shows the block diagram of such a system in both parallel (a) and series configuration (b) for the secondary sides.

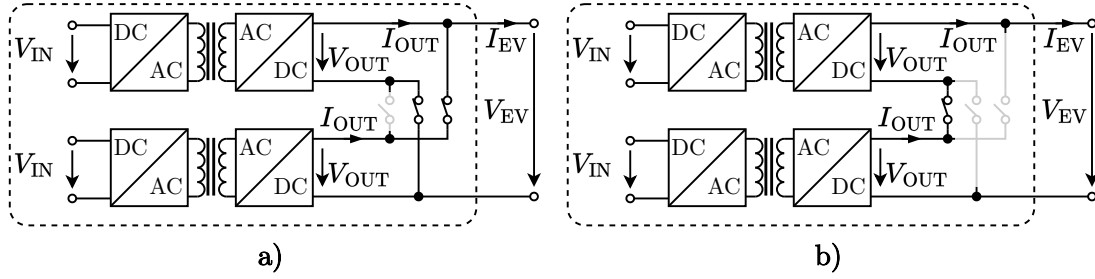


Figure 4.4 – Isolated DC-DC converter system with switchable secondary side configuration: a) parallel and b) series connection of the secondary sides. The primary sides can be connected either in parallel or in series.

Depending on the maximum converter output current $I_{OUT,max}$ and output voltage $V_{OUT,max}$, it may occur that the maximum output power cannot be achieved over the entire desired output voltage range. If $V_{OUT,max} < P_{EV,max}/I_{OUT,max}$, the maximum power that can be achieved is less for lower voltages in series configuration, resulting in a dip in the maximum system power curve. Fig. 4.5 shows example maximum system power curves for different maximum converter currents and voltages with and without this dip in the maximum output power.

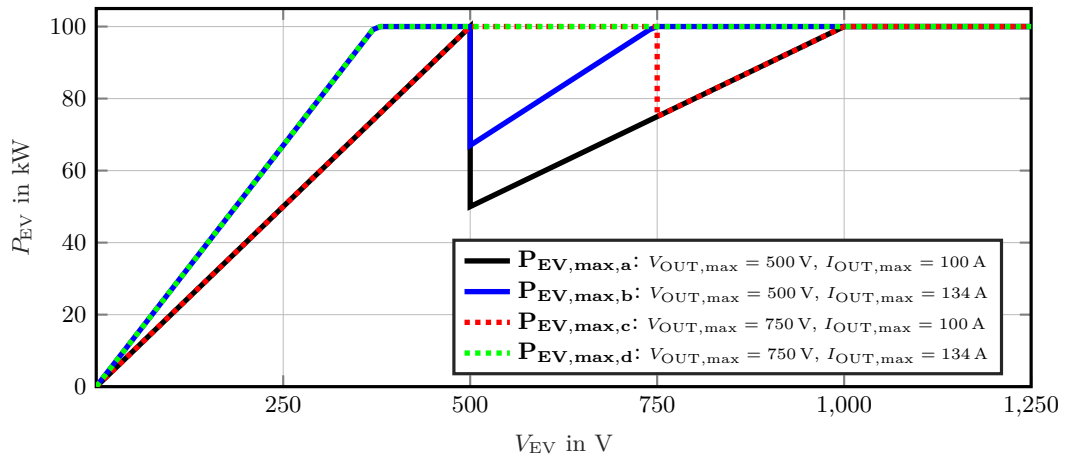


Figure 4.5 – Output curves for an example isolated DC-DC converter system with switchable secondary-side configuration and a maximum output power of $P_{EV,max} = 100$ kW: maximum system power curves for different maximum converter currents and voltages

Fig. 4.6 shows the output curves of an example system with switchable secondary sides for the CCS and MCS voltage ranges, capable of providing full output power in series configuration. The maximum output current is assumed to be constant for the low voltages ($V_{\text{OUT}} < P_{\text{OUT,max}}/I_{\text{OUT,max}}$) and the maximum output power $P_{\text{EV,max}}$ therefore depends on the output voltage.

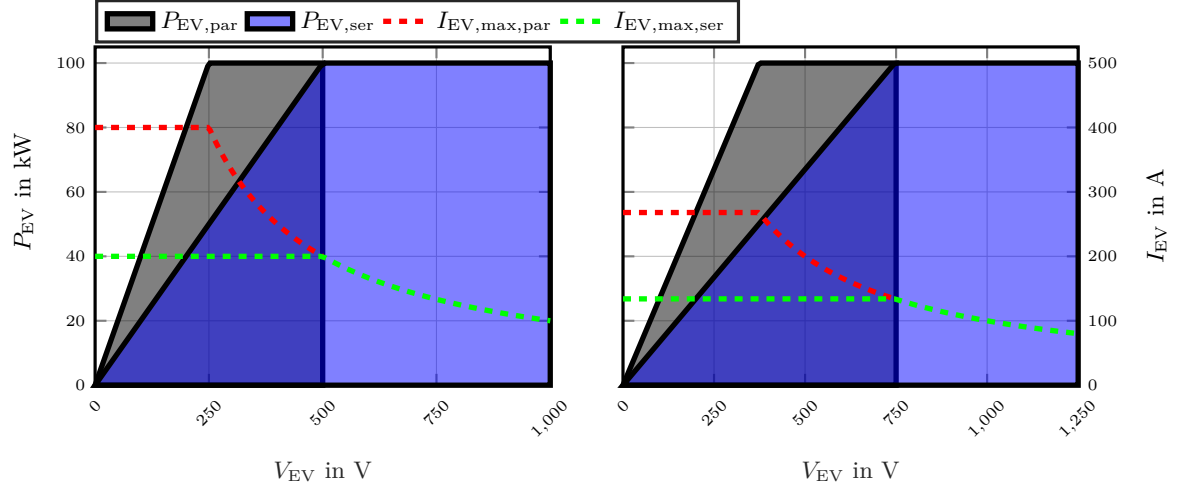


Figure 4.6 – Output curves for a maximum output power of $P_{\text{EV,max}} = 100 \text{ kW}$: left: power range and maximum current for a CCS system with a maximum converter output voltage of $V_{\text{OUT,max}} = 500 \text{ V}$ and a maximum output current of $I_{\text{OUT,max}} = 200 \text{ A}$, right: power range and maximum current for a MCS system with $V_{\text{OUT,max}} = 750 \text{ V}$ and $I_{\text{OUT,max}} \approx 134 \text{ A}$

Since this ability to deliver full output power over the full voltage range is not always required, many chargers currently available will accept this for cost reasons. For this work, it is assumed that the maximum output power can be delivered over the entire MCS voltage range.

4.1.3 Isolated DC-DC converter topologies for high-power

Four different isolated DC-DC converter topologies suitable for this high-power charging application are introduced and analyzed in the course of this chapter. Table 4.1 gives an overview of the four topologies investigated in this work. The operating principles of the

Table 4.1 – Overview of the different DC-DC converter topologies

Name	Description
PSFB converter	Phase-Shift-Full-Bridge converter
LLC converter	LLC resonant converter
DAB	Dual Active Bridge
TSC	Two-Stage Converter

different topologies are explained below. For each topology several different configurations are theoretically possible, such as different phase legs (half bridge, full bridge, three phase, three level), different rectifier stage (voltage/current doubler, active rectifier). In this work, only the full-bridge configurations using MOSFETs are considered.

Analysis of the system variables and dimensioning of the passive components

The first step in analyzing the different DC-DC converter topologies is to calculate the currents through and the voltages across the individual components of the circuits. Referred to as system variables, they vary widely between the different topologies, depend on the operating point, and are required to fully design the active and passive components of the converter.

The passive components for each topology are then discussed. The dimensioning of all the passive components shown in the circuit diagrams is described by finding analytical dimensioning rules. Passive components for EMC filters on the input and output side, as well as the DC-link capacitor C_{IN} are not taken into account here. Assuming that the differences between these components not considered in the four topologies are negligible, the design guidelines presented are sufficient for a fair comparison of the four topologies, which will be done in the next chapter.

4.2 PSFB converter

The name of the PSFB converter consists of two parts. The first part, "phase shift," refers to the modulation technique employed for output regulation. The second part is derived from the use of a full bridge on the primary side and, in this case, also on the secondary side. The PSFB converter is classically used in applications with higher input (400 V to 800 V) and lower output voltages (up to 48 V) in the power range of less than one kW to a few kW (usually in the secondary current doubler topology) [55]. However, there are more and more applications in the higher power and voltage range [56], and the PSFB converter is now also a widely used DC-DC converter topology in the field of EV charging.

4.2.1 Converter operating principle

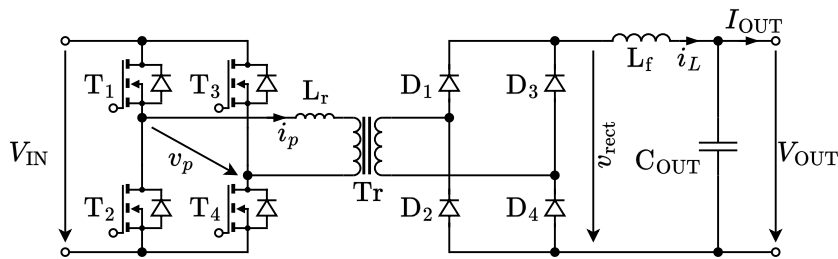


Figure 4.7 – Basic circuit diagram of the PSFB converter

Figure 4.7 shows the schematic of the PSFB converter with a diode rectifier. Here and in the following, only the PSFB converter with a full bridge on both sides will be discussed. The two primary-side half bridges consisting of T_1 and T_2 as well as T_3 and T_4 switch with a duty cycle of 50 % each. To control the output (voltage, current, or power), the phase position of

the two half bridges is shifted against each other. If resistive, inductive, and diode voltage drops are neglected, the output voltage of the PSFB in continuous conduction mode is

$$V_{OUT} = 2ps \cdot n \cdot V_{IN}, \quad (4.1)$$

where $n = n_s/n_p$ is the transformer turns ratio and ps is the phase shift of the two primary-side half bridges. No phase shift means that no voltage is applied to the transformer Tr and therefore no energy transfer takes place. Full phase shift ($ps = 0.5$) means that a square wave voltage is applied to the transformer with $\pm V_{IN}$ and therefore the maximum output voltage ($V_{OUT} = n \cdot V_{IN}$) is achieved. The phase during which voltage is applied to the transformer is called the energy transfer phase, while the phase with no voltage across the transformer is known as the freewheeling phase. Voltage and current waveforms for the PSFB converter are shown in the analysis later in fig. 4.9.

Active rectification

The secondary-side diodes ($D_{1..4}$) in the PSFB converter can be replaced with MOSFETs. This allows the voltage drop across the diodes to be substituted by the ohmic behavior of the reverse-conducting MOSFET. This way, the efficiency of the converter can be increased, especially at partial load. Fig. 4.8 shows the PSFB converter with the active rectification through MOSFETs ($T_{5..8}$).

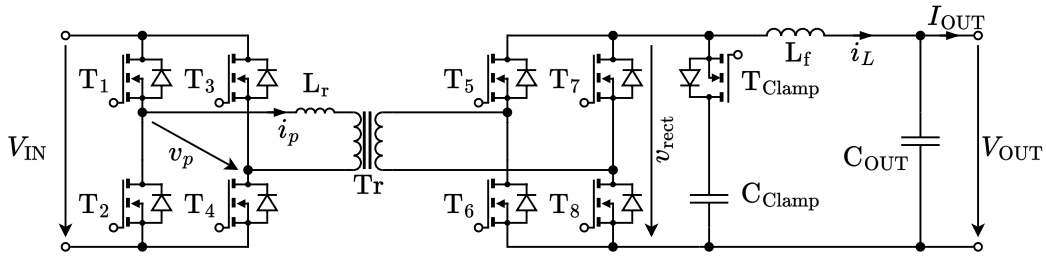


Figure 4.8 – Circuit diagram of the PSFB converter with active rectification through MOSFETs and active clamping circuit to reduce overvoltages caused by parasitics

The control of the secondary-side MOSFETs can be distinguished into three different operation modes [57]:

- Mode 0: Passive rectification via the body diodes (not very useful as body diodes usually have poor conduction characteristics)
- Mode 1: MOSFETs are turned on during energy transfer from primary to secondary side (ideal diode behavior)
- Mode 2: Similar to Mode 1 with an extended on-time to conduct also during freewheeling, resulting in lowest losses

Through this active rectification circuit a bidirectional operation would be possible [58], although not investigated here.

Since the different topologies will be compared in the following chapter and the comparison should be as fair as possible, the same semiconductors are used. For this reason, and due to

the lower availability of high-power diodes at higher frequencies compared to MOSFETs, the active rectification is assumed for the PSFB converter.

Active clamping

The parasitic capacitance C_T of the transformer and the MOSFETs output capacitance C_{OSS} (not shown in the circuit diagram), together with the stray inductance L_r cause a ringing across the rectifier. This yields in high voltage overshoots at the secondary-side semiconductors that could potentially destroy them [59]. To protect these semiconductors, a clamping circuit is required. There are different types of clamping, the easiest being an RCD-snubber [60]. Since the resistor of the snubber circuit has to absorb the whole energy from the overshoot, the overall efficiency decreases. A more efficient way is to retrieve this energy from the clamping capacitor to the output capacitor with an active clamping circuit. There are different types of active clamping circuits [61–63]. In this case, the circuit with only one additional switch is used.

In figure 4.8 the additional clamping circuit consisting of the capacitor C_{Clamp} and the MOSFET T_{Clamp} is shown. The energy from the overshoot is stored in the capacitor via the body diode of T_{Clamp} . By turning on the MOSFET, the energy can be recovered and pushed to the output capacitor. At a steady state, the average voltage across the capacitor C_{Clamp} then equals the input voltage reflected to the secondary side ($n \cdot V_{IN}$).

4.2.2 System variables of the PSFB converter

For the automated converter design in the next chapter, the currents and voltages for all components in the PSFB converter must be calculated. Two main operating modes have to be considered: continuous (CCM) and discontinuous (DCM) conduction of the secondary-side inductor current i_L . The current and voltage waveforms can be described as piecewise linear functions. The following calculations are derived from [55]. Fig. 4.9 shows the switching states of the primary-side phase legs (leg A consists of T_1 and T_2 and leg B of T_3 and T_4) and the voltage and current waveforms for an example operating point in CCM. For all of the following equations it is assumed that the magnetizing inductance is negligible ($L_m \gg L_r$). The first step is to calculate the knots of the primary-side transformer current i_p . Using $D = \frac{V_{OUT}}{n \cdot V_{IN}}$ and $L_{res} = L_r + L_f/n^2$, the auxiliary variable I_L can be calculated with

$$I_L = \frac{D \cdot t_p}{2} \cdot \frac{V_{IN} - V_{OUT}/n}{L_{res}}. \quad (4.2)$$

The given operating point is in CCM when the condition

$$\frac{P_{OUT}}{D \cdot V_{IN}} \geq \frac{I_L}{2} \quad (4.3)$$

is met, and in DCM if it is not. This allows the first knot of the waveform

$$I_{p,act} = \begin{cases} 0 & \text{for DCM} \\ \frac{P_{OUT}}{D \cdot V_{IN}} - \frac{I_L}{2} & \text{for CCM} \end{cases} \quad (4.4)$$

of the primary-side current i_p to be calculated. The second knot $I_{p,\text{off},B}$ determines the switch-off current for leg B and is therefore required for the switching loss calculation.

For the two different modes, $I_{p,\text{off},B}$ results in

$$I_{p,\text{off},B} = \begin{cases} I_L & \text{for DCM} \\ I_{p,\text{act}} + I_L & \text{for CCM.} \end{cases} \quad (4.5)$$

The next knot ($I_{p,\text{off},A}$, switch-off current for the phase leg A) is calculated by

$$I_{p,\text{off},A} = \begin{cases} 0 & \text{for DCM} \\ I_{p,\text{off},B} - \frac{t_\alpha V_{\text{OUT}}}{n \cdot L_{\text{res}}} & \text{for CCM} \end{cases} \quad (4.6)$$

with

$$t_\alpha = \frac{V_{\text{IN}} \cdot t_p \cdot \frac{1-D}{2L_r} - I_{p,\text{off},B} - I_{p,\text{act}}}{V_{\text{IN}}/L_r - \frac{V_{\text{OUT}}}{n \cdot L_{\text{res}}}} \quad (4.7)$$

and determines, together with other parameters, the switching losses in leg A. It can be seen that the switched currents, and therefore the switching losses, are generally different for the two phase legs.

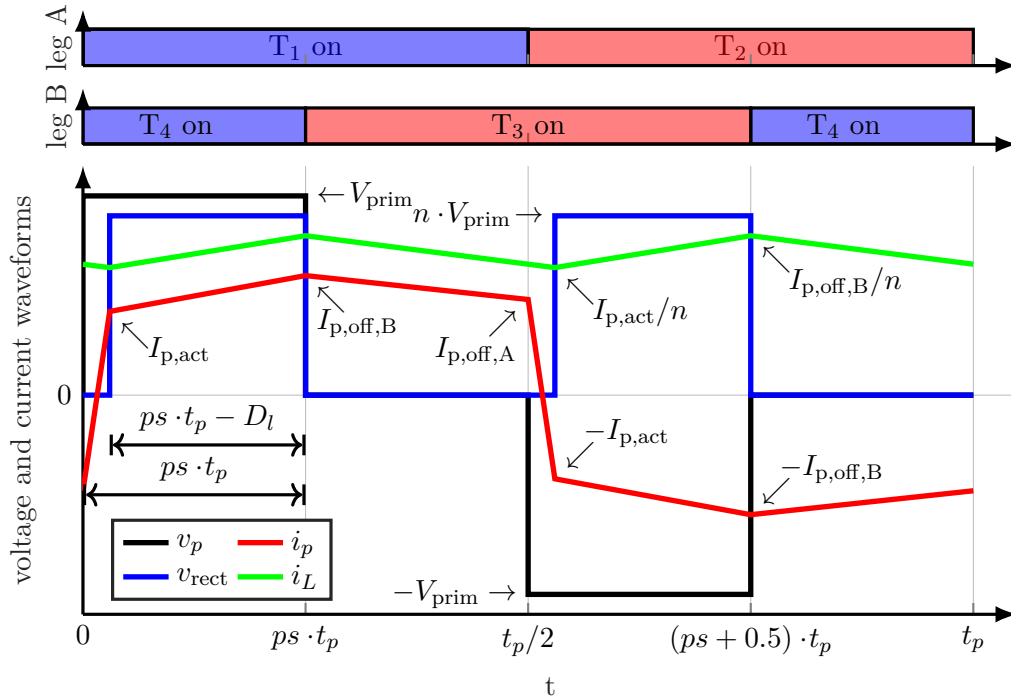


Figure 4.9 – Switching states and voltage and current waveforms for the PSFB converter for an example operating point in continuous conduction mode. The two phase legs operate at a duty cycle of 50% and the phase is shifted by $ps = 0.25$. The waveform plot shows the voltage v_p between phase legs A and B, the rectified voltage v_{rect} on the secondary side, the primary-side current i_p and the output inductor current i_L . The waveforms are piecewise linear and can be described by the marked knots connecting the linear segments.

The respective currents through the MOSFETs on the primary side can be determined by multiplying the primary-side current i_p by the switching state (off = 0 and on = 1) of the respective switch. Similarly, the current through the output inductor i_L can be derived from the knots $I_{p,act}$ and $I_{p,off,B}$ of the primary-side current by reflection on the secondary side. There is an additional knot for the DCM: As soon as the current reaches zero, it remains at zero until the next positive edge of v_{rect} and then increases linearly to $I_{p,off,B}/n$ again.

The current through the output capacitor C_{OUT} is equal to the AC component of the inductor current when the capacitor voltage ripple is neglected:

$$I_{Co} = i_L - I_{OUT} \quad (4.8)$$

Duty cycle loss

The rate of rise and fall of the primary-side current at the times $t = k \cdot t_p/2$ for $k \in \mathbb{N}$ is limited by the remagnetization of L_r and therefore depends on the input voltage V_{IN} and L_r . During this time, which is required for remagnetization, no energy can be transferred via the transformer. This time is referred to as duty cycle loss D_l and increases with increasing output current. To compensate for D_l , a slightly higher phase shift, depending on the output current must be applied to reach the same output voltage $ps = D + D_l$. The duty cycle loss can be estimated to [55]

$$D_l = 2L_r \frac{I_{p,off,A} + I_{p,act}}{V_{IN} \cdot t_p} \quad (4.9)$$

with the previous determined currents. Since the PSFB converter cannot step up, the resulting limited maximum output voltage must be considered in the design.

ZVS

For fig. 4.9 the dead time between the switches of a phase leg is not considered. In the real converter, however, this dead time is necessary. On the one hand, the dead time must compensate for the limited turn-on and turn-off times of the switches in order to avoid bridge short circuits. On the other hand, the parasitic output capacitors of the switches (and winding capacitance of the transformer) can be recharged by the circulating freewheeling current during this dead time. If these capacitors are fully charged during the dead time, the on-turning switch can turn on at zero voltage, this is referred to as a complete ZVS, while only partial recharging results in an incomplete ZVS. For a complete zero voltage turn on of the switch in the respective leg, the freewheeling energy must meet the condition [64]

$$E_{Lr,A/B} = \frac{1}{2} L_r I_{p,off,A/B}^2 \geq \left(\frac{4}{3} C_{OSS} + \frac{1}{2} C_T \right) V_{IN}^2 \quad (4.10)$$

with the output capacitance of the switch C_{OSS} and the parasitic winding capacitance of the transformer C_T .

4.2.3 Passives of the PSFB converter

For the PSFB converter the considered passives are transformer Tr , output filter inductor L_f and output capacitor C_{OUT} .

The two design parameters for the transformer are the turns ratio $n = n_s/n_p$ and the stray inductance L_r . As described in 4.2.2, L_r influences the duty cycle loss D_l and therefore the maximum achievable output voltage. Therefore,

$$n \geq \frac{V_{OUT,max}}{V_{IN,min} - V_{drop}} \quad (4.11)$$

has to be set large enough to transfer the minimum input voltage to the maximum output voltage and to compensate for the voltage drop V_{drop} across all components, including switches and ohmic and inductive voltage drops. Since these depend on the other components, V_{drop} can be estimated and treated as constant in order to simplify the dimensioning of the transformer. Since the value of the stray inductance L_r of the transformer is highly dependent on the geometry and the distance between primary and secondary side, as well as the exact number of turns, the transformer has to be fully designed. The resulting value for L_r can then be calculated and checked if $L_{r,min} \leq L_r \leq L_{r,max}$, where $L_{r,min}$ indicates the minimum inductance required to achieve ZVS from a certain power level and $L_{r,max}$ the maximum inductance to still reach the desired maximum output voltage at full power. Furthermore, the transformer should be designed so that the magnetizing inductance $L_m \gg L_r$ (no air gap).

The parameters to calculate the inductance of the output filter inductor L_f are the maximum permissible ripple current diL (in % of the maximum output current) and the switching frequency f_{sw} . The inductance is calculated to

$$L_f = ps_{Lf} \cdot \frac{nV_{IN} - V_{OUT}}{f_{sw} \cdot \Delta I_{Lf,max}}, \quad (4.12)$$

where $\Delta I_{Lf,max} = diL \cdot I_{OUT,max}$ is defined here as peak to peak ripple current and the phase shift ps_{Lf} is approximated by $ps_{Lf} = \frac{P_{OUT,max}}{2nV_{IN} \cdot I_{OUT,max}}$ (D_l is neglected). This means that L_f is designed at the minimum voltage for the maximum output power $V_{OUT,Lf} = P_{OUT,max}/I_{OUT,max}$.

The minimum output capacitance, in order not to exceed the maximum allowable output voltage ripple $\Delta V_{OUT,max}$ can be calculated to [64]

$$C_{OUT,min} = \frac{\Delta I_{Lf,max}}{16f_{sw} \cdot \Delta V_{OUT,max}} \quad (4.13)$$

and therefore $C_{OUT} \geq C_{OUT,min}$ can be chosen.

4.3 LLC converter

The LLC converter, well known from low to medium power applications, is increasingly being used for higher power applications. The name (LLC) comes from the resonant tank, which consists of the two inductors L_r and L_m and the capacitor C_r . Although it is also available in a non-isolated version, the LLC converter is usually designed with a transformer, forming an isolated DC-DC converter.

4.3.1 Converter operating principle

The two primary-side phase legs of the LLC converter, as for the PSFB converter, operate with a duty cycle of 50 %. The phase shift is always at $ps = 0.5$, applying a square wave voltage of $\pm V_{IN}$ to the resonant tank. The output is controlled by varying the frequency of this square wave voltage. Different frequencies result in different voltage gains of the resonant tank and thus different output voltages can be set. Since the converter can be operated over a wide range with zero voltage switching (ZVS) on the primary side and zero current switching (ZCS) on the secondary side, high switching frequencies are possible, which in turn leads to a reduction in the volume of the passive components. Fig. 4.10 shows the schematics of the full-bridge LLC converter with a full-bridge diode rectifier.

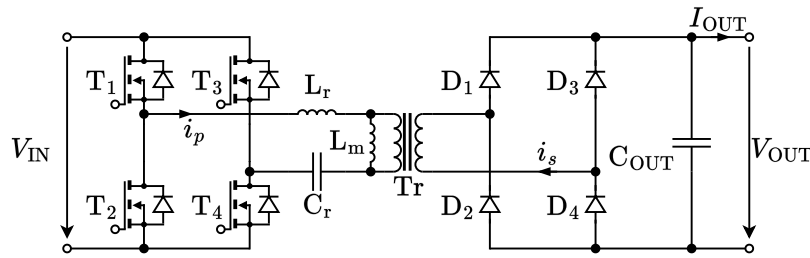


Figure 4.10 – Circuit diagram of the full bridge LLC converter with full bridge rectifier

Figure 4.11 shows an example voltage gain curve for the resonant tank of the LLC converter as a function of the switching frequency. The gain also depends on the load condition. At the resonant frequency $f_{sw} = f_r$ the voltage gain of the resonant tank is one for all loads. ZVS for the primary-side switches can only be achieved in the inductive region, therefore the capacitive region should be avoided. In the inductive region, a switching frequency higher than the resonant frequency ($f_{sw} > f_r$) results in a lower output voltage (buck mode) and a switching frequency lower than the resonant frequency results in a higher output voltage (boost mode).

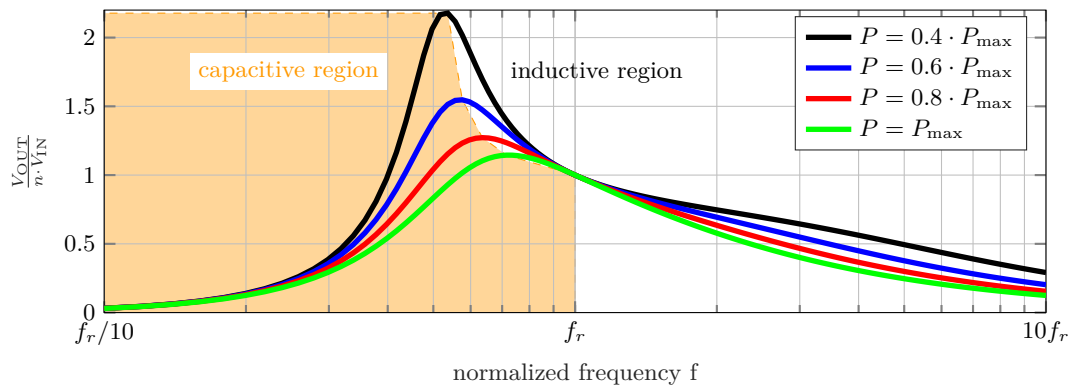


Figure 4.11 – LLC converter resonant tank (gain over frequency) curve for different power levels. When operated in the inductive region the output voltage decreases with increasing frequency.

Half-bridge configurations (primary and secondary) of the LLC converter are also widely used, especially for lower power applications. The functional principle is the same, but these will not be considered further here due to the high-power levels.

Active rectification

The LLC converter allows active rectification by replacing the secondary-side diodes with MOSFETs, providing the same benefits as for the PSFB converter. However, the control of the switches is much more complicated, because, on the one hand, a different frequency is applied depending on the operating point, and on the other hand, the phase shift between voltage and current (also depending on the operating point) varies. In principle, there are three ways to control the active rectification in LLC converters by calculating the switch-on and switch-off times of the rectifier using [65]:

- Current measurement
- Voltage measurement
- Operating point dependent calculation

The current sensing versions measure either directly the current through the MOSFETs or the secondary-side AC current. In the former case, the MOSFET is turned on when the body diode would be conducting and turned off when it is not. However, this requires a current sensor in the commutation path, which leads to higher switching overvoltages due to increased parasitic inductance, and is therefore usually not suitable for higher power applications. In the second case, the AC current i_s is measured and the sign is used to decide which two diagonally opposite MOSFETs of the secondary-side full bridge should conduct.

The voltage measurement variant also aims to measure the conduction state of the body diode and turn on the switch accordingly. However, this requires complex measurement technology for the respective switch.

The calculation of the switching times depending on the operating point (different methods are possible) does not require an additional sensor, but is relatively inaccurate due to parasitic effects and component tolerances, especially at low loads. Miscalculation of switching times can result in loss of ZCS, increased reactive currents and, in the worst case, destruction of the switches due to overcurrent.

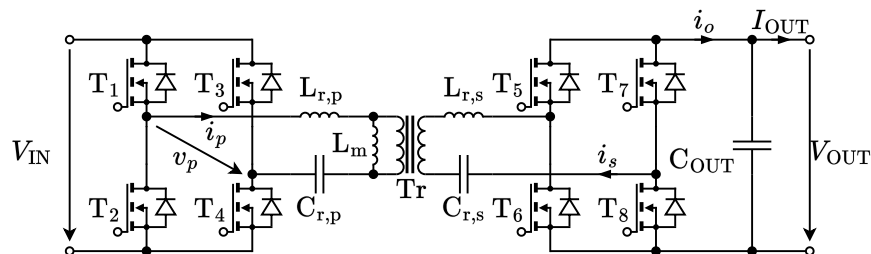


Figure 4.12 – Circuit diagram of the bidirectional CLLC converter

When the resonant tank of the LLC converter with active rectification is divided between primary and secondary side, the result is a so-called CLLC converter. This allows bidirectional operation with buck and boost mode in both directions [66–68]. Fig. 4.12 shows the bidirectional CLLC converter.

4.3.2 System variables of the LLC converter

In terms of determining the system variables, the LLC is probably the most complicated of the four topologies. The most common method of analysis is done with the fundamental harmonic approximation (FHA) [69–72], which assumes purely sinusoidal currents and voltages in the resonant tank. However, as the switching frequency deviates from the resonant frequency, the FHA becomes less accurate because the actual waveforms deviate more and more from the ideal sinusoidal shape. For a LLC converter design, the FHA is usually very sufficient, especially for lower voltage ranges [73], for a more precise analysis of the losses, more accurate methods must be used. For this work the differential equations for the three operation stages (P,N and O) of the converter from [74] operating in six different modes (PO, PON, PN, NP, NOP and OPO) are set and solved for each mode. With that a closed form is achieved and an accurate analysis can be done. The design of the LLC converter is then done with the algorithm described in [75, 76]. Fig. 4.13 shows the calculated primary-side voltage v_p and current i_p waveforms for a example LLC converter design in the different operating modes.

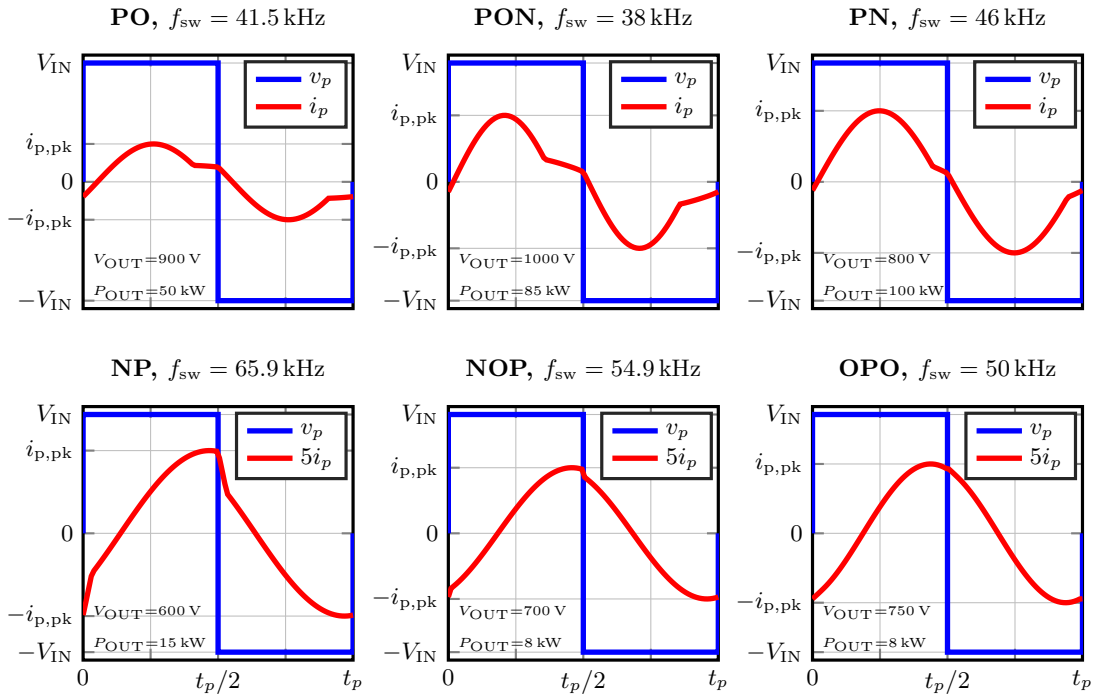


Figure 4.13 – Calculated primary-side currents for the LLC converter using the equations from [74] for the six different operation modes PO, PON, PN, NP, NOP, and OPO for an example LLC converter design with $L_r = 30 \mu\text{H}$, $L_m = 90 \mu\text{H}$, $C_r = 340 \text{ nF}$, $f_r = 50 \text{ kHz}$ and $n = 1$. The input voltage is $V_{\text{IN}} = 750 \text{ V}$.

In fig. 4.14 the equivalent circuit diagrams for the three different operation stages P, N, and O of the LLC converter can be seen.

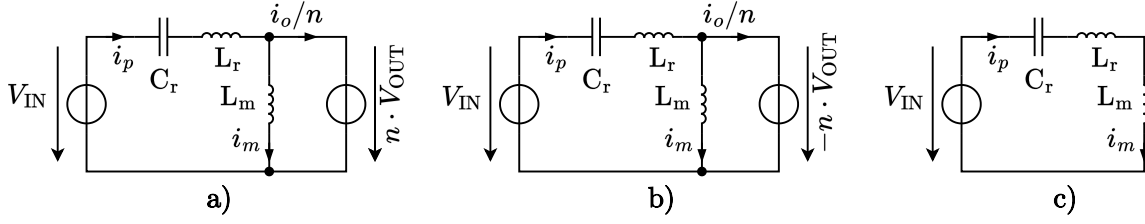


Figure 4.14 – Equivalent circuit diagrams for the three different operation stages of the LLC converter: P (a), N (b), and O (c) according to [74]

4.3.3 Passives of the LLC converter

The values to be determined for the LLC converter passives are the transformer turns ratio n and the values of the resonant tank passives C_r , L_r and L_m .

At rated power the LLC converter achieves its highest efficiency in the range of the rated transformer winding ratio, i.e. around the output voltage point $V_{OUT} = n \cdot V_{IN}$. It is therefore common to choose

$$n = \frac{V_{OUT,nom}}{V_{IN}}, \quad (4.14)$$

so that maximum efficiency is achieved at the point of maximum operating time. Usually it is a good practice to choose $V_{OUT,nom} = 0.5 \cdot (V_{OUT,min} + V_{OUT,max})$.

Since the calculation for the system variables in the LLC converter is so complex that it can only be done with the help of a computer, the dimensioning of C_r , L_r and L_m in this work is also done with MATLAB. Therefore, the design algorithm, presented in [75, 76] is implemented. The input parameters for the algorithm are: n , V_{IN} , V_{OUT} , P_{OUT} , $f_{sw,min}$ and a design space of values for the resonant capacitor C_r . The design algorithm differs for the different modes, but the basic principle is to compute L_r and L_m for each C_r of the design space and check if the solution is valid for all operating points. To find the best design, an optimization has to be done in a second step. In this work all the valid designs are used and the optimization is done for the complete design (active and passive components) as shown in the next chapter.

The calculations are done for the unidirectional topology of fig. 4.10, but can be adapted so that the design is also valid for the bidirectional topology by dividing the L_r and C_r and reflecting it on the secondary side with

$$L_{r,p} = L_r/2 \quad (4.15a)$$

$$L_{r,s} = n^2 L_r/2 \quad (4.15b)$$

$$C_{r,p} = 2C_r \quad (4.15c)$$

$$C_{r,s} = \frac{2C_r}{n^2}. \quad (4.15d)$$

Note: the system variables for the components of the resonant tank are no longer valid in this case, and for the negative power flow (from OUT to IN) the calculations must be done by swapping the two sides (input and output).

4.4 Dual Active Bridge (DAB)

The DAB is probably the most widely used DC-DC converter topology for the upper power range. Unlike the two previously presented topologies PSFB and LLC converter, bidirectional operation is possible with the basic circuit. The DAB is also the topology with the lowest number of components. With a good design, ZVS can be achieved over a large operating range, resulting in high efficiency levels. The name comes from the fact that active full bridges are used on both, primary and secondary side.

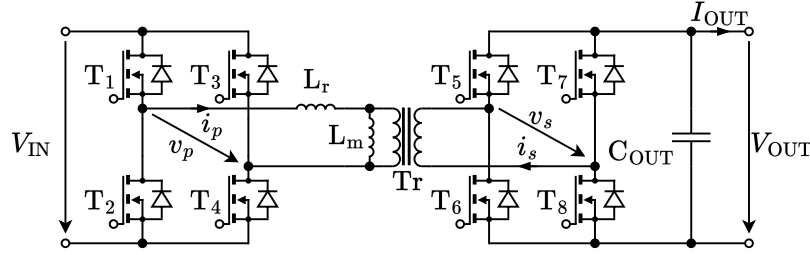


Figure 4.15 – Circuit diagram of the DAB

Fig. 4.15 shows the circuit diagram of the DAB. It features the two full bridges, the inductor L_r and the transformer Tr (L_m is the magnetizing inductance of the transformer). Depending on the required inductance L_r , this can also be integrated into the transformer [77].

4.4.1 Basic converter operating principle

The basic principle of operation of the DAB is two AC voltage sources, one on the primary side and one on the secondary side. By shifting the phase of the two voltage sources with respect to each other a power flow can be set. The four half bridges each switch with a duty cycle of 50% and a phase shift of $ps = 0.5$ between the legs, resulting in a square wave voltage with the amplitude $\pm V_{IN}$ and $\pm V_{OUT}$ on the primary and secondary side, respectively [78]. Figure 4.16a shows the equivalent circuit diagram with the two square wave voltage sources and the inductor L_r . Fig. 4.16b shows the waveforms of the main system variables of the DAB for an example operating point.

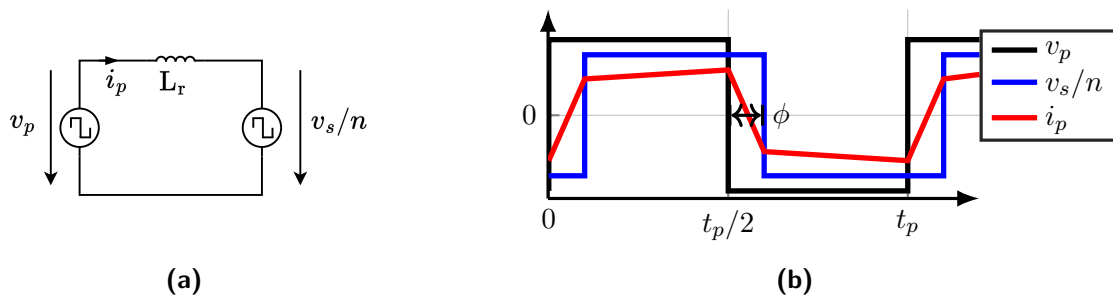


Figure 4.16 – a) equivalent circuit diagram of the DAB with two square wave voltage sources and the inductor L_r and b) example waveforms of the primary-side AC voltage v_p , reflected secondary-side AC voltage v_s/n and primary-side current i_p of the DAB

The switching frequency $f_{sw} = 1/t_p$ is constant and the power flow [79]

$$P_{OUT} = \frac{nV_{IN}V_{OUT}}{2\pi f_{sw}L_r} \left(1 - \frac{\phi}{\pi}\right) \phi \quad (4.16)$$

is controlled by the phase shift ϕ between the primary and secondary-side square wave voltages.

Modulation schemes

There are several types of modulation schemes for the DAB. The first has already been introduced and is generally referred to as Single Phase Shift (SPS) modulation [78, 80]. In this method, both the primary and secondary sides are operated at 50% duty cycle and full phase shift between the two legs, and only the phase shift between the two sides is used to control the power flow. If the phase shift between the two half-bridges on the primary and secondary sides is also varied, i.e. freewheeling is also possible and a zero voltage can be applied to the transformer, two additional degrees of freedom are obtained. This modulation (called Double Phase Shift, DPS and Triple Phase Shift, TPS) can be used to shape the transformer current. In the triangular current mode TRIM, ZCS can be achieved, mainly at lower power levels, to achieve higher efficiencies [81]. Trapezoidal modulation (TRAM) allows a lower RMS value of the transformer current (compared to SPS) and can therefore reduce conduction losses in the switches and winding losses in the transformer (and inductor, if designed as a separate component). For the highest possible efficiency over the entire operating range, a combination of triangular and trapezoidal modulation is the best solution [82, 83]. Therefore, in this work, this combined modulation type is used for the DAB and assumed for all further calculations.

4.4.2 System variables of the DAB

As already mentioned, the waveform of the primary-side current depends heavily on the modulation method. Therefore, to determine this primary-side current waveform, the modulation method (SPS, TRIM, TRAM) must first be determined for the current operating point. In the second step, assuming that the input and output voltage are constant, the switching times and thus the primary and secondary-side voltage waveforms can then be determined. In the third step, the known voltages across L_r can be used to determine the primary-side current i_p and from this the current curves as piecewise linear functions. Since only the TRIM and TRAM modulation methods are considered in this work, only these will be described here. For TRIM, the primary-side current waveform differs in buck ($V_{IN} > V_{OUT}$) and boost ($V_{IN} \leq V_{OUT}$) mode. The primary-side current in TRIM is given by [84]

$$i_p(t) = \begin{cases} \frac{V_{IN}-aV_{OUT}/n}{L_r}t & \text{for } 0 \leq t < t_1 \\ \frac{V_{IN}-aV_{OUT}/n}{L_r}t_1 + \frac{bV_{IN}-V_{OUT}/n}{L_r}(t-t_1) & \text{for } t_1 \leq t < t_2 \\ 0 & \text{for } t_2 \leq t < t_3 \end{cases} \quad (4.17)$$

with the auxiliary variables $a = 1$ if $V_{IN} > V_{OUT}$ and $a = 0$ otherwise, and $b = \lambda$. The voltage drops across switches and parasitics are neglected here, and $L_r \gg L_m$ is assumed.

For TRAM the waveform of the primary-side current can be described as

$$i_p(t) = \begin{cases} \frac{V_{IN}}{L_r} t & \text{for } 0 \leq t < t_1 \\ \frac{V_{IN}}{L_r} t_1 + \frac{V_{IN}-V_{OUT}/n}{L_r} (t - t_1) & \text{for } t_1 \leq t < t_2 \\ \frac{V_{IN}}{L_r} t_1 + \frac{V_{IN}-V_{OUT}/n}{L_r} (t_2 - t_1) + \frac{-V_{OUT}/n}{L_r} (t - t_2) & \text{for } t_2 \leq t < t_3 \\ 0 & \text{for } t_3 \leq t < t_4 \end{cases} \quad (4.18)$$

Since the waveform is symmetric, for the second half of the period i_p from 4.17 and 4.18 can be mirrored around the x-axis as shown in fig. 4.17.

As with the other topologies, the current waveforms for the respective switches can be derived by multiplying the primary-side current by the respective switching state. The switching times $t_{1..4}$ are calculated according to [84].

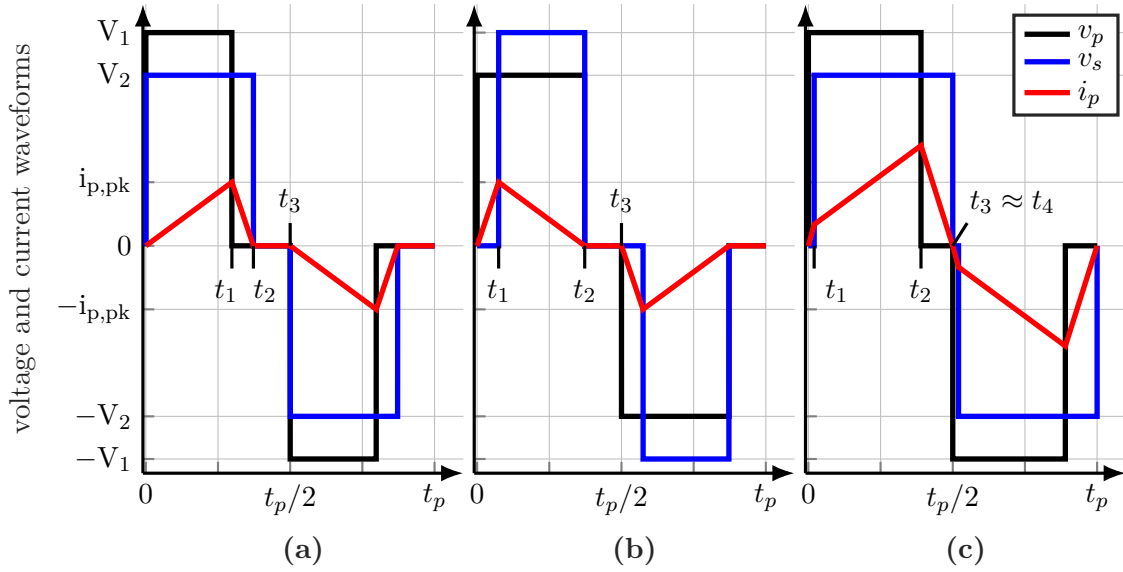


Figure 4.17 – Example voltage and current waveforms for the DAB with different modulation schemes: a) TRIM in buck mode, b) TRIM in boost mode and c) TRAM. The voltages $V_1 = V_{IN}$ and $V_2 = V_{OUT}$ for a) and c) and $V_1 = V_{OUT}$ and $V_2 = V_{IN}$ for b) represent the maximum value of the switched voltages, while $i_{p,pk}$ is the peak value of the primary-side current for TRIM in this example operating point. The transformer turns ratio is assumed to $n = 1$.

Fig. 4.17 shows example waveforms of v_p , v_s and i_p for the different modulation schemes TRIM (buck and boost mode) and TRAM.

4.4.3 Passives of the DAB

The transformer turns ratio n and the inductance L_r in combination with the switching frequency f_{sw} are the main parameters for the design of the passives of the DAB.

The turns ratio for the transformer of the DAB is calculated similar to the LLC converter transformer to

$$n = \frac{0.5 \cdot (V_{OUT,min} + V_{OUT,max})}{V_{IN}}, \quad (4.19)$$

in order to reach maximum efficiency in the middle of the output voltage range.

The design of the inductance L_r is usually done with an iterative approach to get an optimal value. There are three different options to optimize [85]:

- minimum RMS current $I_{p,rms}$
- minimum peak current $I_{p,pk}$
- minimum overall losses

Here, L_r should be optimized for the minimum RMS current, since at this point the other components to estimate the overall losses are not known. SPS modulation is assumed here to ensure operation even in the worst-case scenario. Since

$$I_{p,rms} = \sqrt{\frac{I_1^2 + I_2^2 + I_1 I_2 (1 - 2\phi/\pi)}{3}} \quad (4.20)$$

with $I_1 = \frac{2V_{IN} \cdot \phi/\pi - V_{IN} + V_{OUT}/n}{4f_{sw} \cdot L_r}$, $I_2 = \frac{2V_{OUT}/n \cdot \phi/\pi + V_{IN} - V_{OUT}/n}{4f_{sw} \cdot L_r}$ and

$$\phi = \pi/2 \left(1 - \sqrt{1 - \frac{8f_{sw} \cdot L_r \cdot P_{OUT,max}}{V_{IN} \cdot V_{OUT}/n}} \right), \quad (4.21)$$

the optimal value for minimum RMS current can be found by minimizing the geometrical mean value

$$\min \left(\sqrt{I_{p,rms}^2(V_{OUT} = V_{OUT,min}) + I_{p,rms}^2(V_{OUT} = V_{OUT,max})} \right) \quad (4.22)$$

for the RMS currents at minimum and at maximum output voltage for maximum output power for a given set of L_r . For high-power applications L_r can sometimes be integrated into the transformer as stray inductance, especially for low values of L_r . As for the transformer of the PSFB converter it is assumed that $L_m \gg L_r$.

With the permissible voltage ripple $\Delta V_{OUT,max}$ it is possible to find an analytical solution for the value of the output capacitor

$$C_{OUT} \geq C_{OUT,min} = \frac{I_{p,pk}/n}{2f_{sw} \cdot \Delta V_{OUT,max}}. \quad (4.23)$$

4.5 Two-stage converter TSC

The Two-Stage Converter gets its name from the fact that the two functions, isolation and power flow control, are separated from each other and divided into two blocks. The basic idea behind the TSC is that the isolation stage is always operated at its optimum operating point, minimizing losses in this stage. The second stage has the task of controlling the power flow and can be either a step-up or step-down converter or a combination of the two. Fig. 4.18 shows the circuit diagram of the TSC with active rectifier and dual-interleaved buck converter. The principle of the isolation stage can also be found in the literature in the category of solid-state transformers (SST) under the name DC transformer. The application is always an isolated system, where either no power flow control is required or this is realized by an

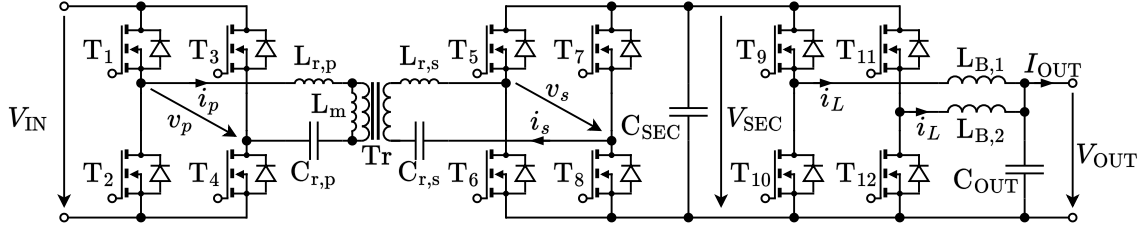


Figure 4.18 – Circuit diagram of the Two-Stage Converter

additional stage before or after the DC transformer [79, chapter 13]. The principles of the DC transformer have already been studied and the behavior is well known [86, 87]. In [88] it is shown that the TSC can compete with the other topologies (CLLC and DAB) in terms of cost and efficiency, which is why it was chosen to be investigated in this work. Also, [89] shows that two-stage converters can have higher a efficiency than single-stage converters.

4.5.1 Converter operating principle

As can be seen in figure 4.18, the isolation stage consists of a LLC (or CLLC) basic circuit. The magnetizing inductance in this case is negligible ($L_m \gg L_{r,p/s}$). The inductors $L_{r,p}$ and $L_{r,s}$ represent the leakage inductance of the transformer Tr . The capacitors $C_{r,p}$ and $C_{r,s}$ compensate for this leakage inductance by bringing the impedance

$$Z_{r,p/s} = j\omega_r L_{r,p/s} + \frac{1}{j\omega_r C_{r,p/s}} \rightarrow 0 \quad (4.24)$$

to zero. The isolation stage is therefore always operating at the resonant frequency $f_{sw,iso} = f_r$. As can be seen in the figure 4.11, the gain of the resonant tank is constant at this point and therefore independent of the load. As with PSFB and LLC converters, active rectification is used here; for an unidirectional variant, a secondary diode rectifier could also be used. Operating at the resonant frequency allows controlled active rectification, eliminating the need for more complex processes (as in the active rectification of the LLC converter). The second stage of the TSC, the buck converter, is designed as a synchronous and therefore bidirectional variant. The basic principle of the synchronous buck converter, which consists of two switches, an inductor and an output capacitor, is that the input voltage is applied to the output by PWM control of the switches over a pulse duration for the top switch that is proportional to the ratio of output to input voltage over one clock period. For the remainder of the clock period, the buck converter is in freewheeling mode (top switch open, bottom switch closed) and the energy stored in the inductor and output capacitor is tapped at the output [90]. For the buck converter from fig. 4.18 the output voltage

$$V_{OUT} = d \cdot V_{SEC}, \quad (4.25)$$

where the duty cycle d is the ratio of on to off time for the top switches $T_{9/11}$. Since with $0 \leq d \leq 1$, $V_{OUT} \leq V_{SEC}$ the output voltage of the buck converter can not exceed the input voltage.

Figure 4.19a shows the characteristic voltage and current waveforms for the isolation stage. Due to the resonant tank, the primary-side current is sinusoidal (a large value is assumed for

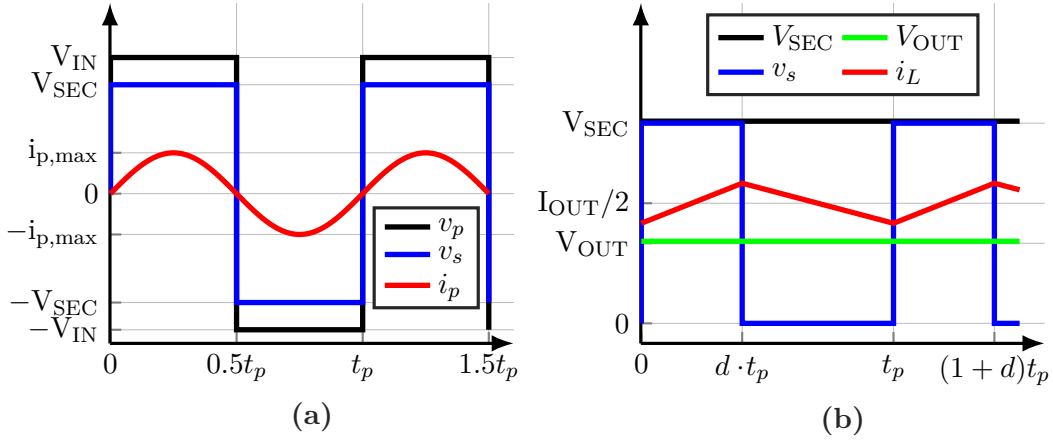


Figure 4.19 – a) characteristic voltage and current waveforms for the isolation stage with primary and secondary-side AC voltage and primary-side current and b) example waveforms for the buck converter for a duty cycle $d = 0.4$

L_m so that the current through L_m can be neglected). In fig. 4.19b the waveforms of the buck converter for an example operating point ($d = 0.4$) can be seen (only the voltage and current waveforms for one of the two interleaved buck converters are shown). In the case of the dual interleaved buck converter, the waveforms of the second leg are phase-shifted by $0.5 \cdot t_p$.

4.5.2 System variables of the TSC

The current and voltage waveforms of the TSC are calculated individually for the two stages. In contrast to the LLC converter, the FHA can be used as a good approximation for the isolation stage, as the converter operates at the resonant frequency and the primary-side current is therefore very close to an ideal sinusoidal shape. In the real converter, a dead time must be inserted between the on states of the high and low side switches of a half bridge. This dead time causes a slight phase shift, resulting in inductive behavior (current lags). This effect can be used to recharge the output capacitance of the MOSFETs and thus to achieve ZVS. Since turn-off losses due to tail currents often dominate in IGBTs, the opposite effect (leading current, capacitive behavior) is more desirable [86, 87]. For this purpose, the converter is then operated at a frequency $f_{sw,iso} < f_r$.

Here the phase shift caused by the dead time t_d is considered for the waveform of the primary-side current. With $i_{p,pk} = \pi/2 \cdot P_{OUT}/V_{IN}$ the primary-side current

$$i_p(t) = i_{p,pk} \cdot \sin(2\pi f_{sw,iso}(t - t_d)) \quad (4.26)$$

can be calculated.

The currents in the buck converter can be derived from the inductor current i_L . CCM is considered here, as for the synchronous buck converter i_L can also be negative for $I_{OUT} > 0$ (and is not clamped to zero). The current through the inductor L_B can be calculated by

$$i_L(t) = I_{OUT}/n_i + \begin{cases} \frac{V_{SEC}-V_{OUT}}{L_B}(t - t_1/2) & \text{for } 0 \leq t < t_1 \\ \frac{V_{SEC}-V_{OUT}}{L_B}(t_1/2) - \frac{V_{OUT}}{L_B}(t - t_1) & \text{for } t_1 \leq t < t_p \end{cases} \quad (4.27)$$

with $t_1 = d \cdot t_p$ and n_i is the number of interleaved buck converters.

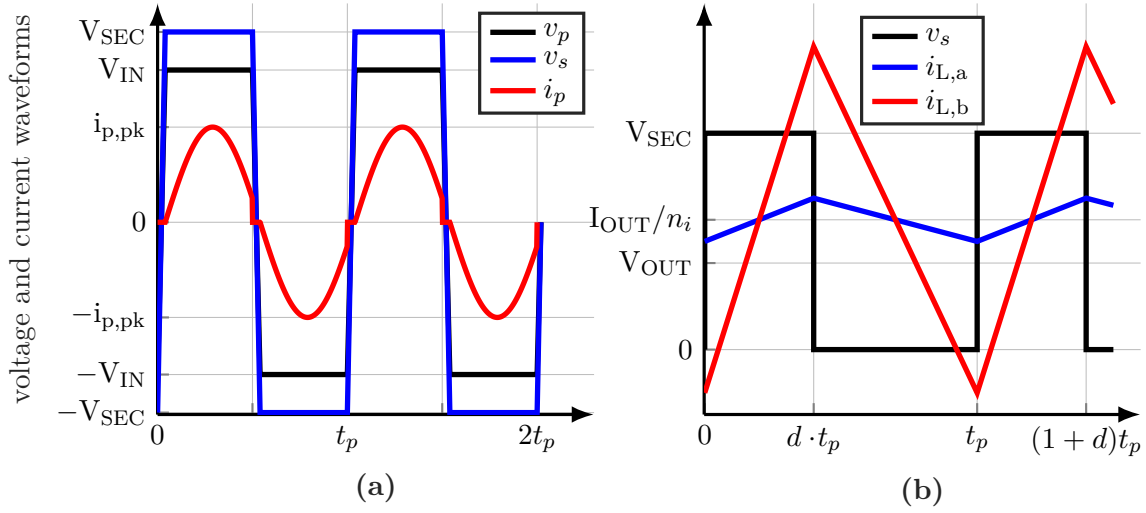


Figure 4.20 – Waveforms for an example operating point for the two stages of the TSC: a) v_p , v_s and i_p of the isolation stage with the slight phase shift of the current caused by the dead time and b) switched voltage v_s and inductor current $i_{L,a/b}$ for two different inductances at the same operating point.

Figure 4.20 shows the Waveforms in the two stages for an example operating point. It can be seen, that the primary-side current i_p drops to zero during the dead time at the zero crossing of the voltages v_p and v_s . Here an ideal charging and discharging of the parasitic output capacitors is assumed, which is why the voltages show linear slopes. For the buck converter the waveforms for two different inductors are shown. The plot is made for two different inductance values for the buck inductors L_B with $L_a = 8 \cdot L_b$ and shows that the current through the inductor can also be negative for a positive output current.

4.5.3 Passives of the TSC

Similar to the PSFB converter the TSC can not step up. Therefore, the transformer turns ratio

$$n = k \frac{V_{OUT,max}}{V_{IN,min}} \quad (4.28)$$

has to be set in a way, that the maximum output voltage can also be reached for the minimum input voltage. In the same way as for the PSFB converter, the other components that influence k (ohmic and inductive voltage drops and limited duty cycle due to the dead time of the buck converter) are not known at this point and therefore it is assumed that $k = 1.02$ to 1.05 .

With the transformer designed, the stray inductance can be measured or calculated. The value for the resonant capacitors can then be calculated by solving equation 4.24 for $C_{r,p/s}$ at the resonant frequency $\omega_r = 2\pi f_{sw,iso}$, which results in

$$C_{r,p/s} = \frac{1}{\omega_r^2 L_{r,p/s}}. \quad (4.29)$$

The inductor for the buck converter is defined with a chosen ripple diL to

$$L_B = d_{LB} \frac{nV_{IN} - d_{LB} V_{IN}}{f_{sw,buck} \cdot \Delta I_{LB}}, \quad (4.30)$$

with $\Delta I_{LB} = diL \cdot I_{OUT,max}$ and $d_{LB} = P_{OUT,max}/I_{OUT,max}$, at the minimum output voltage for maximum output power.

Since the ripple current in L_B peaks at $d = 0.5$, $\Delta I_{LB,max} = \frac{nV_{IN}}{4f_{sw,buck} \cdot L_B}$ and the minimal output capacitance results in

$$C_{OUT,min} = \frac{\Delta I_{LB,max}}{8f_{sw,buck} \cdot \Delta V_{OUT,max}}, \quad (4.31)$$

with a maximum ripple voltage of $\Delta V_{OUT,max}$ at 50% of $V_{OUT,max}$. For the interleaved buck converter the minimum output capacitance can be reduced since the capacitor current is reduced [91]. Considering the maximum current ripple of the entire output range, the capacitor can be reduced by

$$C_{OUT,interl} \geq C_{OUT,min}/n_i \quad (4.32)$$

where n_i is the number of interleaved buck converters.

4.6 Conclusion

This chapter provides an introduction to isolated DC-DC converters and the benefits of modular interconnection of multiple converters. With a switchable secondary side configuration of two converters the operating range can be extended. Four different DC-DC converter topologies are selected and presented: PSFB converter, LLC converter, DAB and TSC. For each topology, the operating principle is introduced, the system variables are analyzed, and the passive components are dimensioned. This forms the basis for the automated design routines presented in the next chapter.

5 Design and optimization of DC-DC converters for a high-power charging system

In order to evaluate and compare the different topologies from chapter 4, and in the end find the most suitable topology for the high-power charging system, a metric must be found to crystallize out the optimal designs. For power electronic converters, such metrics can be efficiency, price (total or specific per watt/kilowatt), volume, weight, and power density.

This chapter presents an automated design and optimization process for high-power DC-DC converters. For this purpose, script-based design routines implemented in Matlab are created. The DC-DC converter design routines (one per topology) are responsible for designing the entire converter, while subroutines perform the design and loss calculation of active and passive components such as semiconductors, inductors, transformers, and capacitors. Another routine is used to design and optimize the required forced-air cooling systems. A multi-objective optimization is applied to find the most suitable topology and the best DC-DC converter design from the large number of solutions generated by the design routine. The following sections introduce and describe this design process and the subroutines in general. From section 5.5 on, the routine is used to design high-power DC-DC converters for a MCS system, where the optimal results are then identified and analyzed.

The Matlab scripts for the design routines were created during my time at Siemens, partly by myself, partly by my dear colleagues and partly in collaboration. A detailed breakdown of individual contributions can be found in the appendix in A.2.

5.1 Design routine for the semiconductors

To evaluate DC-DC converter designs, it is essential to determine the performance in terms of efficiency and cost. Since the active devices contribute significantly to both, the design routine for the semiconductors is fundamental. Three main semiconductor materials with different properties are currently used in power electronic systems: silicon (Si), silicon carbide (SiC), and gallium nitride (GaN). Three different types, including switches (MOSFETs or IGBTs) and diodes, are considered in the design routine. The most important criterion is the maximum junction temperature, which determines whether a device will operate well, have a reduced lifetime, or, in the worst case, be destroyed. The second important aspect, that has a significant impact on the overall design, is the cost of these semiconductor devices. The semiconductor design routine calculates the losses and maximum junction temperatures of the different active devices in the converter for a given combination of semiconductor and cooling system. This allows the valid designs to be identified and the efficiency to be calculated.

5.1.1 Design routine

Fig. 5.1 shows the flowchart of the semiconductor design routine. The inputs are the system variables and the models for the semiconductor and the cooling system. These inputs are used to calculate the conduction and switching losses of the semiconductors and the resulting junction temperature. The steps of the design routine are described in detail below.

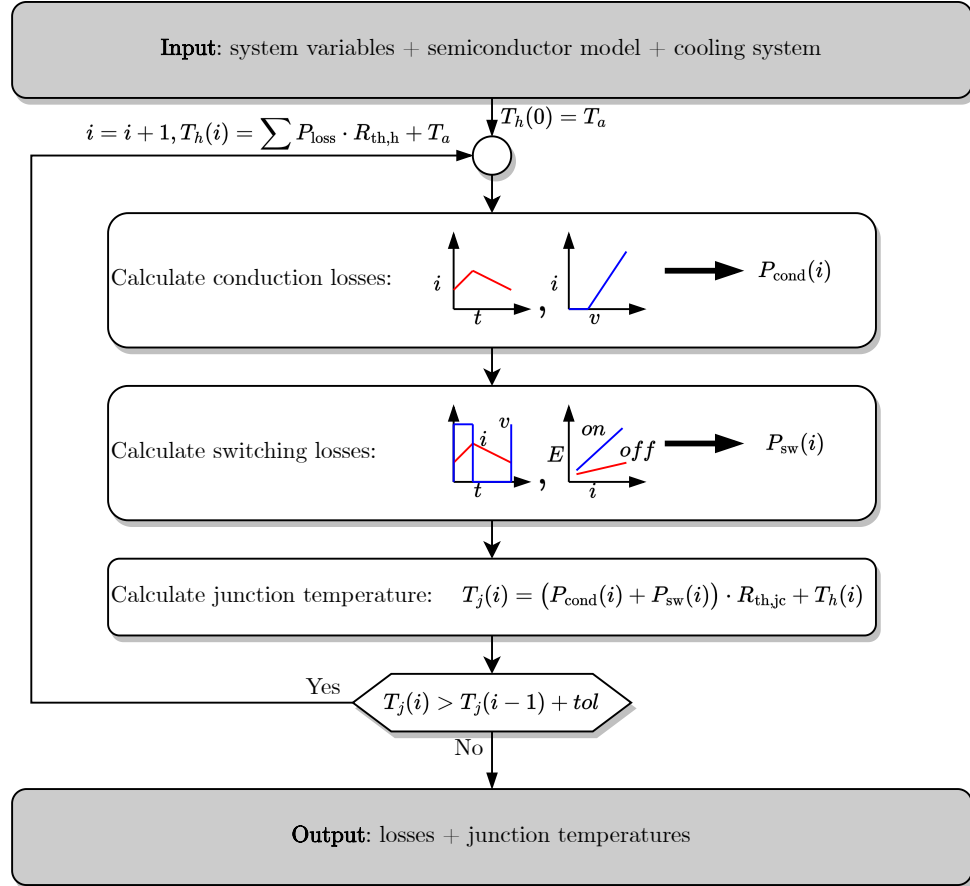


Figure 5.1 – Flowchart of the design routine for the semiconductors: with the given system variables and models for semiconductor and cooling system, the losses and resulting junction temperature are calculated

System variables

The system variables for the different topologies are calculated beforehand in a subfunction. These include the currents through and the voltages across the semiconductor devices needed for the loss calculation. The calculation of the system variables is performed according to chapter 4.

Semiconductor model

The semiconductors are assumed to be half-bridge power modules consisting of two semiconductor chips placed on an isolated baseplate. With these half bridges all the semiconductors for the four different DC-DC converter topologies can be represented. Loss models (described in detail below) are stored for the different semiconductor devices. The parameters for conduction and switching losses and thermal resistance are specified in these models.

More and more manufacturers provide precise loss models for their semiconductor devices (and modules) in the form of XML database files. These files can be used by the simulation tool PLECS to simulate accurately switching and conduction losses. The design routine for the semiconductors performs the loss calculation whenever the XML loss model file is available for the respective semiconductor device.

Losses and junction temperature

The semiconductor design routine is called up separately for each operating point. For each semiconductor device, the losses are repeatedly calculated at the temperature resulting from the previous step (starting temperature is the ambient temperature) until a steady state of the junction temperature is reached. Since temperature has a large effect on the losses, it is crucial to determine the dissipation as a function of junction temperature. The losses are divided into conduction losses and switching losses:

$$P_{\text{loss}}(T) = P_{\text{cond}}(T) + P_{\text{sw}}(T). \quad (5.1)$$

5.1.2 Conduction losses

Conduction losses occur when current flows through the device. There are ohmic losses (caused by the finite conductivity of the semiconductor material) and losses caused by the voltage drop across the pn junction (for diodes and IGBTs). The output characteristics of the devices can be approximated by a piecewise linear function. The characteristic functions for the different semiconductor devices are shown in fig. 5.2.

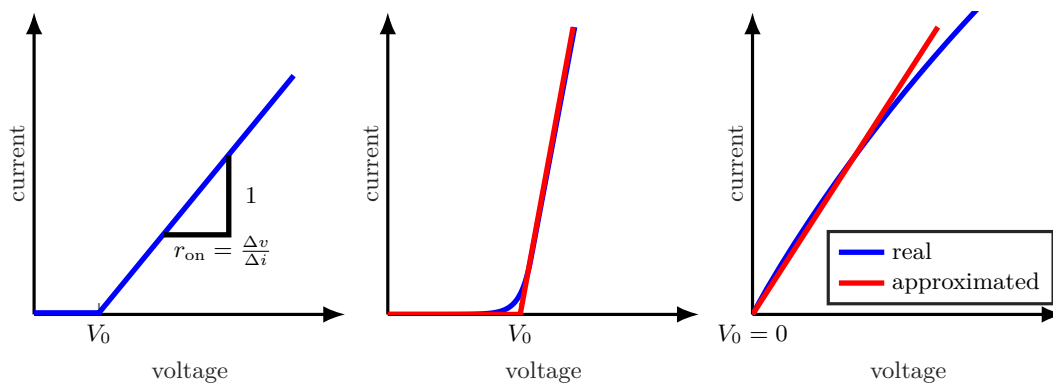


Figure 5.2 – Output characteristics for the semiconductors - left: general output characteristic function, center: approximated diode/IGBT, right: MOSFET

The general output characteristic is a straight line function with slope $1/r_{\text{on}}$ shifted by V_0 . For MOSFETs, $V_0 = 0$ [92], while for IGBTs and diodes, V_0 is typically in the low single-digit volt range. This approximation is only valid as long as the IGBT is operated in the saturation region and the MOSFET is operated in the ohmic region (see 5.2 on the right).

The conduction losses can then be calculated with

$$P_{\text{cond}}(T) = I_{\text{av}} \cdot V_0(T) + I_{\text{rms}}^2 \cdot r_{\text{on}}(T) \quad (5.2)$$

where I_{av} is the mean value and I_{rms} is the RMS value of the current through the device. The temperature dependence of V_0 and r_{on} should not be neglected. V_0 usually has a negative temperature coefficient for diodes and IGBTs, r_{on} a positive one for Si and SiC semiconductors. Most manufacturers specify these values at different temperatures, between which linear interpolation is acceptable. If the parameters are only given at one temperature, they can be linearly scaled to the desired temperature using empirical parameters, as described in [93].

The design routine considers two different cases when calculating the conduction losses. The first case is that only the data sheet values for V_0 and r_{on} are given. If these values are given only for one temperature, an extrapolation is performed using the empirical parameters. If the data is available for two or more different temperatures, linear interpolation is performed for the desired temperature. In the second case, an XML file containing the loss data for the semiconductor device is stored. A 2D lookup table with the voltage drop as a function of current and temperature is then available, and the voltage drop can be linearly interpolated in 2D.

Using the resulting voltage drop for each point on the current waveform, the conduction losses are calculated by multiplying it by the current. The average conduction losses over the switching period are then calculated by taking the mean value of the losses.

5.1.3 Switching losses

Switching losses are divided into turn-on and turn-off losses. Turn-on losses occur when the device changes from blocking state to conducting state, while the reverse state change results in turn-off losses. There are several ways to calculate switching losses. The most common way is to measure the energy loss during a reference switching operation, then scale it to the operating point being calculated and multiply it by the switching frequency:

$$P_{\text{sw}}(V, I, T) = f_s \cdot E_{\text{sw}}(T) \cdot \left(\frac{I}{I_{\text{ref}}} \right)^{K_I} \cdot \left(\frac{V}{V_{\text{ref}}} \right)^{K_V} \quad (5.3)$$

The exponents for the current and voltage dependence of the switching losses K_I and K_V are device dependent, table 5.1 shows these parameters determined in [94] for the different device types. The switching energy is also temperature dependent, so most manufacturers specify it for different temperatures. If only the switching energy for one certain temperature is specified, it is scaled with [95]

$$E_{\text{sw}}(T) = (E_{\text{ON}} + E_{\text{OFF}}) \cdot \left[1 + \frac{k_T}{1000} (T - T_{\text{ref}}) \right]. \quad (5.4)$$

The values for k_T are positive (switching energy and thus losses increase with increasing temperature). The parameters K_V , K_I , and k_T are listed in table 5.1.

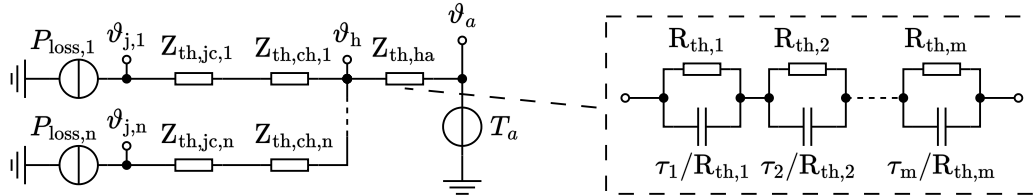
Parameter	MOSFET	IGBT	Diode
K_V	1	1.2...1,4	0,6
K_I	1	1	0,6
k_T	<1	3	5...6

Table 5.1 – Parameters for current, voltage and temperature scaling for switching losses [95]

In the design routine the turn-on and the turn-off losses are calculated separately (considering the respective device voltage and current during the switching event) and then summed. As for the conduction losses, the two cases of data sheet value and XML file are distinguished. In the case that only one value for the switching energy is available the scaling is done according to 5.3. In the XML file the switching energy is represented in a 3D-lookup table as a function of voltage, current and temperature. Further tables for energy scaling can be stored, for example scaling factors in dependency of the gate resistor. A linear interpolation between the given points in the XML file is performed for the respective operating point and temperature. The switching losses are then calculated by multiplying the resulting switching energy with the switching frequency. The sum of the turn-on and turn-off losses is then the total switching loss.

5.1.4 Junction temperature

If the thermal models of the semiconductor device and the cooling system are known, the junction temperature in the semiconductor can be calculated using the previously calculated losses (equation 5.1). Figure 5.3 (left) shows the thermal chain for the heat dissipation from the semiconductor to the environment.

**Figure 5.3** – Equivalent thermal circuit diagram of the loss path from source to sink according to Foster

The losses in the semiconductor are modeled as a current source, causing a temperature difference at the thermal impedances. $Z_{th,jc}$ describes the heat transfer from the semiconductor to the baseplate of the module, $Z_{th,ch}$ that from the baseplate to the heat sink, and $Z_{th,ha}$ that from the heat sink to the environment, which can be represented as a voltage (temperature) source. A thermal impedance consists of (as shown in fig. 5.3 on the right) multiple parallel resistor and capacitor combinations connected in series ($\tau = R_{th} \cdot C_{th}$). For a purely static view, the thermal capacitances can be neglected and the thermal resistances $R_{th1..n}$ can be combined into one resistance $R_{th,tot}$. The resulting junction temperature of the semiconductor can then be calculated via

$$\vartheta_{j,x} = P_{loss,x} \cdot R_{th,jh,x} + \vartheta_h, \quad (5.5)$$

with $R_{th,jh,x} = R_{th,jc,x} + R_{th,ch,x}$. The total losses are calculated and multiplied by the thermal resistance of the cooling system $R_{th,ha}$, in order to get the surface temperature

$$\vartheta_h = \sum_{i=1}^n P_{loss,i} \cdot R_{th,ha} + \vartheta_a \quad (5.6)$$

of the heatsink.

In computer-aided semiconductor temperature calculations, it is effective to iteratively calculate the temperature and power loss (as the losses are temperature-dependent), until the system reaches a steady state (difference between successive steps is sufficiently small). Experience has shown that this is usually the case after three to four iterations [94].

5.2 Design routines for the passive components

Passive components, together with semiconductors, are the key contributors to losses and cost in the system. The passive components considered for the converter design are inductors, transformers and capacitors (DC-link and resonant). While capacitors are typically available off-the-shelf for a wide range of applications, magnetic components are mostly custom designed and optimized for a specific application. Due to the large number of available core shapes, sizes and materials, as well as different possible winding configurations (cross-section, number of strands, insulation), it is difficult to find an optimal design for the inductors and transformers. One possibility is to perform a brute force calculation for all possible combinations and then find the best solution based on various criteria such as price, efficiency, weight or volume.

5.2.1 Magnetics design

The design process of the magnetics is done using a brute force approach. This requires multiple nested loops and can result in high computational requirements, depending on the input parameters. The magnetics must be designed for the worst-case operating point in order to ensure proper function over the entire operating range.

The figures 5.4 and 5.5 show the simplified flowcharts of the design processes for transformer and inductor. The two outer loops are similar for both components. The outermost loop iterates over the different cores given as input in the form of a table. In this table, parameters such as shape (EE, EI, UU, UI, PQ and all other possible core shapes), core material, effective cross-section A_e , effective magnetic path length l_e and manufacturer partnumber are given. Depending on the power rating of the overall system, a pre-selection of suitable cores should be made to reduce the computing power. The second loop iterates over the number of stacked cores within a given range. From this point on, the design routines for the two components differ.

For the transformer a table with different conductors (diameter, shape, insulation diameter) is iterated. Within this loop the maximum and minimum number of primary turns are calculated. In the innermost loop (iterating over the number of primary turns from $N_{p,min}$ to $N_{p,max}$ with an increment of one) the number of secondary turns is calculated over the required turns ratio and rounded to the nearest integer. The resulting ratio is then checked

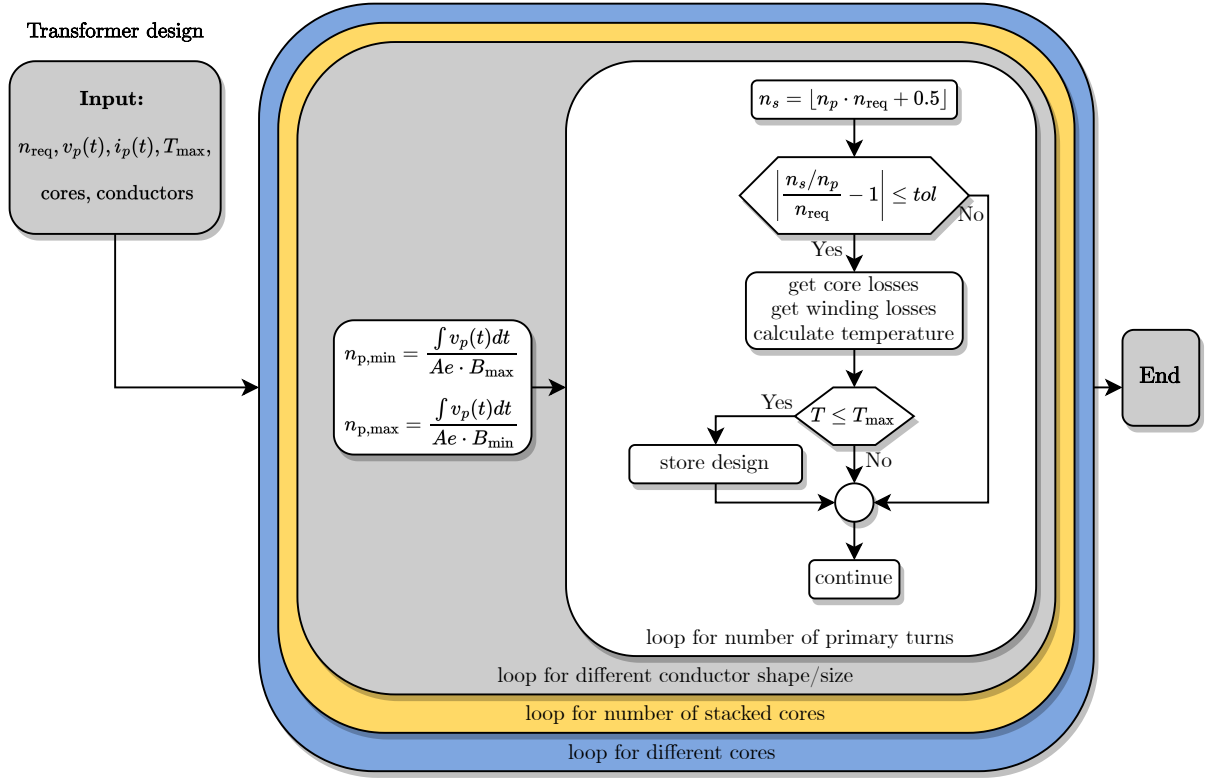


Figure 5.4 – Simplified flowchart of the transformer design routine with the nested loops for the brute force calculation of all possible combinations

to see if it is within the tolerance. If it is, the core and winding losses and the resulting temperature are calculated. If the temperature does not exceed the specified limit, the design is stored.

Since for the inductor different combinations of number of turns and airgap can result in the same inductance, all combinations must be calculated in the inductor design process. This is done in the third loop, where for each airgap (defined in the input) the required number of turns is determined by rounding the ideal number to the nearest integer. To do this, the inductance factor A_L has to be determined from the reluctance model as a function of the core parameters and the airgap. Then the core losses and temperature can be calculated and checked. The two innermost loops iterate over the different conductors (as for the transformer) and the number of strands. The upper limit is defined by the winding window for the respective core.

For the LLC converter the magnetizing inductance L_m is integrated into the transformer. Therefore, a third design process is implemented, which is basically the same as for the inductor, with the only difference that the winding window is divided into two windings and the turns ratio is checked if it is within the specified tolerance.

When all combinations are calculated, the best design can be selected either by lowest price or lowest losses or a combination of both.

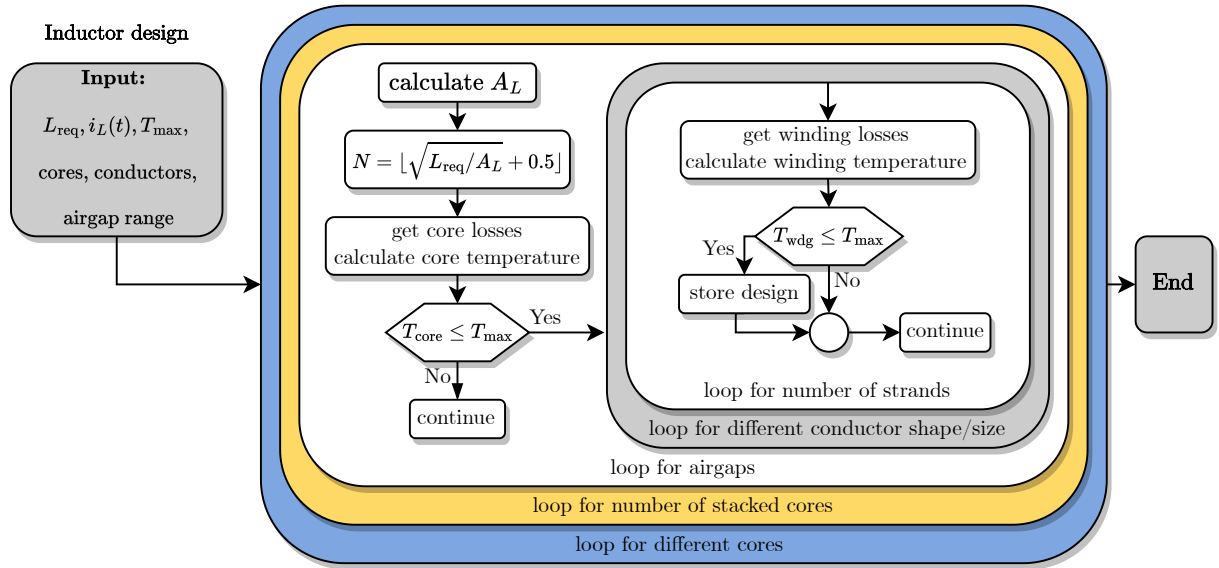


Figure 5.5 – Simplified flowchart of the inductor design routine with the nested loops for the brute force calculation of all possible combinations

5.2.2 Capacitor dimensioning

Two different types of capacitors are considered for the dimensioning of the capacitors: DC-link capacitors and resonant capacitors. For each type, a list of various capacitors from different manufacturers is created and stored.

DC-link capacitors

The first step is to load the stored table of DC-link capacitors. Three different types of capacitors, namely electrolytic, film and ceramic capacitors are considered. Then the following calculations are performed for each capacitor:

- calculate number of in series connected capacitors $n_{\text{ser}} = \lceil V_{\text{DC}}/V_{\text{Cap,max}} \rceil$
- calculate number of parallel connected capacitors $n_{\text{par}} = \lceil I_{\text{ripple}}/I_{\text{Cap,max}} \rceil$
- increase n_{par} until $C_{\text{tot}} \geq C_{\text{DC,min}}$

The total number of capacitors required for each type is then $n_{\text{tot}} = n_{\text{ser}} \cdot n_{\text{par}}$ and $C_{\text{tot}} = C_{\text{Cap}} \cdot n_{\text{par}}/n_{\text{ser}}$. The input values for the required DC-link capacitor are $C_{\text{DC,min}}$, V_{DC} , and I_{ripple} , and $V_{\text{Cap,max}}$, $I_{\text{Cap,max}}$, while C_{Cap} are the rated values for the individual capacitor. With n_{tot} the resulting cost, losses, volume and weight can be calculated and the optimal capacitor for each of these criteria can be selected.

Resonant capacitors

The calculation of the resonant capacitors is similar to that of the DC-link capacitors. However, in addition to meeting the current and voltage requirements, the capacitance must be matched

as accurately as possible. Since a pure AC voltage is applied to the resonant capacitors, electrolytic capacitors cannot be used. Therefore, only film capacitors and Class 1 ceramic capacitors are considered. In the dimensioning routine for the resonant capacitors, first the same design algorithm as for the DC-link capacitors is used. Then, in order to match the required capacitance, additional series or parallel capacitors are added until the resulting capacitance is within the desired tolerance band of the required value.

5.2.3 Loss calculation

This subsection describes the calculation of the losses in the different design routines for the passive components. Fig. 5.6 shows the equivalent circuit diagram of the passive components considered.

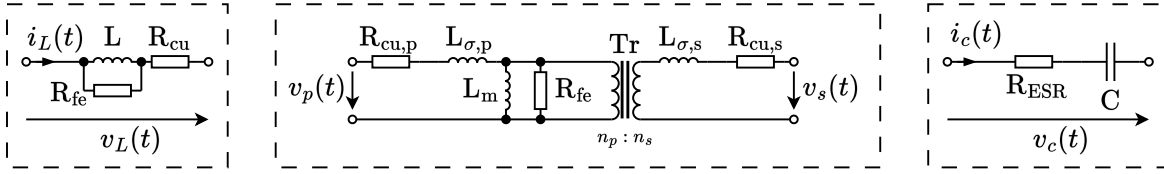


Figure 5.6 – Equivalent circuit diagram of the passive components including ohmic and inductive parasitics. From the left to the right: inductor, transformer and capacitor

Core losses

Core losses in a given ferrite material depend on the flux density over time $B(t)$ (magnitude, offset and frequency) and the temperature of the core. There is a nonlinear relationship between these parameters and the losses vary for different core materials. In the equivalent circuits the core losses are modeled as ohmic losses with R_{fe} . To estimate the core losses, the flux density $B(t)$ must first be calculated. For an inductor this can be done with

$$B(t) = \frac{L \cdot i_L(t)}{Ae \cdot N}, \quad (5.7)$$

where L is the inductance, $i_L(t)$ is the current through the inductor, Ae is the effective cross section of the core, and N is the number of turns.

$B(t)$ of the transformer can also be calculated with 5.7, by substituting $i_L(t)$ with $i_{Lm}(t)$. With the assumption that $L_\sigma = L_{\sigma,p} + L_{\sigma,s}/n^2 \ll L_m$, $i_{Lm}(t)$ can be calculated by integrating the voltage $v_p(t)$ over t and divide it through L_m :

$$B(t) = \frac{\int v_p(t) dt}{Ae \cdot n_p}. \quad (5.8)$$

A numerical approach is used in this work to calculate the core losses of the magnetics. Due to the nonlinear frequency dependence of the losses, a Fast Fourier Transformation (FFT) is performed for $B(t)$ for a defined number of harmonics i . The losses are then calculated by interpolating the loss density of each harmonic in a given 3D-lookup table for the respective

core material (parameters are flux density, frequency, and temperature), summing, and multiplying by the core volume.

$$P_{\text{fe}} = V_{\text{core}} \cdot \sum_i LUT_{\text{ld}}[B(f(i)), f(i), T] \quad (5.9)$$

If $B(t)$ is offset free, then the total core loss density is the sum of the loss densities of each harmonic. If $B(t)$ also has an offset, this sum needs to be scaled by an additional factor, called displacement factor DPF [96]. To calculate the core losses the resulting loss density is multiplied by the core volume.

Winding losses

Winding losses in inductors and transformers are ohmic losses in the conductor, caused by the current flowing through it. The losses are highly influenced by the frequency of the current through the conductor, other conductors in the winding window and external magnetic fields. The winding losses can be modeled as

$$P_{\text{cu}} = R_{\text{DC}} \cdot I^2 \cdot X, \quad (5.10)$$

with R_{DC} being the DC resistance of the conductor material, I the RMS value of the current through the conductor and X a function depicting the AC losses. For the design algorithm equations from [97] have been implemented. For the AC losses skin effect as well as proximity (internal and external) effect have been considered. For simplicity only round (solid and litz) wires are considered. Depending on the number of layers and turns and whether there is an air gap or not, the respective equation set is used. As with core losses the different frequency components of the current are calculated individually and summed. Since the winding losses are also temperature dependent, the losses have to be calculated with the specific conductivity at the resulting temperature.

Thermal model

To calculate the resulting temperature of core and winding, a thermal model is set up. An equivalent circuit diagram with losses as current sources, thermal resistances as resistors and temperatures as voltages has to be parameterized (similar to the temperature calculation for the semiconductors in fig. 5.3). According to [97], the three heat transfer mechanisms conduction, convection and radiation have been considered to sink the losses from the magnetic component to the ambient air.

Capacitor losses

The capacitor losses can be calculated with

$$P_C = R_{\text{ESR}} \cdot I_C^2, \quad (5.11)$$

where I_C is the RMS value of $i_C(t)$. For a higher accuracy the capacitor losses can be calculated for every harmonic of the capacitor current. Since in this work the design algorithm

is run with a large number of different capacitors from different manufacturers, the data of the frequency dependent R_{ESR} is not available for all types and therefore only the simplified equation 5.11 is used. The temperature of the capacitors is not calculated and it is assumed that the maximum temperature is not exceeded when operating the device within the specified limits.

5.2.4 Design routine for the cooling system

A design routine is implemented to compute a large number of different cooling system designs within a range of specified geometries and to identify the optimal designs for different thermal resistances $R_{\text{th,ha}}$. Figure 5.7 shows the flowchart of the design routine for the cooling system. Forced-air convection in combination with extruded aluminum heatsinks is assumed. To design such a system, two problems have to be solved. First, the thermal resistance of the designed aluminum heatsink as function of the air volume flow rate and the geometry $R_{\text{th,ha}}(\dot{V}, \text{geom})$ must be found. Then the pressure drop of the heatsink, also in dependency of the volume flow rate is calculated. With a given fan curve (pressure drop in dependency of the volume flow) the resulting operating point can be found. The equations presented and verified in [98] are used to implement a subfunction that calculates the resulting thermal resistance $R_{\text{th,ha}}$ for a given combination of heatsink design and fan.

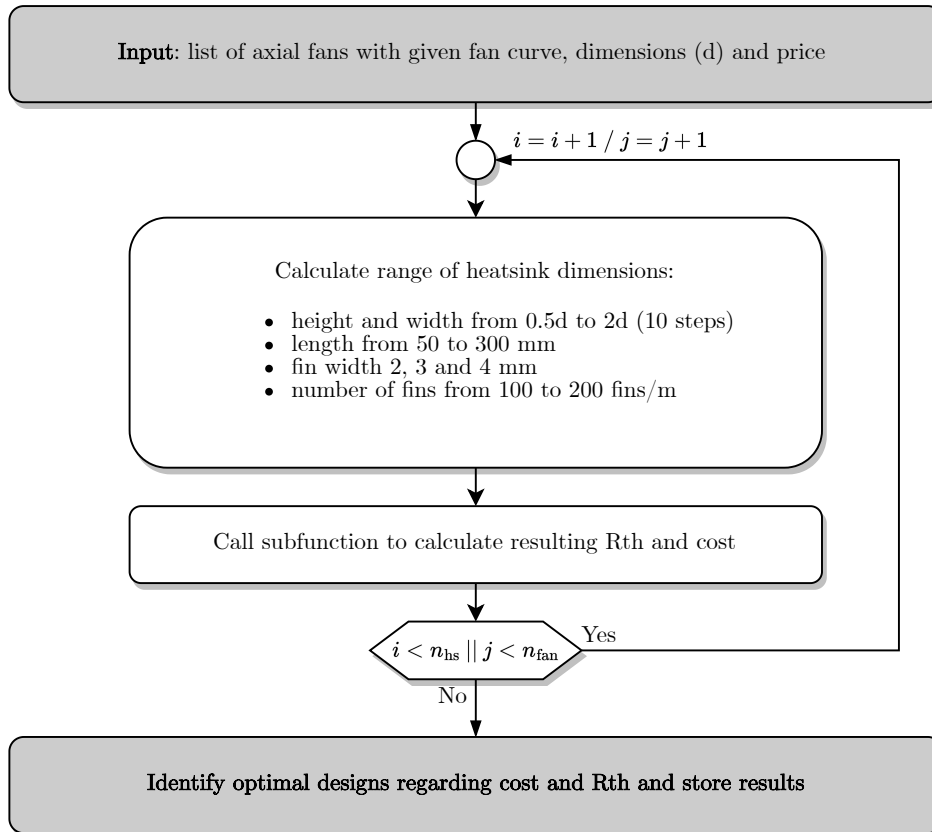


Figure 5.7 – Flowchart of the design routine for the cooling system

The cooling system design routine uses this subfunction to calculate the resulting thermal resistance for all possible combinations from a given set of fans and various heatsink geometries. The cost of the cooling system is then calculated from the cost of the fan and the amount of aluminum required. From all the calculated cooling system designs, the optimal designs must be identified. This is done with a two-dimensional optimization of the two parameters $R_{th,ha}$ and cost (lower is better). Only the optimal designs are stored and used later in the design routine for the DC-DC converters described below.

5.3 Cost modeling

Accurately modeling the cost of each component of the DC-DC converter is crucial for an effective optimization. This section provides a detailed overview of the cost modeling approach employed in this work. The costs used here for the standard components refer to a quantity of 10 000 pieces per year. A major component that is not considered in the total cost is the mechanical housing, which is highly dependent on the materials used and the overall design. However, this is assumed to be the same for each of the designs of the different DC-DC converter topologies, so the relative cost comparison is valid.

Semiconductors

The cost of the semiconductors is requested from the various module and chip manufacturers for the mentioned number of units per year. The prices obtained in this way are stored in the semiconductor models. However, the exact pricing information is subject to confidentiality agreements between the manufacturers and Siemens, and therefore, cannot be disclosed in this work. Due to these confidentiality constraints, only relative costs, rather than precise price points, are presented and discussed here.

Magnetics

The cost of the magnetics (transformers and inductors) can be divided into two main components: core cost and winding cost. The cost of the various cores available, which vary in shape and material, was obtained from the manufacturers and entered into the database. Unknown prices were scaled by weight or volume. The total cost for the cores in a design is the core price multiplied by the number of cores used. The material cost of the winding is calculated from the cost of a single strand. These are stored for different strand diameters and then linearly scaled for the number and length required in the design. The total cost of a design is then the sum of the two components. Any additional costs for bobbins, extra wire insulation or potting material are not taken into account here.

Capacitors

Since the DC-link and resonant capacitors are standard components, the required prices are stored in the database. In the dimensioning routine, these are then multiplied by the number of capacitors required.

Cooling system

The total cost of the forced-air cooling system is the sum of the fan and heatsink costs . While the fans are again standard components, the prices for the aluminum heatsinks are scaled by the weight of the particular design. Manufacturing costs are not considered.

Auxiliary circuits

The additional cost of the auxiliary circuitry is very important to the total cost of the system. The auxiliary circuitry includes:

- isolated gate driver circuit including supply
- DSP and control unit
- analog measurement circuitry for voltages, currents and temperatures
- auxiliary voltage supply

These costs are assumed to be topology independent. The cost of the driver is scaled by the number of switches used. Table 5.2 shows the assumed cost of the auxiliary circuits.

Table 5.2 – Additional costs considered

Component	cost
gate driver	2.5 €/switch
DSP and control	25 €
measurement circuitry	20 €
auxiliary voltage supply	10 €

5.4 Design and optimization

This section describes the main design routine for the DC-DC converters. First, the valid DC-DC converter designs from all possible combinations of design variables, semiconductors, and cooling systems are calculated for each topology and stored if valid. In the second step, this large number of designs is compared and the most suitable designs are found using multi-objective optimization. This method is already a well-known optimization tool for power electronic converters [99]. While the design routine in this work uses a similar concept to [99], the design process is more focused on real components such as semiconductors (with the option to use the loss models from the manufacturers), capacitors, and ferrite cores. The optimization is then performed for the two dimensions of cost and efficiency, considering multiple topologies and configurations.

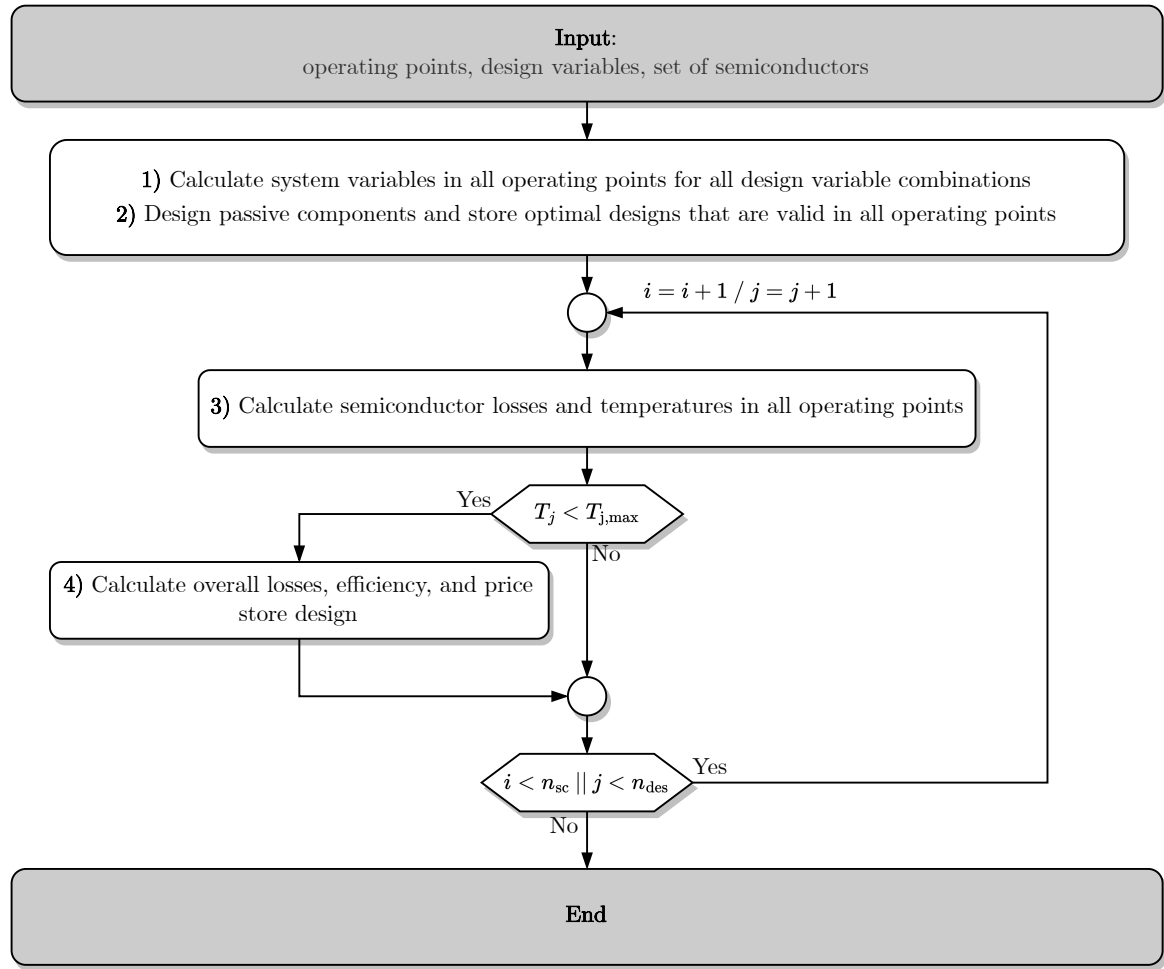


Figure 5.8 – Simplified flowchart of the design process for the different DC-DC converter topologies

5.4.1 Design routine for the DC-DC converters

Fig. 5.8 shows the flowchart of the design process for the DC-DC converters. The input variables are the different operating points, the design variables, and the set of semiconductors. An individual design routine is implemented for each of the four topologies, following the design process of fig. 5.8. The most critical criterion in determining whether a design is valid or not is the temperature of the individual components. Too high temperatures can lead to destruction or shortened life. Two main physical quantities define the resulting temperature in the components: The losses and the thermal chain from the hot spot to the cooling medium.

Design variables for the different topologies

The design variables affect the waveforms of the component currents and voltages. Therefore, the system variables must be calculated for all combinations of the design variables. These design variables differ for the four topologies:

For the PSFB converter, the first design variable is the switching frequency f_{sw} . It affects the core size of transformer and inductor, the switching losses in the semiconductors, and the size of the capacitors. The second design variable for the design routine is the allowable current ripple in the output inductor diL , which together with the switching frequency defines the inductance and thus the design of the inductor and the output capacitor.

The first design variable for the LLC converter is the resonant frequency f_r . Higher frequencies result in smaller inductor and transformer core sizes, but since the switching frequency for the LLC converter is variable, the passives are designed at the most critical operating point, which is not necessarily operating at the resonant frequency. The second design variable is the resonant capacitance C_r . The overall behavior of the LLC is determined by its resonant tank and a higher C_r results in a smaller L_r and vice versa. Since the LLC converter can step down and step up its output voltage, the transformer turns ratio n is also considered as a design variable and is swept in the design process.

For the DAB the design variables are the switching frequency f_{sw} and the inductance L_r . While the switching frequency is provided as a list of different values, for the inductance an optimal value must be found for each switching frequency as described in 4.4. To ensure that a global optimum is found, different values around the optimal value of L_r are swept.

For the TSC, the two stages are considered independent and are therefore calculated separately. For the isolation stage, the only design variable is the switching frequency f_{sw} , which, as for the other topologies, defines the size of the transformer and influences the losses of the semiconductors. For the buck converter, the design variables are the switching frequency f_{sw} and the allowed current ripple in the output inductor diL .

The summarized design variables for the different topologies are shown in table 5.3.

Table 5.3 – Design variables for the different topologies

PSFB	LLC	DAB	TSC
f_{sw} diL	f_r C_r n	f_{sw} L_r	$f_{sw,iso}$ $f_{sw,buck}$ diL

1) Calculation of the system variables

For each combination of the design variables the system variables (voltage and current waveforms for each component) are calculated. The calculation is done for each of the given operating points (V_{IN} , V_{OUT} , and P_{OUT}) according to the equations presented in chapter 4.

2) Design of the passive components

With the calculated system variables the values of the passives can be calculated according to chapter 4. The most critical operating point for the passives must be found in order to design the passives. Most often this critical operating point is at full power and maximum output current. Using the system variables and the passive component values, the different design routines from 5.2 are used to create the designs of the passives. The losses and resulting

temperatures in the passives are calculated for each operating point. If the transformer or inductor design fails at any point, for example, because the worst-case operating point is not at full power and maximum output current, the design process is repeated for that operating point. For the inductor, it is also possible to connect two or more identical inductors in series. If the design fails, the design process is repeated by dividing the inductance value by the increased number of inductors in series (the losses are then multiplied by this number). If no design is found by the time a termination criterion is reached, that combination of design variables is marked as invalid and excluded from further calculations. The valid combinations, including the component designs, are stored in a buffer.

3) Calculation of the semiconductor losses

The semiconductor losses are calculated using the semiconductor design routine from 5.1. Three parameters are considered: system variables, semiconductor model, and cooling system. The semiconductor models used in the converter stages primary side, secondary side, and in the case of the TSC the buck converter are provided. For the cooling system, a stored set of optimal designs created with the routine in 5.2 is used for the calculations. For all combinations of semiconductors used for the different stages, the losses for each cooling system from the given set are calculated. This is done for each of the previously determined designs with valid passives in all operating points. If the maximum junction temperature is not exceeded in any operating point, the design is valid.

4) Saving the valid designs

If the design is valid in the previous steps, further calculations are performed. These are: calculation of the total losses by summing the losses of each component, calculation of the efficiency for each operating point, and calculation of the total material cost of the system.

Depending on the input parameters, the number of valid designs can be huge. For a comprehensive comparison of different topologies, as done in this work, thousands or even tens of thousands of resulting designs are determined. Therefore, it may be useful to store only the calculated final results such as losses, efficiency, and cost, and drop the intermediate results such as system variables and the cached data from the design of the passives.

5.4.2 Evaluation of the designs

The second step of the multi-objective optimization is the evaluation of the computed designs. In this work the optimization is performed over the two variables cost and efficiency. For the cost comparison the specific cost (in €/kW) is used. The efficiency is averaged over all operating points at full output power, partial load is not considered for optimization, although it can be implemented for other use cases. This allows the identification of Pareto optimal designs by computing the Pareto front and selecting the most favorable options. A Pareto front describes the set of non-dominated solutions within a solution space. This means that there is no other solution that improves one objective (cost or efficiency) without simultaneously worsening the other.

5.5 DC-DC Converter design for MCS

In this section, the previously presented DC-DC converter design routine is used to compare the four topologies PSFB, LLC, DAB and TSC for the case of a MCS fast charging application ($V_{EV} = 500\text{ V}$ to 1250 V) in the charging park with the 1500 V DC distribution grid. For this purpose, the design routines for the different topologies are called up individually and the results are then compared and evaluated. With a multi-objective optimization the best designs in terms of cost and efficiency are found and the most suitable design for this particular application is chosen.

The conditions for the design routines of the different topologies need to be as similar as possible to ensure a fair comparison. The parameters and conditions used for the design process are presented below.

5.5.1 System configuration

The voltage of the DC distribution grid is chosen to $V_{DC} = 1500\text{ V}$ (see section 3.3). For a cost efficient overall system the DC-DC converters should follow a modular approach, i.e. scalable power to cover the MCS and NCS applications. Therefore the power level of one system needs to be between 100 and 150 kW . Multiple systems are then connected in parallel to reach the MCS power level. For the given DC bus voltage V_{DC} and EV voltage range V_{EV} and the selected semiconductor blocking voltages, four interconnection variants are selected (switchable or series-connected variants with 2000 V semiconductors do not make sense). These four configurations are shown in fig. 5.9.

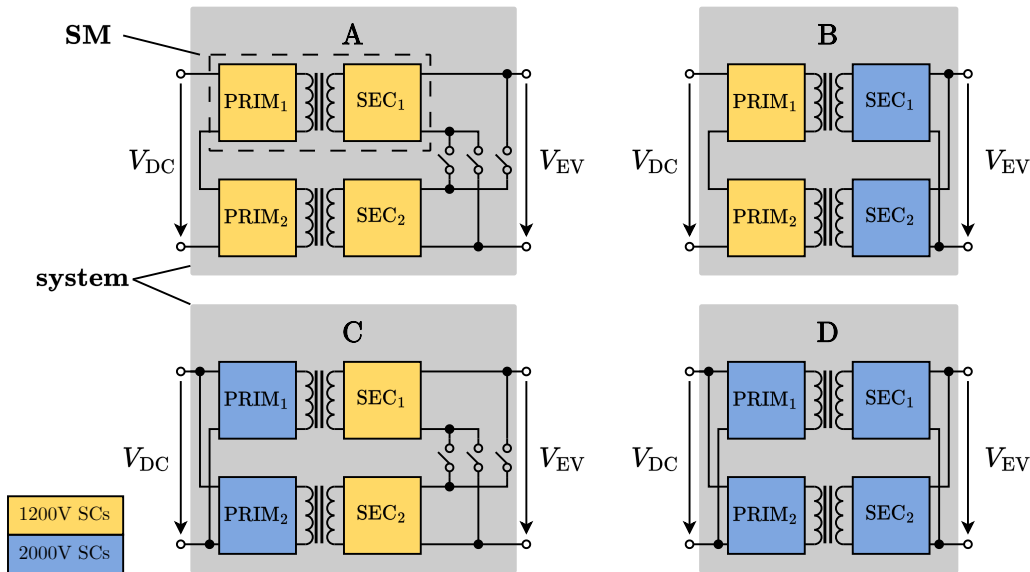


Figure 5.9 – The four different system configurations, each consisting of two interconnected submodules SM, used to compute the designs: **A**: primary side series connection and switchable secondary side configuration with 1200 V semiconductors, **B**: primary side series and secondary side parallel connection with 1200 V / 2000 V semiconductors, **C**: primary side parallel connection and switchable secondary side configuration with 2000 V / 1200 V semiconductors and **D**: parallel/parallel connection with 2000 V semiconductors

The design routine considers only the DC-DC converter submodule (SM), not the system configuration. Therefore, the input and output voltage and power are set per submodule for each configuration. The power values for the submodules are chosen to be as high as possible for each topology and configuration, but low enough to ensure a large number of valid designs. This is done by systematically running the design routine with increasing output power (with a reduced set of design variables to save calculation time), until only a small number of valid results is obtained. Tab. 5.4 shows the parameters for the four topologies in the different configurations.

Table 5.4 – Input and output voltage and maximum power for one submodule for the different topologies and configurations. The system power is twice the power of one submodule (multiple systems can then be connected in parallel for higher power, such as MCS).

Config.	$V_{IN,SM}$	$V_{OUT,SM}$	$P_{SM,PSFB}$	$P_{SM,LLC}$	$P_{SM,DAB}$	$P_{SM,TSC}$
A	750 V	375 V to 750 V	50 kW	50 kW	50 kW	75 kW
B	750 V	500 V to 1250 V	45 kW	40 kW	-	-
C	1500 V	375 V to 750 V	50 kW	50 kW	50 kW	75 kW
D	1500 V	500 V to 1250 V	45 kW	35 kW	-	60 kW

Some combinations do not make sense, for the DAB the switchable secondary side configuration is required for a good utilization of the semiconductors. The power level for the configurations **B** and **D** would be very low, since maximum power needs to be achieved for the entire output voltage range. For the TSC configuration **B** is not investigated further, because the isolation stage with the given semiconductors would have a power capability of more than 100 kW. Due to the input voltage, two submodules are required and the resulting power level would be too high for one system. In addition, the system would require at least four interleaved buck converters per submodule to handle the high resulting current at lower EV voltages. Two interleaved buck converters are used for the TSC in configuration **A** and **C** (as shown in 4.18) and three in configuration **D**.

For the evaluation, the total converter efficiency is calculated as the average efficiency for three different equidistant output voltages of the range and maximum output power. For the configurations **A** and **C**, the efficiency is calculated for the output voltages 375 V, 562.5 V, and 750 V, while for the configurations **B** and **D** the voltages 875 V, 1250 V, and 750 V are considered.

5.5.2 Semiconductors

The comparison between the different topologies and system configurations should be done as fair as possible. Two different semiconductor switches are considered, a 1200 V, 4 mΩ and a 2000 V, 12 mΩ SiC MOSFET. IGBTs and other types of semiconductors are not taken into account. The selected switches are FF4MR12W2M1H and IMYH200R012M1H from Infineon. The switching power of the two transistors should be about the same and is, according to the data sheet,

$$P_{T,1200V} = V_{DSS} \cdot I_{D,cont} = 240 \text{ kW and } P_{T,2000V} = 246 \text{ kW.} \quad (5.12)$$

FF4MR12W2M1H is a half-bridge module, while IMYH200R012M1H is a discrete device (at the time of this work, no 2000 V, 12 mΩ modules were available). Therefore, the isolation

from the chip to the heatsink must also be taken into account. The thermal resistance from the isolation, $R_{th,ch}$, is therefore chosen and $R_{th,jh} = R_{th,jc} + R_{th,ch} = 0.192 \text{ K/W}$ for both devices. For the calculations, these switches are also used for the active rectification, so there is no need to use any diodes. These existing semiconductor switches have been chosen to calculate losses as realistically as possible, but can also be scaled in performance if needed. The same approach is applied to the cost: to eliminate pricing influenced by non-technical factors, it is assumed that the cost of both devices is the same.

5.5.3 Passive components

The parameters that determine the dimensioning of the passive components in the DC-DC converter have a major influence on the overall design. The most important point is to choose the parameters in such a way that the design routines generate as large a set of valid solutions as possible, so that a global optimum can be found in the subsequent selection of the optimal design. Another important point is the limitation of the design space in order to avoid unnecessarily long computing times. This can also be done iteratively by reducing the set of input parameters by the values that do not lead to a valid design.

Magnetics

For magnetics, there are three parameters that can be used to optimize computation time. The first is to limit the number of different cores and core materials. This reduces the number of runs of the magnetics design routines shown in fig. 5.4 and 5.5. For example, cores that are too small (the upper end of available core sizes is required for the high power levels being considered) or cores that cannot be stacked can be eliminated from the design process. Also the number of solutions can be reduced by reducing the number of different materials under consideration, only the materials N87 and N97 from TDK are considered. The second parameter is the set of air gaps used in the calculation of the inductors and the LLC converter transformer. By limiting the set to a reasonable range for these applications, the number of iterations can be reduced, saving computation time. The third parameter to reduce the number of calculation combinations is to restrict the conductor materials and geometries used. Here, only strands of round copper conductors with a diameter of 0.071 mm are used. For the frequencies considered, this should be a good compromise between cost and performance, since simulations show that larger diameters have higher losses and smaller diameters have disproportionately higher relative costs.

Capacitors

For the dimensioning routines for the capacitors, two important points have emerged in relation to the stored capacitor database. The first point is to use of as many different capacitor types (voltage and current ratings) as possible. The way the DC-link capacitor design routine is implemented, a solution is found for all input parameters (even with only one capacitor type in the database a solution would be found, as the calculation would simply increase the number of devices connected in parallel and in series). An optimal solution in terms of cost or volume in general can only be found by considering the appropriate capacitors for the individual application. For both design routines (DC-link and resonant

capacitors), a wide range of voltage, current, and capacitance values, varied by different capacitors, contributes greatly to finding an optimal solution. The second point again involves reducing the computing time. This is much less critical when dimensioning capacitors than with magnetics because the calculation is vectorial, which avoids inefficient loops. Nevertheless, it makes sense to limit the number of capacitors in the database, since capacitors that do not represent an optimal solution in terms of cost or efficiency for any voltage, current or capacitance value only create unnecessary computational overhead.

Cooling system

The cooling system design routine is used to find and store optimal solutions for different cooling performances. As a result, more than 300 optimal solutions for cooling systems with $R_{th,ha}$ of 0.02 K/W to 1.1 K/W have been found. In the design routine for the semiconductors, one heatsink is assumed for the primary side, one for the secondary side, and in the case of the TSC, one for the buck converter. Five cooling systems are selected from those over 300 solutions as a compromise between large solution space and computation time. The cooling performance (thermal resistance to the ambient) of these different cooling systems is shown in table 5.5.

Relays for parallel/series configuration

For a fair cost comparison between the configurations, the cost of the relays for switching between parallel and series connection must be taken into account. These relays are only required for configurations **A** and **C**. A comparison of available standard 1000 Vdc, 150 A to 200 A relays shows an about 10 % higher cost for 200 A compared to 150 A relays. Therefore, the cost is assumed to be 50 € per relay, for a total of 150 € for a power level of up to 56 kW, and 55/165 € for a power level of up to 75 kW. The losses occurring in the relays are neglected in the calculations.

5.5.4 Parameters, maximum values, and design variables

This subsection provides an overview of the parameters, maximum values, and design variables used in the design routines for the different topology DC-DC converters. It details the key inputs that influence the design process, including maximum values that define the scope of valid solutions. In addition to the common parameters shared across all topologies, specific parameters are employed for each topology.

Table 5.5 provides a summary of the common parameters and maximum values used in the design processes of the four different topologies.

Table 5.5 – Parameters and maximum values used for the the design processes of all four topologies

Parameter	Symbol	Value
Maximum ambient temperature	T_a	50 °C
Maximum junction temperature	$T_{j,max}$	125 °C
Maximum winding temperature	$T_{wdg,max}$	120 °C
Maximum core temperature	$T_{core,max}$	100 °C
Maximum output voltage ripple	$\Delta V_{OUT,max}$	2 V
Cooling systems	$R_{th,ha}$	{0.03, 0.45, 0.09, 0.1, 0.17} K/W

Topology specific

The topology-specific parameters described below are preselected manually by eliminating input parameters that do not lead to a valid design to reduce the calculation time. For this purpose the design routine for the passive components is used to identify non-valid inputs.

The design variables specific to the PSFB (Phase-Shifted Full-Bridge) converter are presented in table 5.6. The transformer turns ratio is calculated in the design process and is therefore not considered as a design variable. The design variables for the PSFB converter do not differ between the four different system configurations.

Table 5.6 – Design variables used for the PSFB converter

Parameter	Symbol	Config. A-D
Switching frequency	f_{sw}	{20, 25, ..., 70} kHz
Maximum inductor current ripple	diL	{10, 20, ..., 100} %
Inductor cores	-	{E70, E80, E100}
Stacked inductor cores	$N_{L,st}$	{1, 2, ..., 5}
Transformer cores	-	{E100, U93}
Stacked transformer cores	$N_{Tr,st}$	{1, 2, ..., 6}

Table 5.7 outlines the design variables utilized for the LLC converter. The set of different transformer turns ratios as well as the range of the resonant capacitor is different for each system configuration, since the total computation time for the design process would be extraordinarily high if the full set of combinations had to be calculated for each configuration.

Table 5.7 – Design variables used for the LLC converter

Parameter	Sym.	Config. A	Config. B	Config. C	Config. D
Sw. freq.	f_{sw}	{20, 25, ..., 40} kHz			
Tr. wdg. ratio	n	{0.7, 0.75, 0.8}	{1, 1.05, 1.1}	{0.3, 0.4, 0.5}	{0.5, 0.6, 0.7}
Reson. cap.	C_r	[50, 400] nF	[50, 200] nF	[10, 120] nF	
Ind. cores	-	{E80, E100, U93}			
St. ind. cores	$N_{\text{L,st}}$	{1, 2, ..., 8}			
Tr. cores	-	{E100, U93}			
St. tr. cores	$N_{\text{Tr,st}}$	{1, 2, ..., 8}			

The design variables applied to the DAB are detailed in table 5.8. The same set of design variables are applied for configurations **A** and **C**

Table 5.8 – Design variables used for the DAB

Parameter	Symbol	Config. A and C
Switching frequency	f_{sw}	{20, 25, ..., 50} kHz
Inductor	L_r	[5, 20] μ H
Inductor cores	-	{E80, E100}
Stacked inductor cores	$N_{L,st}$	{1, 2, ..., 5}
Transformer cores	-	{E100, U93}
Stacked transformer cores	$N_{Tr,st}$	{1, 2, ..., 8}

Table 5.9 lists the specific design variables utilized for the TSC. The values for both stages in the three system configurations used are provided.

Table 5.9 – Design variables used for the TSC

Parameter	Symbol	Config. A, C and D
Switching frequency isolation stage	$f_{sw,iso}$	{70, 90, ..., 130} kHz
Switching frequency buck converter	$f_{sw,buck}$	{30, 35, ..., 60} kHz
Maximum inductor current ripple	diL	{60, 70, ..., 100} %
Inductor cores	-	{E70, E80, E100}
Stacked inductor cores	$N_{L,st}$	{1, 2, ..., 5}
Transformer cores	-	{E100, U93}
Stacked transformer cores	$N_{Tr,st}$	{1, 2, ..., 8}

5.6 Design results and multi-objective optimization

The previously presented design routines for the different topologies are employed to systematically calculate all feasible designs of each topology, ensuring that a wide range of potential solutions is explored. In this section, the design results are presented and analyzed to understand the strengths and weaknesses of the designs. To identify the most advantageous designs, a Pareto front is constructed, which highlights the optimal trade-offs between performance and cost. This approach allows for a clear visualization of the balance between these two critical factors, enabling the selection of designs that offer the best overall value. Through this process, the most efficient and cost-effective solutions are identified, providing valuable insights for the final decision to select the best design.

5.6.1 Comparison of all topologies

The DC-DC converter designs obtained by executing the design routines are saved for the different topologies and configurations. The resulting number of valid designs depends on the topology as well as the configuration. The lowest number of designs is obtained by the DAB and PSFB and LLC converters in configurations **B** and **D** with just over 1000 designs

each. While the PSFB and LLC converters in configurations **A** and **C** reach a number of well over 2000 different valid designs, the TSC exceeds this number by a factor of about five. This is due to the higher number of possible combinations of the cooling system due to the additional stage. For the comparison, the number of TSC results is reduced by eliminating the indistinguishable designs that are very close to each other. In order to compare this set of solutions, the first step is to display them graphically in two dimensions. This representation is shown in fig. 5.10. Each point represents a valid design and is plotted between specific costs on the x-axis and efficiency on the y-axis. The efficiency is the average value of the calculated efficiencies at full output power for different output voltages $V_{OUT,SM}$ of the range displayed in tab. 5.4.

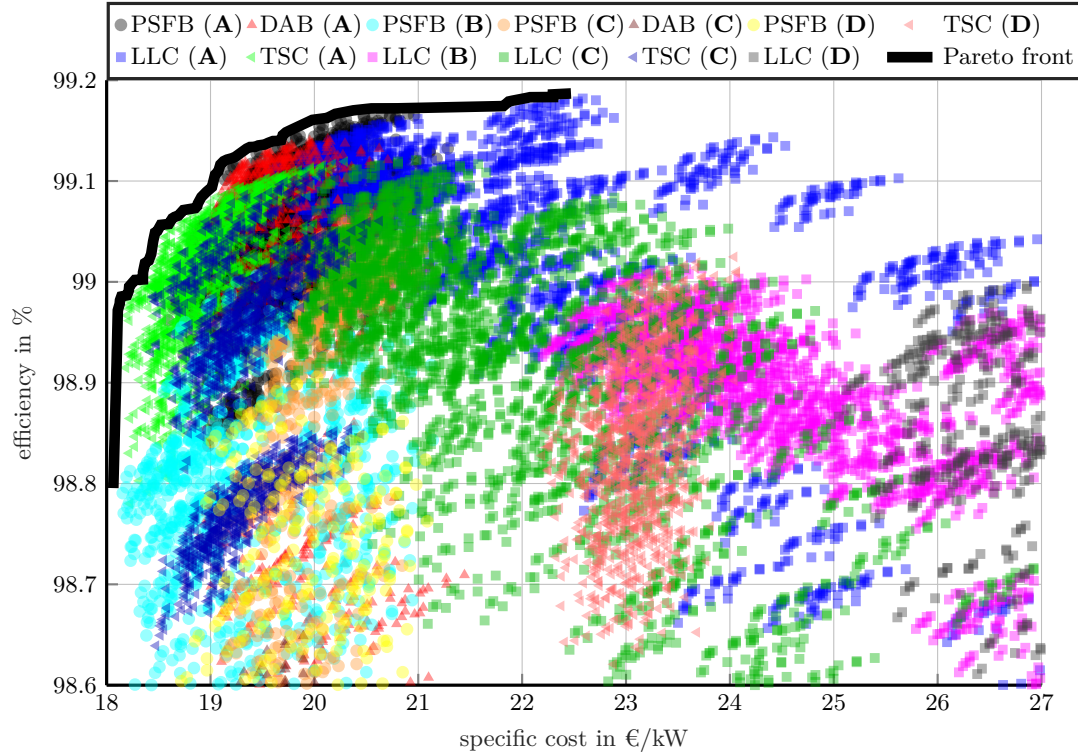


Figure 5.10 – Efficiency versus specific cost for all DC-DC converter designs across all topologies and configurations. The global Pareto front, representing the optimal designs among all four configurations, is highlighted. To maintain clarity, designs that fall outside the displayed limits have been excluded, as they do not represent optimal results.

The Pareto fronts for all designs in the different configurations are shown in fig. 5.11. It can be seen that the optimal designs of configuration **A** have a higher efficiency and a lower specific cost compared to the other configuration. The designs of configuration **D** show the lowest performance and the highest cost. In particular, the designs of the LLC converter in configuration **D** do not represent optimal designs across the three topologies compared in this configuration. This is due to the fact, that a lower maximum output power can be achieved compared to the other topologies in this configuration. Therefore, the specific cost is higher since the constant cost factors such as semiconductors and auxiliary circuits do not change.

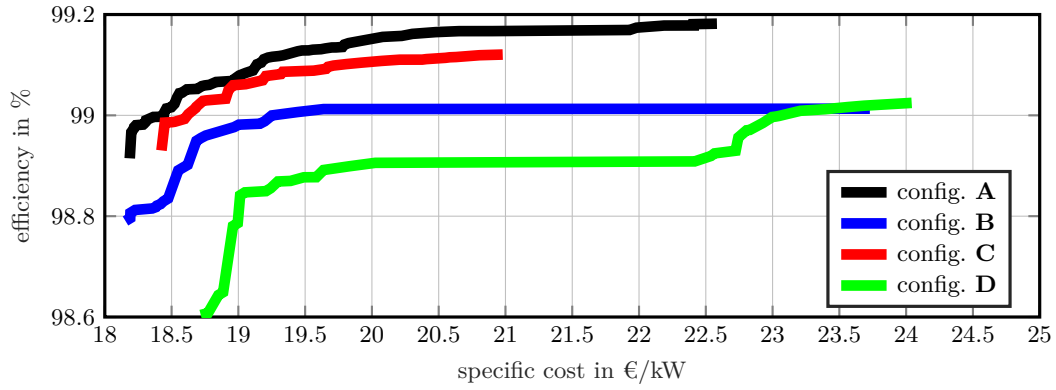


Figure 5.11 – Pareto fronts of the optimal designs within a configuration for the four different system configurations **A**, **B**, **C** and **D**. This graphical representation leads to the unambiguous result that the optimal designs of configuration **A** outperform the designs of the three other configurations in all points. Therefore, **A** is clearly the best configuration in terms of efficiency and specific cost.

5.6.2 Best system configuration and best topology

As it can be seen in figure 5.11, the Pareto optimal designs of configuration **A** are superior to all designs of the three other configurations. This is mainly due to the better utilization of the semiconductors on the secondary side due to the switchable configuration and the better performance of the 1200 V semiconductors compared to the 2000 V semiconductors. Given the superiority of configuration **A**, the designs associated with configurations **B**, **C** and **D** are excluded from further consideration in this work. Focusing exclusively on the designs of configuration **A**, the resulting plot is shown in fig. 5.12, where the solution space for each topology is detailed. Notably, within configuration **A**, each of the four topologies contributes multiple globally optimal designs.

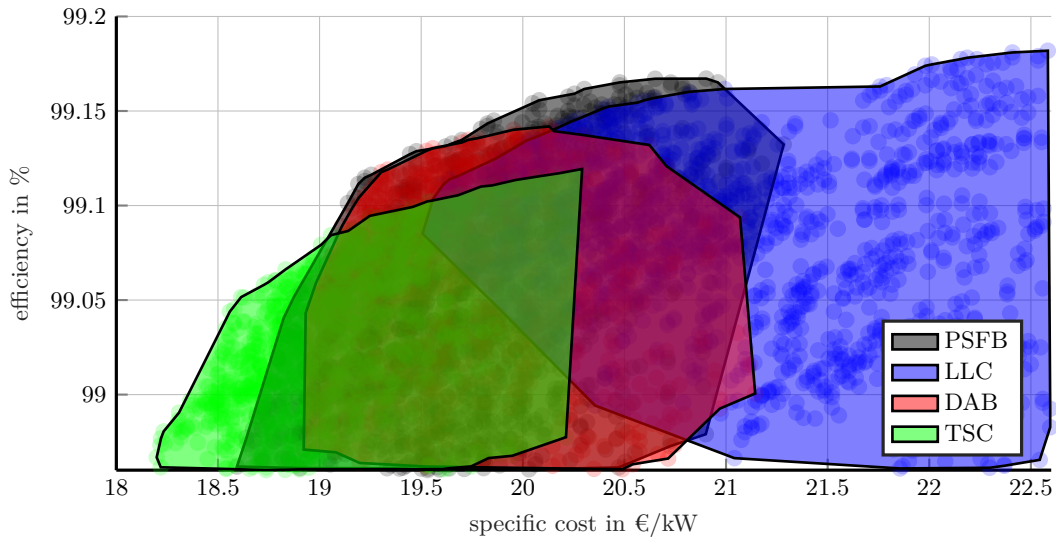


Figure 5.12 – Efficiency over cost plot for the DC-DC converter designs of the different topologies in configuration **A** with the highlighted solution space

PSFB converter

The PSFB converter designs show a wide range of solutions in terms of efficiency and cost. Compared to the other topologies, the optimal designs can be found in the middle of the specific cost range. On the Pareto front of the PSFB converter designs, there are designs with a switching frequency of 25 kHz to 60 kHz. While the low-frequency designs have high efficiency and are on the right side of the Pareto front, the higher-frequency designs feature lower cost for the passives and are on the left side of the Pareto front. It is worth noting that only low current ripple ($<50\%$) designs provide an optimal result, as the lower resulting efficiency of the high ripple designs cannot be offset by the lower cost of the inductor. In fact, the cost of a low inductance, high ripple inductor design can exceed the cost of a higher inductance design because the flux of the higher current must be handled with either a larger core cross-section or a larger number of turns.

LLC converter

With the widest range of solutions, the LLC converter offers the best way to trim a design for cost and efficiency. Furthermore, with the LLC converter, the highest efficiency can be achieved due to the lowest average semiconductor losses. While the cheaper designs do not represent a global optimum due to their lower efficiency compared to the other topologies, the optimal designs on the right side of the Pareto front represent a global optimum due to their higher efficiency. One finding for the LLC converter is that compared to the PSFB converter and the TSC, the designs can reach high cost and/or high losses while still being a valid design. This is due to the fact that different combinations of L_r and C_r result in the same resonant frequency and also provide a valid operating range. The designs with a low value for C_r require a high value for L_r at the same resonant frequency. The resulting higher inductor volume and higher voltage rating for the resonant capacitor result in higher design cost (and volume, which is not considered here) without a significant loss in performance. These designs are not shown in the plots above because they do not represent optimal designs. All values for the considered resonant frequencies can be found on the Pareto front. Again, as with the PSFB converter, lower switching frequencies provide higher efficiency, while higher switching frequencies reduce the volume and cost of the passives, especially the transformer, allowing for more cost-optimized designs.

DAB

Due to the lower component count, and the consequent lower cost compared to the other topologies, the designs for the DAB are located in the left region of the efficiency versus cost plot, especially when compared to the topologies operating at the same power level, the PSFB and the LLC converter. The DAB shows the smallest range of valid solutions in terms of cost, while having a very high range in the efficiency direction of the plot (better visible in the plot of all designs in fig. 5.11). This is due to the fact that the non-optimized inductance values (see section 4.4) are also calculated and displayed. Although the design is valid (only possible with high cooling performance), the high primary rms current leads to high losses in the transformer and inductor windings, as well as increased conduction losses in the primary and secondary side semiconductors. Especially for the combinations of

low switching frequency and low inductance, the primary peak current is very high, causing additional high switching losses in the outer areas of the output voltage range.

TSC

The left side of the plot shows the TSC designs. This means that the most cost-effective design can be realized with the TSC (only for configurations **A** and **C**, for **D** the PSFB converter has a lower specific cost). This lower specific cost is achieved with the higher permissible power level, since the cost for the auxiliary circuits (except the drivers) are assumed to be the same as for the other topologies. The specific cost of the semiconductors remains the same as for the other three topologies, since the 50 % higher power level is achieved with 50 % more semiconductors (due to the additional stage). The effect of switching frequency on cost and efficiency is the same as for the other topologies. In contrast to the PSFB converter, designs with a higher current ripple for the buck converter achieve a higher efficiency, as the turn-on losses of the considered semiconductor are higher by a factor of about four compared to the turn-off losses. A higher ripple means a lower turn-on current and therefore lower losses, for the high-side switches of the buck converter, which offsets the higher turn-off losses.

Comparison

To better understand the advantages and disadvantages of the different topologies, the optimal designs of each topology are examined in more detail. The first point to analyze is the distribution of costs. Figure 5.13 shows this distribution of specific costs for the optimal designs of configuration **A** for the different topologies. The fixed costs, which remain the same for all designs of a topology, are shown on the left, while the variable cost units, whose costs result from the choice of different design parameters, are shown on the right. The components that have the same cost for all designs are: the semiconductors, the drivers, the DSP (here representative of the combined cost of PCB, control and measurement circuitry), and the switches for the parallel/series configuration. The variable cost components are the transformer, inductor, cooling system, DC-link and resonant capacitors.

For the PSFB converter five different transformer and eight different inductor designs can be observed in the designs on the Pareto front. It is noteworthy, that 13 out of 15 different possible cost combinations for the cooling system can be found in the optimal designs.

For the LLC converter, the optimal designs are based on only four different designs for the resonance tank and the transformer. The 36 optimal designs then consist of one of these four designs and are distinguished by the different cooling systems, of which there are 14 different cost combinations to be found on the Pareto front. The five most expensive designs have a high cost for the resonant capacitor and represent an optimal solution due to a high efficiency with at low switching frequency and a high C_r to L_r ratio.

Although designs with different switching frequencies are on the Pareto front of the DAB, the price of the transformer does not differ significantly because the number of cores and turns for the optimal designs do not differ. This can be explained by the fact that the frequency range of the optimal designs is relatively narrow and the primary current is almost identical, which does not result in more optimal combinations of the number of cores and turns. Although the inductance changes for the different frequencies, the price changes are small because

the number of cores remains constant and only the number of turns changes. The largest difference in cost for the optimal DAB designs is therefore in the cooling system, where there are 14 different cost combinations.

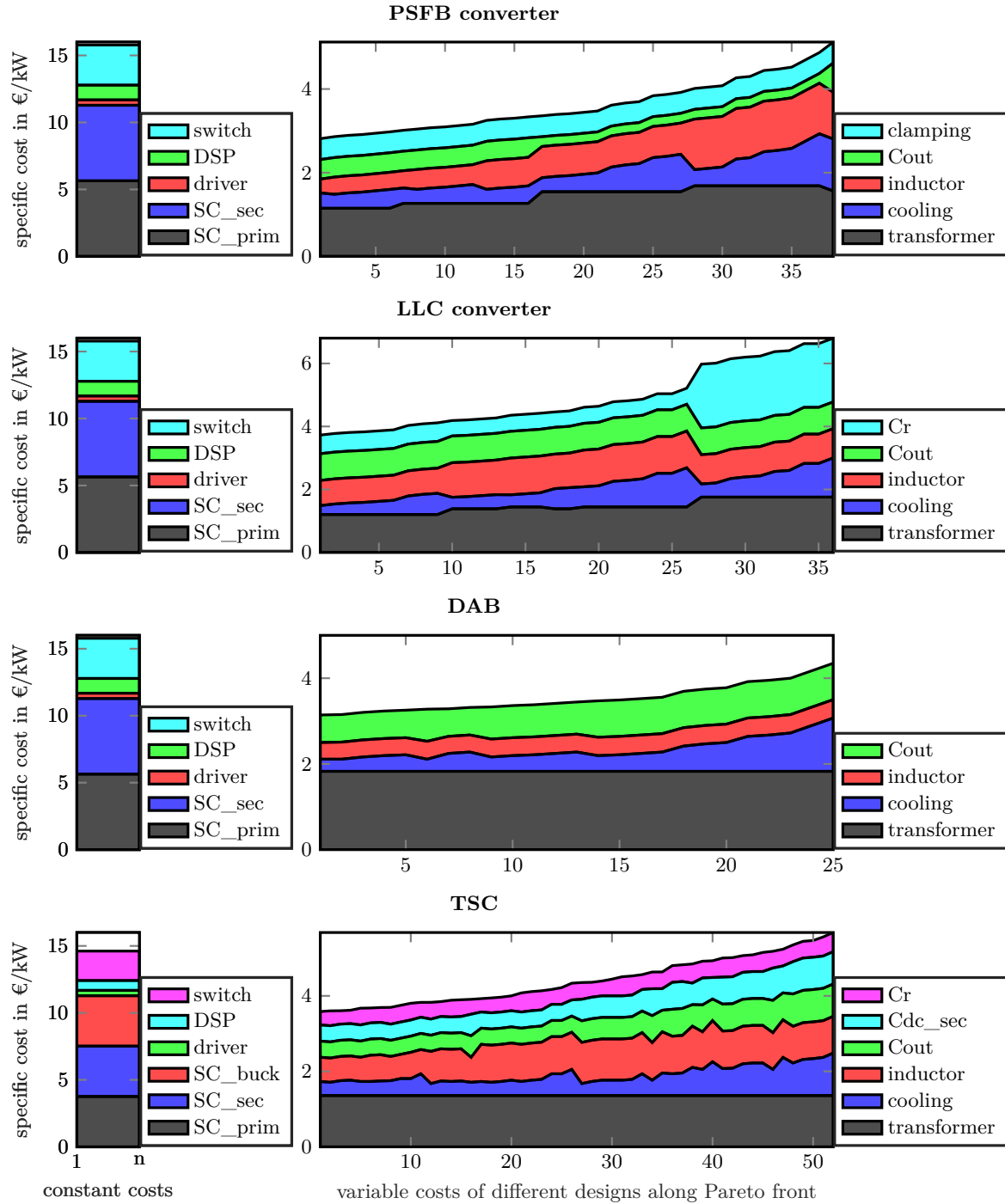


Figure 5.13 – Distribution of the cost of the Pareto optimal designs for the different topologies in configuration **A**. Left: constant costs that are the same for each design, such as semiconductors, drivers and control, and the parallel/series switch. Right: variable cost distribution along the Pareto front (total costs from low to high), among the passive components considered.

The same phenomenon as for the DAB transformer can be seen here for the transformer for the optimal designs of the TSC. The small frequency range of the optimal solutions means that a single transformer design is used for the optimal designs. Eight different buck inductor designs for the different combinations of switching frequency and ripple, and 24 out of 43 possible cooling system cost combinations can be found among the optimal designs.

The second point to analyze is the distribution of losses in the different topologies. The components considered are the semiconductors, the transformer, the inductor and the capacitors. Fig. 5.14 shows this distribution of losses for the optimal designs of the different topologies in configuration **A**. The losses are weighted by the output power and averaged for the different output voltages. It can be seen that the share of the capacitors in the total losses is almost negligible.

For the optimal PSFB converter designs, a large portion of the total losses occur in the primary-side semiconductors. In general, the lower cost designs have higher primary-side losses due to the higher switching frequency. The secondary-side semiconductor losses vary slightly for the different ripple currents due to the different rms values of the currents through the switches. Transformer losses are also within a small range for all designs, while inductor losses increase moderately with lower frequency due to the increased amount of core material required.

For the LLC designs, the secondary-side semiconductor losses remain about the same over the different switching frequencies of the optimal designs (due to ZCS), while the losses of the primary-side semiconductors decrease with decreasing switching frequency. The sum of transformer and inductor losses is almost the same for the optimal designs, while the proportions are minimally different.

The semiconductor losses for the DAB decrease with decreasing switching frequency for both the primary and secondary sides. The same can be observed for the inductor, while for the transformer the losses increase slightly.

For the TSC the semiconductor losses on the secondary side remain almost the same within the optimal designs. The losses on the primary side vary for the different switching frequencies of the isolation stage. Since the losses of the semiconductors of the buck converter dominate (decreasing with decreasing switching frequency), the different primary-side losses are distributed along the Pareto front. The losses in transformer and inductors vary only marginally for the optimal designs.

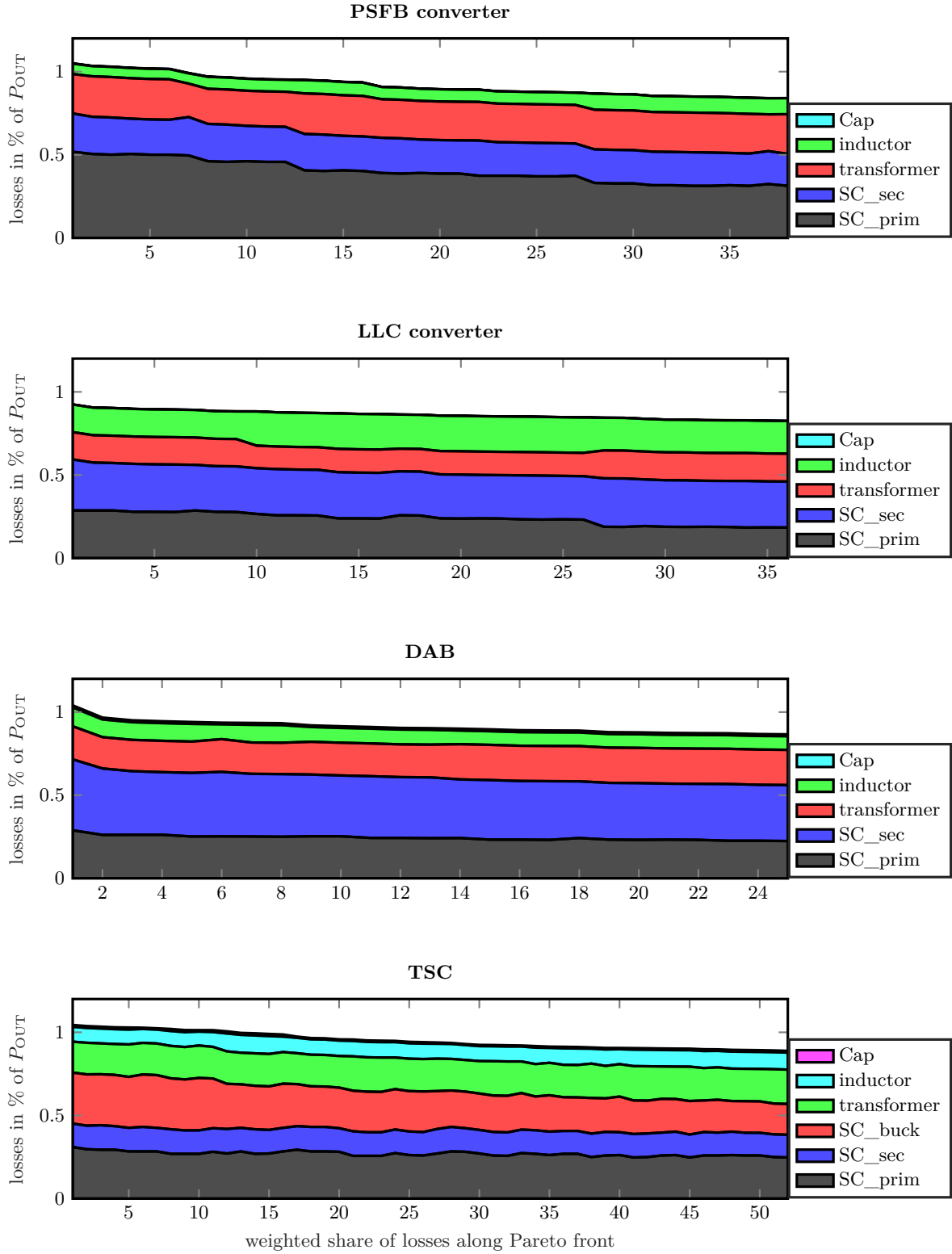


Figure 5.14 – Distribution of the losses of the Pareto optimal designs for the different topologies in configuration **A**. The losses are weighted to match the efficiency plot and form the average losses that occur in the different components for the different output voltages at full output power.

Best topology and best design

Since each of the four topologies provides designs that represent a global optimum, the best topology cannot be found without considering other aspects. One such aspect could be output voltage dependent efficiency. Figure 5.15 shows the efficiency curves for selected configuration **A** designs from the center of the topology-specific Pareto fronts. Note that the efficiency appears to be higher than in the previous plots. This is due to the fact that the efficiencies for the submodule output voltages 375 V (giving 750 V in series configuration), 562.5 V, and 750 V are averaged for the design calculation. The most suitable topology could be selected with a given voltage profile, which indicates what percentage of the converter's lifetime it will operate at what output voltage.

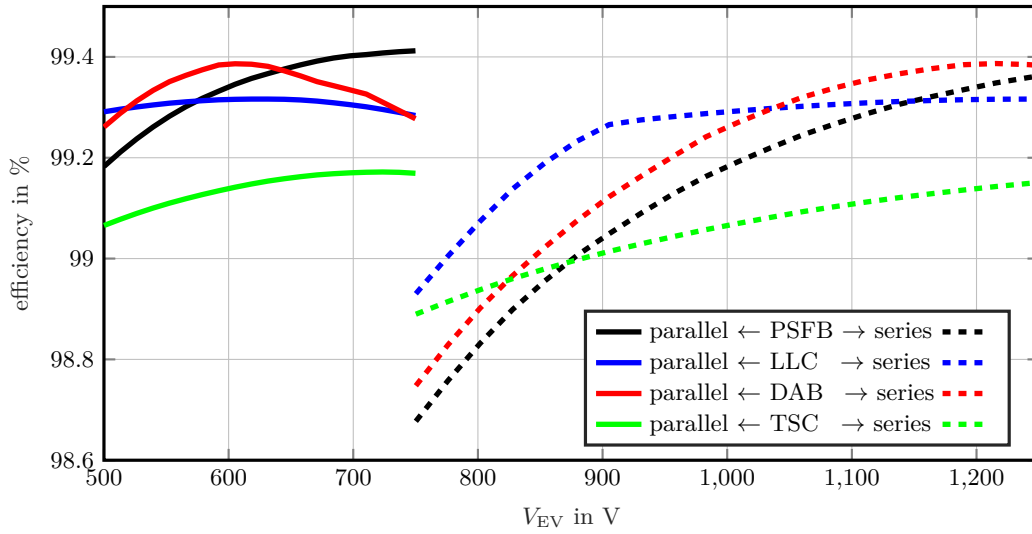


Figure 5.15 – Efficiency vs. system output voltage for the different topologies in parallel and in series configuration for one out of the optimal designs on the Pareto front

Another way to select an optimal design is to reduce the optimization problem to one dimension. This can be achieved by calculating the specific life-cycle cost, assuming an average efficiency, pricing the losses over the lifetime and adding them to the initial (material) cost of the converter. Using an example energy price, the specific life-cycle cost is calculated for different numbers of operating hours. With an assumed energy cost of $c_{\text{energy}} = 10 \frac{\text{ct}}{\text{kWh}}$, the comparison of the specific life-cycle costs of the optimal designs of configuration **A** is shown in fig. 5.16. The optimal converter designs in terms of life-cycle costs are highlighted on the corresponding Pareto front.

For a low number of operating hours, the cost of the converter dominates the life-cycle cost, which is why the TSC shows the most cost-effective designs. As the lifetime increases, the cost of losses exceeds the initial cost of the converter and higher efficiency begins to pay off. It can be seen that from 10 khr of full load, the PSFB converter shows the most cost-effective overall designs. Although the lifetime is highly dependent on the environmental conditions, a very long lifetime should be achieved for sustainability reasons.

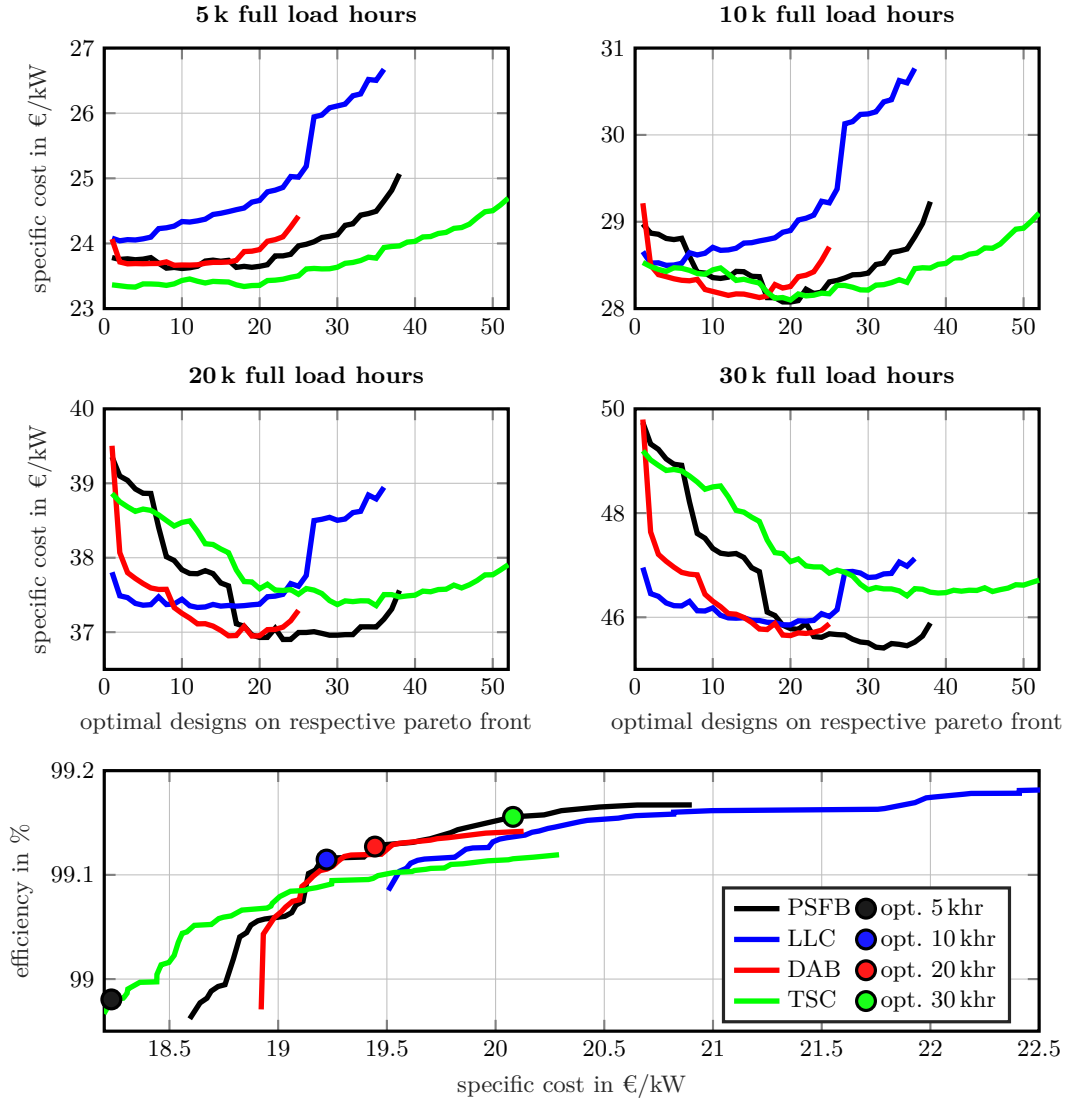


Figure 5.16 – Specific life-cycle cost of the different optimal designs of each topology of configuration **A** for a different number of operating hours, where the price for the losses is $10 \frac{\text{ct}}{\text{kWh}}$. The most cost-effective designs for 5, 10, 20 and 30 khr are highlighted on the corresponding Pareto front.

Therefore, the optimal PSFB converter design for a lifetime of 30 khr, number 32 on the topologies Pareto front, is selected as the best design. For example, 30 khr is equivalent to about one third of operating time in ten years. The design uses a switching frequency f_{sw} and a permissible current ripple diL from the lower end of the design variable set. Table 5.10 shows the parameters and values used for the selected design and how the passive components are designed.

Table 5.10 – Parameters and values for the best design

Parameter	Value
Topology	PSFB converter
Configuration	A
$P_{SM,PSFB}$	50 kW
f_{sw}	25 kHz
diL	30 %
Semiconductors	FF4MR12W2M1H (prim. and sec.)
Inductor	$L_f = 49 \mu\text{H}$, 5 x E100, N87, $n = 8$, airgap = 5.5 mm
Transformer	2 x U93, N87, $n = n_s/n_p = 9/8$
Capacitor	$C_{OUT} = 240 \mu\text{F}$ (3 x Vishay MKP1848C68080JY5)
Heatsink prim.	$R_{th,ha} = 0.09 \text{ K/W}$, $l/w/h = 100/120/80 \text{ mm}$, $n_{fin}=24$
Heatsink sec.	$R_{th,ha} = 0.1 \text{ K/W}$, $l/w/h = 80/160/67 \text{ mm}$, $n_{fin}=31$

The maximum output power of the converter is $P_{SM,PSFB} = 50 \text{ kW}$, resulting in a system power of 100 kW making it fully suitable for NCS. For MCS, a parallel connection of nine such systems is suggested to achieve the required power level of 900 kW. This scalability also allows for possible higher power levels that may be required in the future. Figure 5.17 shows the block diagram for the chargers of the MCS charging lane connected to the DC distribution grid and the full DC-DC converter in the charger with the highlighted PSFB converter in the parallel connection of nine converter systems.

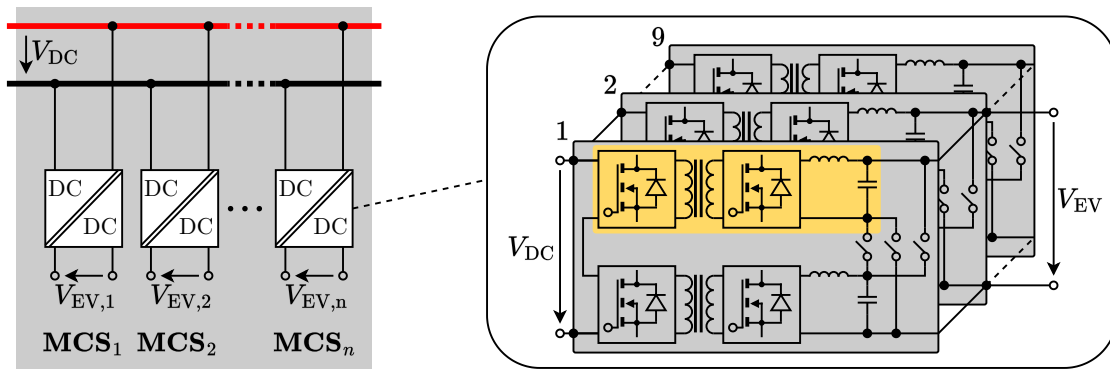


Figure 5.17 – Chargers of the MCS lane and highlighted PSFB converter design in the 900 kW charging system

5.6.3 Findings

Effect of the switchable secondary sides

As it is already discussed, the optimal designs of the configuration **A** are superior to those of the other three configurations. The switchable secondary side configuration (already seen in fig. 4.5) allows for a lower maximum output current per submodule compared to the directly connected configurations. This results in a higher power rating of the converters and thus a lower specific cost (offsetting the cost of the additional switches).

Small range of optimal solutions for the magnetics

The design routines for transformer and inductor select the best design by the lowest cost (see section 5.2). Combined with the limited number of different cores, this results in only a small number of different magnetics within the optimal designs. Furthermore, this type of optimization results in slightly less efficient designs, as the cheaper designs generally result in higher losses. To avoid this effect, the magnetics could be optimized for both cost and efficiency dimensions (as with the cooling system and converter designs) instead of this cost-only optimization. This has been explored at the topology level, but the relative result is not really affected (except for the higher diversity of magnetic designs). Another point is that the design routines are already struggling to find solutions for these high power levels using existing core sizes (resulting in a relatively high number of stacked cores), which limits the number of valid magnetic designs. For this reason, and due to the massively increased computational complexity, it was decided for this work to keep the multi-objective optimization in its introduced form.

5.7 Potential of the converters of the configuration **A**

The previous section established the superiority of configuration **A** over the other configurations. This section discusses additional possibilities for the four converter topologies in this configuration.

5.7.1 Reusability of the MCS converters for HPC (CCS)

Reusability and synergy with other products are key to achieving more cost-effective solutions in power electronics design. Not only development costs, but also maintenance and product lifecycle management efforts can be reduced. Higher annual turnover of components such as semiconductors and passives further reduces the cost. Therefore, the aim here is to propose the reuse of the modular units of the MCS DC-DC converter designs from section 5.6 also for HPC applications. While the converters in the configurations **B** and **D** are designed for full power only from an output voltage of 500 V, the series connection of two secondary sides in configurations **A** and **C** at 750 V requires the individual DC-DC converter modules to achieve full power already at 375 V. Therefore, the configuration **A** and **C** converters can also be used directly for HPC charging and deliver full power even at the important HPC voltage of $V_{EV} = 400$ V. Therefore, as shown in fig. 4.5 (on the right), the DC-DC converters

of configurations **A** and **C** cover the CCS standard and could be reused for the HPC in the charging park.

5.7.2 Input voltage flexibility

The submodules of configuration **A** are connected in series on the primary side to achieve the required voltage rating for the 1500 V DC grid. Without restriction of function, these primary sides could also be configured in parallel and connected to a 750 V DC link. In this way, the converters could also be used for the other distribution grid types presented in chapter 3 (provided that the AC-DC converter provides an appropriate DC-link voltage).

5.8 Conclusion

This chapter details design routines for both active and passive components, as well as complete design procedures for isolated DC-DC converters. The four different topologies PSFB converter, LLC converter, DAB, and TSC, presented in the previous chapter are considered. The design routines are employed to generate a variety of designs by systematically varying the topology-specific design parameters for a MCS application with the wide output voltage range of 500 V to 1250 V. A multi-objective optimization considering both cost and efficiency is performed for each topology and system configuration as well as for all designs, to find the global optimal designs. Among the configurations analyzed, configuration **A** yields the best overall results for all topologies. This finding suggests that the performance improvements achieved by incorporating switchable secondary sides outweigh the additional cost introduced by the extra switches. From a life-cycle cost perspective, one PSFB converter design has proven to be the best overall design. Additional possibilities of the configuration **A** converters are explored.

6 Design and implementation of a DC-DC converter with solid-state parallel-series changeover switch

This chapter deals with the analysis of a PSFB-based DC-DC converter with switchable secondary-side configuration. Instead of using relays to switch between parallel and series configuration, this proposed topology uses MOSFETs. As shown in the previous chapter, the PSFB converter shows very good results in terms of cost and efficiency. The proposed converter is designed for the MCS voltage range and for the connection to the 1500 V DC grid in the charging park. In a first step, the proposed topology is analyzed by studying the individual circuit parts and calculating the system variables. In the second step the different components (active and passive) of the converter are dimensioned, based on the equations of the section 4.2. A simulation of the dimensioned system is then carried out to show the main function. Finally, an experimental validation is performed using a hardware prototype. The content of this chapter is based on the work already published in [100] and [101].

6.1 Introduction

The underlying problem that led to the idea of a solid-state switch for parallel/series configuration is that the relay solution requires either the configuration to be selected before charging or the charging to be interrupted. With the proposed topology (see fig. 6.3) the transition from parallel to series can be effected in a single switching cycle because there is no need to charge/discharge large output capacitors, resulting in seamless power transfer over the entire output voltage range. This allows the benefits of both parallel and series operation to be realized in a single charging session, providing the highest efficiency not only for the 400 V and 800 V battery types (for HPC), but also for batteries with a different voltage (e.g. 600 V or >1000 V).

6.2 The proposed converter topology

This section presents and analyzes the proposed DC-DC converter. The different circuit parts are studied and the system variables are identified and calculated.

6.2.1 Conventional PSFB DC-DC converter with active rectification

The conventional PSFB converter is already introduced and analyzed in 4.2. The proposed topology consists of two PSFB submodules with active rectification and active clamping

circuit featuring a common output filter (consisting of L_f and C_{OUT}). The parallel/series changeover switches are located between the active rectifier and the output filter. This allows a very fast transition between parallel and series configuration, since the voltage at the output capacitor does not change during transition (provided that the phase shift of the primary-side bridges is halved when switching from parallel to series configuration and doubled otherwise).

In fig. 6.1 the circuit diagram of the conventional PSFB converter submodule with active rectifier and active clamping circuit is shown.

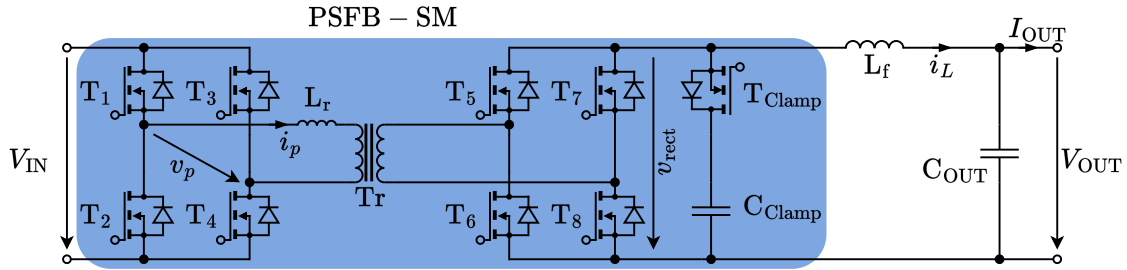


Figure 6.1 – Circuit diagram of the PSFB submodule with active rectifier and active clamping circuit

6.2.2 Parallel/series changeover switches

There are two options for the positioning of the parallel/series changeover switches: one is to interconnect the outputs of the two PSFB converters (after the output capacitor), the other is to place the switches between the output inductor and the rectifier. The advantage of the latter is, on the one hand, that only one output inductor and one capacitor are needed, and on the other hand that the transition from parallel to series configuration and vice versa can be realized instantaneously since the output capacitors do not have to be charged/discharged during transition. In this case, the output inductor and capacitor must be rated for full output current and full output voltage, respectively. Figure 6.2 shows how the changeover switches are placed between the two PSFB-submodules (PSFB-SM, indicated in fig. 6.1).

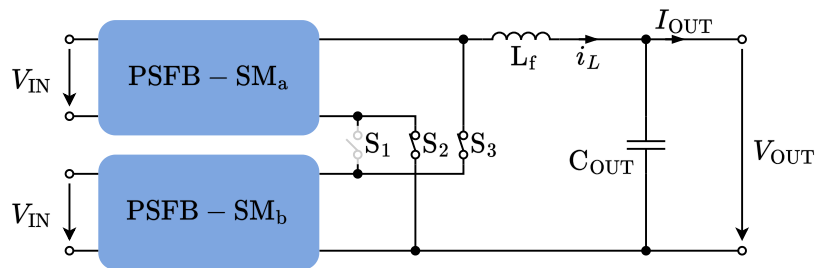


Figure 6.2 – Circuit diagram of the overall converter in parallel configuration including the two PSFB submodules PSFB – SM_a and PSFB – SM_b, the changeover switches $S_{1..3}$ for the parallel/series configuration of the secondary sides and the common output filter

The switch position indicated in fig. 6.2 marks the parallel configuration, since S_2 and S_3 connect the negative and positive rectifier output of PSFB – SM_a with the corresponding

outputs of PSFB – SM_b. In order to change the configuration to series, the switch S_1 is closed, connecting the negative output of PSFB – SM_a with the positive output of PSFB – SM_b, while the switches S_2 and S_3 are opened.

6.2.3 Full topology with active rectification and clamping

The full circuit diagram of the proposed topology is given in fig. 6.3. The two inputs of the primary sides are permanently connected either in series or in parallel. For the 1500 V DC grid in the charging park, the series connection is required when using 1200 V semiconductors. Figure 6.3 shows the full circuit diagram of the proposed topology.

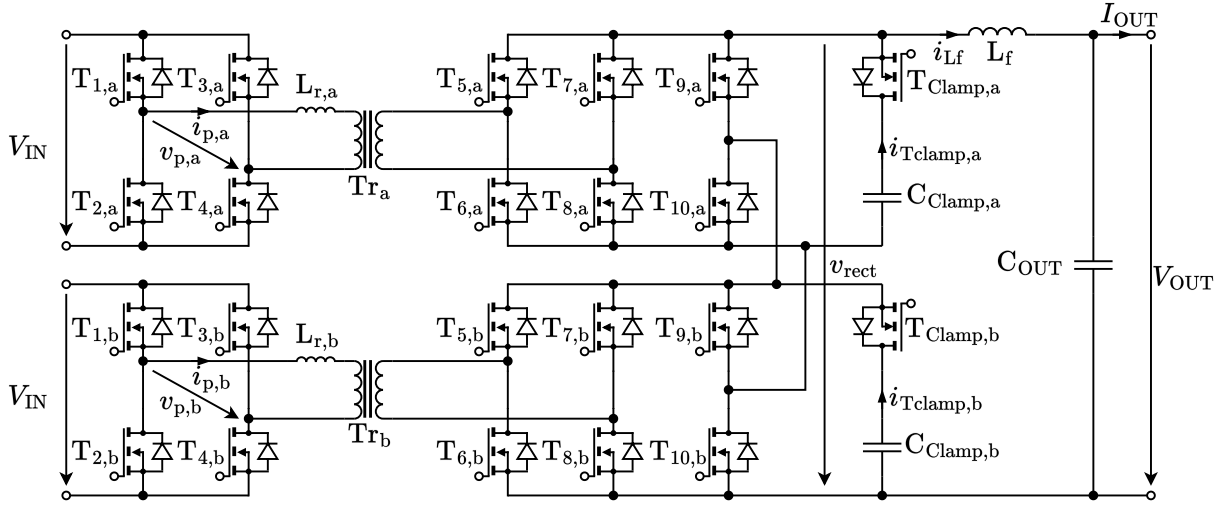


Figure 6.3 – Full circuit diagram of the proposed topology including two PSFB converters with active rectifier and clamping and one common output filter. The solid-state switch is realized with two half bridges consisting of the MOSFETs $T_{9/10,a/b}$

The transistors $T_{x,a}$ and $T_{x,b}$ (with $x \in \{1,2,\dots,8\}$) are the switches from the two conventional PSFB converter submodules. The changeover switches are realized in a symmetrical way so that half-bridge modules can be used to achieve higher power levels. The two SM are connected in parallel when the outer switches $T_{9,a}$ and $T_{10,b}$ are on and in series when $T_{10,a}$ and $T_{9,b}$ are on. In the circuit diagram in fig. 6.3 it can be observed that the switches $T_{10,a}$ and $T_{9,b}$ are connected parallel. This is useful since during their on state (series configuration) the current is shared between those two transistors.

6.2.4 Analysis of the current paths

In order to better understand the function of the circuit, the paths of the current flow are examined in more detail. The two primary sides are connected in series. In principle, one switching period of the converter consists of three different phases: positive and negative voltage across the transformers and freewheeling.

Fig. 6.4 shows the path of the current during positive voltage on the transformers $Tr_{a/b}$ for parallel configuration. For a positive voltage across the transformer the switches $T_{1,a/b}$

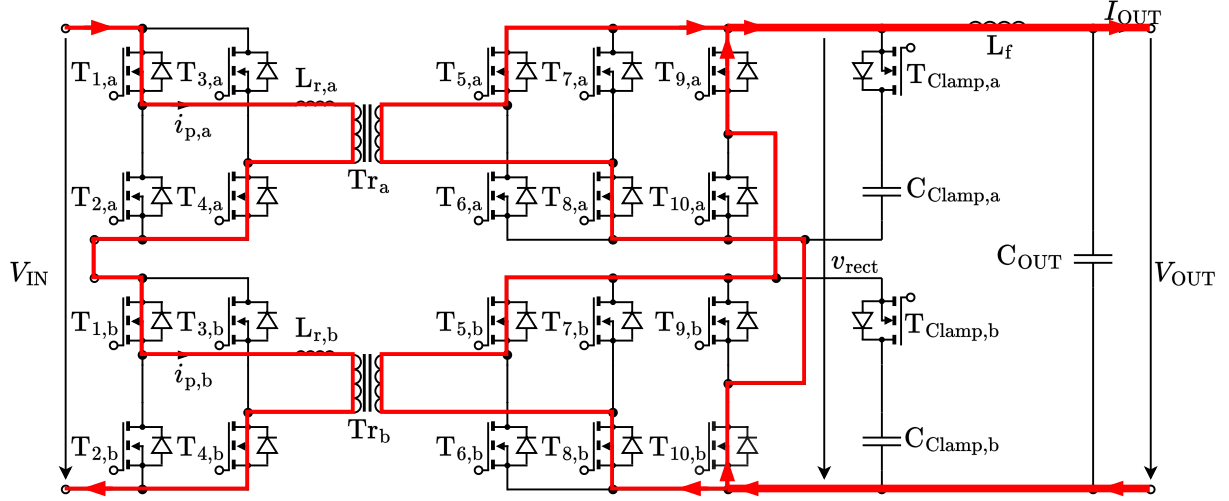


Figure 6.4 – Circuit diagram of the proposed topology in parallel configuration during positive transformer voltage with highlighted current flow path

and $T_{4,a/b}$ and correspondingly, the switches of the active rectifier $T_{5,a/b}$ and $T_{8,a/b}$ are on. Because of the parallel configuration of the secondary sides, the outer changeover switches $T_{9,a}$ and $T_{10,b}$ are on and the output current I_{OUT} corresponds to the DC component of the sum of the currents of the two submodules.

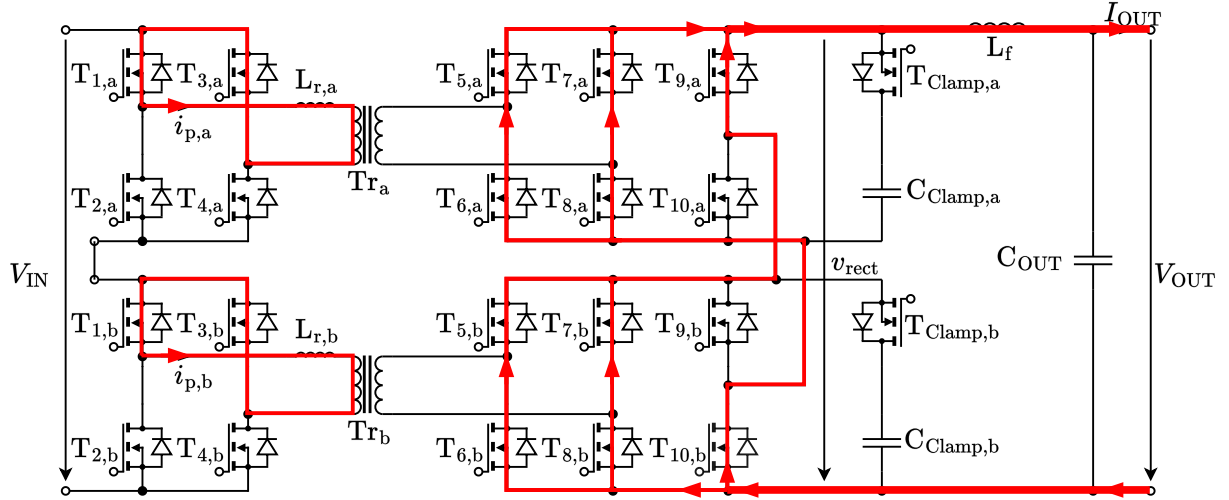


Figure 6.5 – Circuit diagram of the proposed topology in parallel configuration during freewheeling with highlighted current flow path

In fig. 6.5 the path of the current during freewheeling in parallel configuration is shown. In this case, the freewheeling phase after the transition from positive to zero voltage across the transformers $Tr_{a/b}$, with $i_{p,a/b} > 0$ is shown. When $T_{4,a/b}$ are turned off (at the transition from positive to zero voltage across the transformer), the current continues to flow and commutates to the body diodes of $T_{3,a/b}$. This enables ZVS for these two switches. The freewheeling primary-side current then flows through $T_{1,a/b}$ and $T_{3,a/b}$, as well as through the

transformer. On the secondary side, all rectifier switches $T_{5-8,a/b}$ are on (in rectifying mode 2, as for the PSFB converter), resulting in low conduction losses during this freewheeling phase.

The current path for the series configuration and positive voltage across the transformers $Tr_{a/b}$ is shown in fig. 6.6. As for the parallel configuration the switches $T_{1,a/b}$, $T_{4,a/b}$, $T_{5,a/b}$ and $T_{8,a/b}$ on. The switches $T_{10,a}$ and $T_{9,b}$ (direct parallel connection) are on to enable the series configuration. The resulting rectified voltage v_{rect} is therefore the sum of the two submodule voltages.

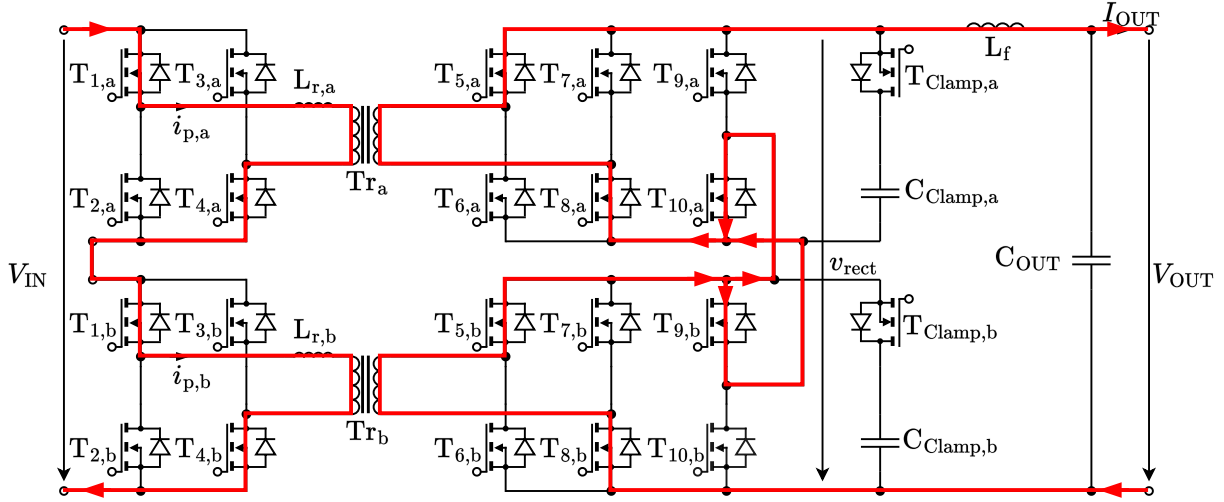


Figure 6.6 – Circuit diagram of the proposed topology in series configuration during positive transformer voltage with highlighted current flow path

Also for the series configuration, the current path for the freewheeling phase after the positive transformer voltage phase is shown in fig. 6.7. As for the parallel configuration the converter operates in rectifying mode 2 with all rectifier switches $T_{5-8,a/b}$ on. For the series configuration also the outer changeover switches $T_{9,a}$ and $T_{10,b}$ can be turned on during the freewheeling phase providing an additional path for the freewheeling current. This modulation is described below and referred to as advanced control strategy for the changeover switches.

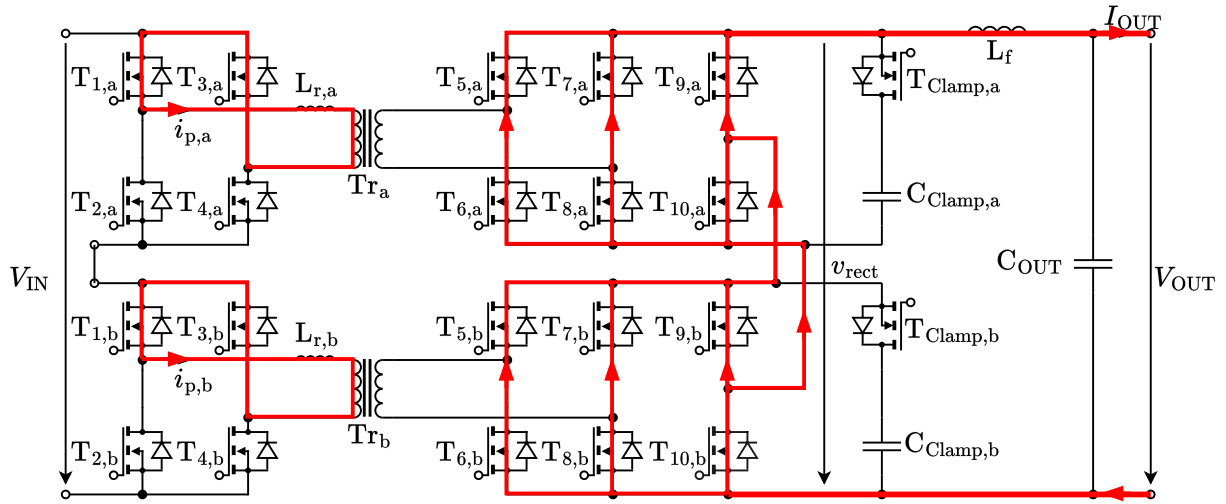


Figure 6.7 – Circuit diagram of the proposed topology in series configuration during freewheeling with highlighted current flow path: The outer switches ($T_{9,a}$ and $T_{10,b}$) are closed and provide an additional path for the freewheeling current

6.2.5 Primary side current shaping using the active clamping circuit

As in the conventional PSFB converter, the parasitics of the transformer and switches lead to a poorly damped ringing at the secondary-side switches (at v_{rect}), since they are not naturally clamped by the output capacitor (compared to the other topologies presented before). To avoid the destruction of the switches or to accept a decrease in efficiency due to this effect, an active clamping circuit (as described in section 4.2) is applied to this topology. Figure 6.8 shows the waveforms of the voltage across the rectifier v_{rect} for an ideal circuit (black), a real circuit without clamping (blue) and the damped ringing with the active clamping circuit (red). The clamping switches $T_{Clamp,a/b}$ are turned on when v_{rect} is high, directing the energy of the overshoot to the capacitors $C_{Clamp,a/b}$, and recovering this energy when the capacitors voltage is higher than v_{rect} by discharging it into the output capacitor.

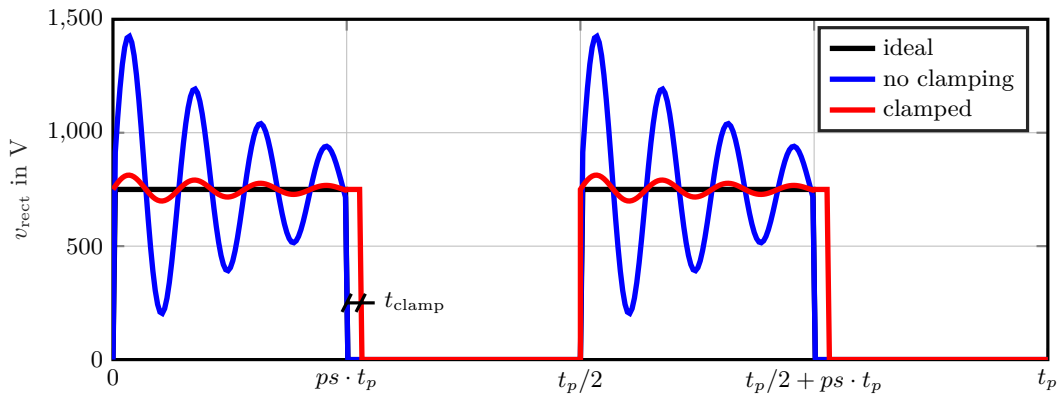


Figure 6.8 – Voltage across the rectifier v_{rect} at a phase shift of $ps = 50\%$: ideal waveform, overshoot and ringing due to the parasitics, and active clamped voltage

This clamping circuit can also be used to reduce losses on the primary-side switches. An advanced modulation scheme can be used to control the clamping switches $T_{\text{Clamp},a/b}$ [102]: After the transition from the energy transfer phase to the freewheeling phase the switch is kept on for a short time t_{clamp} . This keeps the voltage applied across the rectifier and therefore the transformer is not shortened on the secondary side. The energy stored in the stray inductances $L_{r,a/b}$ can no longer circulate on the primary side and is forced to flow to the output, reducing conduction losses in the primary-side switches. Since the shape of the primary-side current differs from the normal operation mode, this modulation will be referred to as current shaping. The main challenge of controlling the switch is to determine the correct length of the pulse (t_{clamp}), applying the clamping voltage just long enough to discharge the energy stored in $L_{r,a/b}$. If the pulse is too long the clamping transistor experiences additional losses. If the pulse is too short not all the energy stored in $L_{r,a/b}$ is brought to zero and conduction losses in the primary-side switches occur during the freewheeling phase. Even though current shaping can also be realized for the conventional PSFB converter with active clamping it is not assumed for the designs in chapter 5.

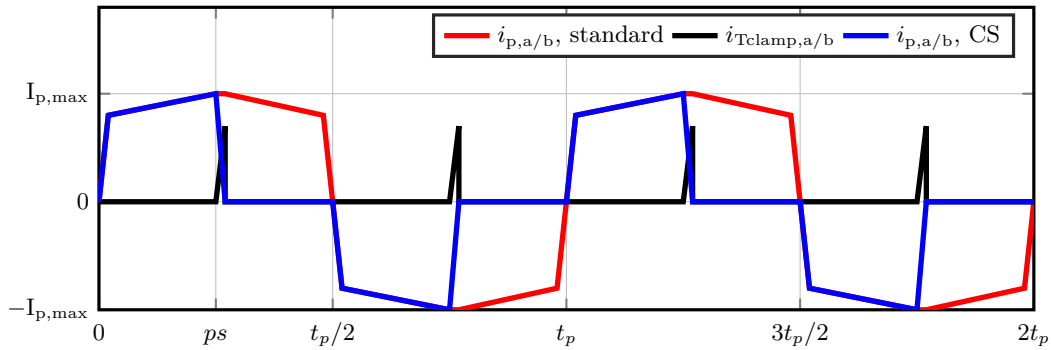


Figure 6.9 – Idealized waveforms for primary-side transformer current i_p with and without current shaping (CS) and the current through the clamping switches $T_{\text{Clamp},a/b}$ at a phase shift of $ps = 50\%$.

Figure 6.9 shows the difference in the primary-side current $i_{p,a/b}$ if the converter is operating in normal mode (red) and in current shaping mode (blue). In this case the current is ideally brought to zero, resulting in lowest conduction losses for the primary-side switches. The current through the clamping switch $i_{T\text{Clamp},a/b}$ is exemplarily shown (black). For this plot it is assumed, that the capacitors $C_{\text{Clamp},a/b}$ are charged only via the body diode of T_{Clamp} . If T_{Clamp} is also used to support the diode during clamping, $i_{T\text{Clamp},a/b}$ becomes negative during the phases of $v_{\text{rect}} > 0$.

In order to estimate the time needed to bring the freewheeling current to zero, the peak current through the stray inductance needs to be determined. The current ripple through the output inductor is

$$\Delta I_{Lf} = ps \cdot \frac{n \cdot V_{\text{IN}} - V_{\text{OUT}}}{4f_{\text{sw}} \cdot L_f} \quad (6.1)$$

with the phase shift $ps = 0..100\%$ and the turns ratio of the transformer $n = n_s/n_p$. Added to the output current and reflected to the primary side, the maximum primary-side current

$$I_{p,\max} = n \cdot \left(ps \cdot \frac{n \cdot V_{\text{IN}} - V_{\text{OUT}}}{4f_{\text{sw}} \cdot L_f} + I_o \right) \quad (6.2)$$

can be calculated. The current slope on the primary side of the transformer during the duty-cycle loss is determined by the stray inductance. Therefore the time needed to bring the primary-side current $i_{p,a/b}$ from $I_{p,max}$ to zero can be estimated to

$$t_{clamp} = \frac{L_r \cdot I_{p,max}}{V_{IN}}. \quad (6.3)$$

Voltage drops, either ohmic or across the inductive voltage divider between L_r and the main inductor, as well as the rising/falling times of the switches are neglected here as the influence is negligible.

6.2.6 Advanced control strategy for loss reduction

The overall efficiency of the converter can be increased with an advanced modulation strategy for the changeover switches. In the series configuration the outer switches $T_{9,a}$ and $T_{10,b}$ are off, while the inner switches $T_{10,a}$ and $T_{9,b}$ are on. During freewheeling the voltage across the outer switches is zero (if the voltage drop of the rectifier is neglected). If the outer switches are turned on during this freewheeling phase they can support the rectifier by sharing the current (see fig. 6.7) and therefore reduce losses and spread the heat on a larger area of the heat sink. This loss reduction is dependent on the phase shift and decreases with higher output voltage. For the parallel configuration this modulation strategy is not applicable as the inner switches are not in the path of the freewheeling current.

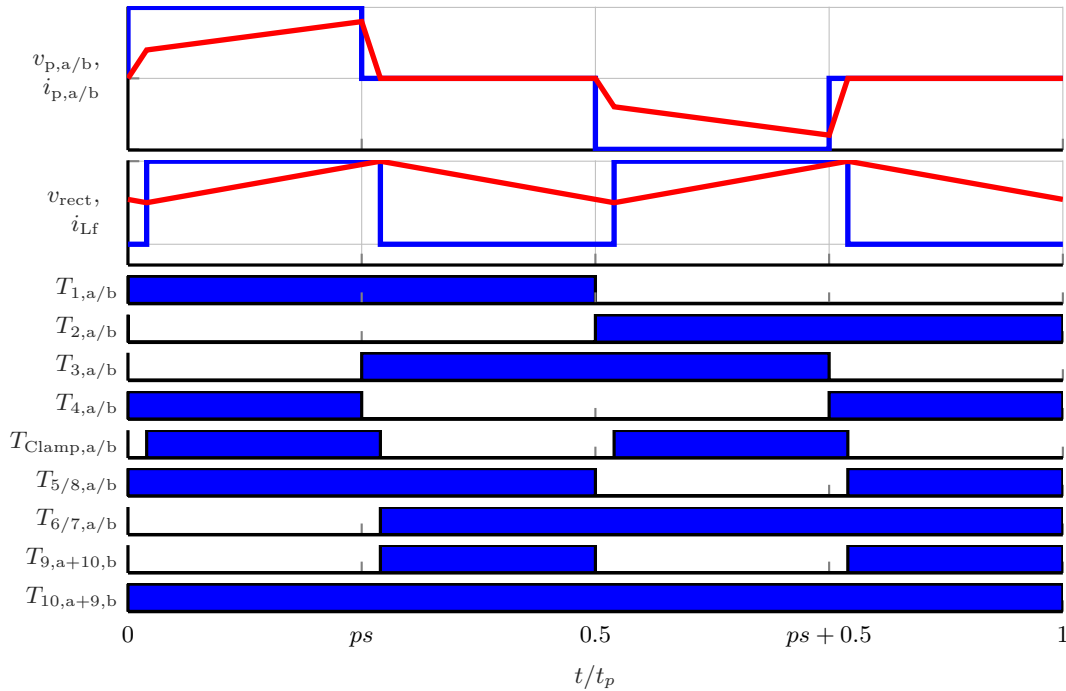


Figure 6.10 – Switching states and waveforms for the proposed topology (fig. 6.3) in active rectifying mode 2 with the advanced control scheme for the outer switches $T_{9,a}$ and $T_{10,b}$ in series configuration ($T_{10,a}$ and $T_{9,b}$ are on continuously)

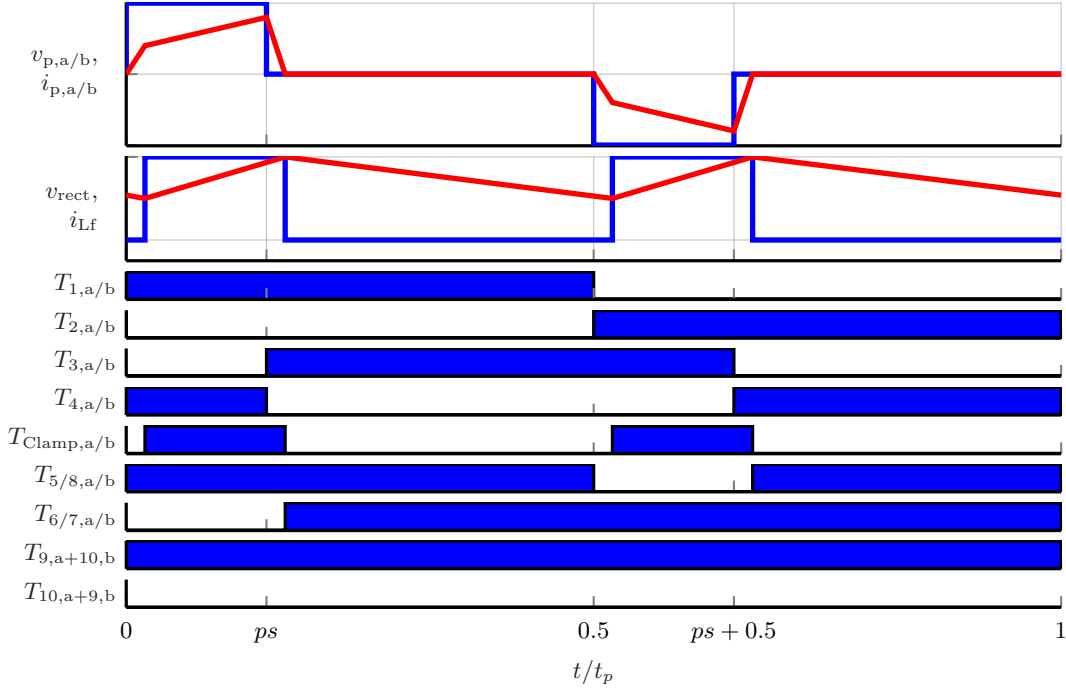


Figure 6.11 – Switching states and waveforms for the proposed topology (fig. 6.3) in active rectifying mode 2 in parallel configuration ($T_{9,a}$ and $T_{10,b}$ are on continuously)

Figure 6.10 shows the states of the switches of the converter and the characteristic waveforms in series configuration. It can be seen that the rectifier operates in mode 2 (according to the section 4.2). The outer changeover switches $T_{9,a}$ and $T_{10,b}$ are turned on during the freewheeling phase while the inner switches $T_{10,a}$ and $T_{9,b}$ are always on. Since the voltage across the rectifier during freewheeling is zero the outer switches achieve zero voltage switching (ZVS) and operate with twice the switching frequency of the primary side. Fig. 6.11 shows the switching states and waveforms for the parallel configuration.

6.3 Dimensioning of the components

This section describes the dimensioning of the active and passive components for the proposed topology. The equations are derived from the PSFB converter (section 4.2).

6.3.1 Passive components

The topology is characterized by three main passive components: The transformer T_r , the output inductor L_f and the output capacitor C_{OUT} .

Transformer

The design parameters of the transformer are the turns ratio $n = n_s/n_p$ and the stray inductance L_r . Two main operating points determine n : The maximum output voltage $V_{\text{out,max}}$, which has to be achieved in the series configuration and the voltage $V_{\text{tr,p/s}}$ at which the transition from parallel to series configuration takes place. Since $V_{\text{tr,p/s}} \geq V_{\text{out,max}}/2$, n can be determined by solving

$$\frac{V_{\text{tr,p/s}}}{V_{\text{IN}}} = n - n^2 \cdot I_{\text{OUT}} \cdot \frac{L_r}{V_{\text{IN}}} \cdot f_{\text{sw}}. \quad (6.4)$$

The second term describes the duty-cycle loss, which depends on the stray inductance L_r , the switching frequency, the input voltage and the output current [103]. Since additional factors such as dead-time and the resistive voltage drop on active and passive components further increase this duty-cycle loss, n should be selected slightly higher than calculated. The stray inductance L_r depends on the winding scheme of the transformer. A lower distance from the primary winding to the secondary winding results in a lower L_r , but lowers also the insulation strength. As in the conventional PSFB converter, L_r should be large enough to achieve ZVS for the primary-side switches, especially in the upper output power range. Although there are possibilities to extend the ZVS range to the full output power range [104] here only the ZVS range given from L_r is considered. Via the assumed minimum output load, and therefore the minimum primary-side current, at which ZVS is desired, the value of L_r arises to

$$L_r \geq \frac{C_r V_{\text{IN}}^2}{I_{\text{min,zvs}}^2}, \quad (6.5)$$

with $C_r = \frac{8}{3}C_{\text{OSS}} + C_T$ (parasitic MOSFET and transformer winding capacitance) [105]. For a good converter design a trade-off between insulation capability, duty-cycle loss and ZVS range has to be found. In the proposed topology two transformers are needed, the difference in the stray inductances $L_{r,a}$ and $L_{r,b}$ should be minimal, otherwise a balancing control is needed to ensure equal energy transfer in both submodules.

Output inductor

The output inductor L_f is the most critical passive component since it has different requirements for parallel and series configuration. In the parallel configuration the output current and therefore also the inductor current is maximal. For the series configuration, because of the higher voltage an increased AC ripple is seen by the inductor (inductance value and switching frequency do not change during the transition). The current ripple in the inductor peaks at 50 % phase shift, which in this case is at the lowest output voltage in series configuration. Therefore, the minimum value of L_f is calculated at the transition voltage $V_{\text{OUT}} = V_{\text{tr,p/s}}$ in series configuration as

$$L_f \geq \frac{2nV_{\text{IN}} - V_{\text{OUT}}}{2f_{\text{sw}}\Delta I_{\text{o,max}}}, \quad (6.6)$$

where $\Delta I_{\text{o,max}}$ is the maximum allowable peak-to-peak current ripple through the inductor.

Output capacitor

The output capacitance C_{OUT} is defined by the maximum output voltage ripple and the current ripple through the inductor L_f [64]

$$C_{\text{OUT}} \geq \frac{\Delta I_{L_f}}{16 \Delta V_o f_{\text{sw}}}. \quad (6.7)$$

The voltage rating of the output capacitor is $V_{\text{out,max}}$, the full output voltage in series configuration.

6.3.2 Active components

In order to dimension the MOSFETs, the semiconductor losses have to be calculated. Following two cases for the secondary-side configuration must be considered:

$$x = \begin{cases} 1 & \text{when in series} \\ 2 & \text{when parallel} \end{cases} \quad (6.8)$$

Here, the losses of the active components are calculated without current shaping (worst-case scenario) in order to avoid undersized switches.

Primary side

The RMS current through the primary-side MOSFETs can be calculated, similar as in the conventional PSFB converter, to

$$I_{\text{Tprim,rms}} = \frac{n}{x\sqrt{2}} I_o. \quad (6.9)$$

The conduction losses can then be estimated to

$$P_{\text{Tprim,cond}} = I_{\text{Tprim,rms}}^2 R_{\text{DS,on}}. \quad (6.10)$$

While the turn-on losses are negligibly small as the PSFB converter is a ZVS topology, the turn-off losses might be roughly approximated by

$$P_{\text{Tprim,sw}} = 1/2 \cdot I_{\text{OFF}} \cdot V_{\text{IN}} \cdot t_{\text{OFF}} \cdot f_{\text{sw}}. \quad (6.11)$$

These switching losses deviate in the two phase legs $T_{1-2,a+b}$ (phase-leg A) and $T_{3-4,a+b}$ (phase-leg B) since the turn-off current through the switches is different:

$$I_{\text{OFF,A}} = n \cdot x (I_o + \Delta I_{L_f}) \quad (6.12)$$

$$I_{\text{OFF,B}} = n \cdot x (I_o - \Delta I_{L_f}). \quad (6.13)$$

Active rectifier

The advanced control strategy for the changeover switches is only applicable in the series configuration. This must be considered when dimensioning the rectifier switches. Depending on the transition voltage, the output current per SM can be higher than in the parallel configuration, which may allow for a smaller chip size of the rectifier (if the advanced control strategy is considered). However, this results in a even lower efficiency at the already worst operating points (low output voltage, high current in series configuration). Therefore, the advanced control strategy is not considered and the RMS current through the rectifier MOSFETS is

$$I_{\text{Trect,rms}} = \frac{1}{x\sqrt{2}} I_o. \quad (6.14)$$

The rectifier switches do not have an voltage/current overlap and therefore neither turn-on nor turn-off losses occur. The only switching losses are the reverse-recovery losses of the body diode. The stray inductance L_r limits the di/dt and hence the reverse recovery charge Q_{rr} of the body diode. Therefore, those losses are negligible compared to the conduction losses, especially in the higher load operations.

Changeover switches

The current through the parallel/series changeover switches is

$$I_{\text{Tp/s,rms}} = \frac{1}{2} I_o \quad (6.15)$$

for the outer switches $T_{9,a}$ and $T_{10,b}$ during parallel operation as well as for the inner switches $T_{10,a}$ and $T_{9,b}$ during series configuration. Since switching only occurs during the transition from parallel to series configuration and vice versa the switching losses can be disregarded.

6.4 Simulation of the topology

In order to verify the function of the proposed topology, a PLECS simulation is made with the parameters shown in table 6.1. A model (XML file) for switching and conduction losses and thermal behavior for the SiC MOSFETs of the power module FF6MR12W2M1 provided by the manufacturer (Infineon) is used to simulate the semiconductor losses. The losses for the passive components transformers $Tr_{a/b}$ and inductor L_f are simulated by a resistor for the winding losses and by integration and scaling of the magnetic flux derived from the voltage across the component for the core losses.

Table 6.1 – Simulation parameters

Parameter	Value
P_{OUT}	150 kW
V_{OUT}	500 V to 1200 V
V_{IN}	750 V
f_{sw}	32 kHz
MOSFETs	FF6MR12W2M1 $R_{DS,on} = 6 \text{ m}\Omega$
n	1
L_r	$1.5 \mu\text{H}$
L_f	$50 \mu\text{H}$
C_{OUT}	$240 \mu\text{F}$
Relay	$R_{on} = 1 \text{ m}\Omega$
T_a	50°C

6.4.1 Modulation

The modulation for the primary side is realized as for the conventional PSFB converter, both primary-side full bridges are controlled with the same phase shift. The active rectification (mode 2) is realized as shown in fig. 6.12. The gate signals $G(T_{5/8,a/b})$ and $G(T_{6/7,a/b})$ for the rectifier are derived from the gate signals of the primary side. To avoid shorting the clamping circuits ($T_{Clamp,a/b}$ would be parallel to $C_{Clamp,a/b}$), a turn-on delay (of $t_{clamp} + t_{dead}$, $t_{dead} = 200 \text{ ns}$) is added. In addition this delay is needed to ensure that the switches are turned on at zero voltage, since the body diodes start conducting at the beginning of the freewheeling.

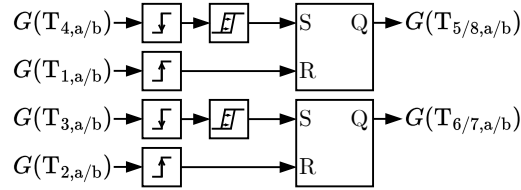


Figure 6.12 – Derivation of the active rectifier control ($G(T_{5/8,a/b})$ and $G(T_{6/7,a/b})$) from the primary-side gate signals. A turn-on delay is added to avoid a short circuit of the clamping switches and to enable ZVS.

To simulate the basic function of the topology, active clamping is not required because the parasitic components that cause voltage overshoot are not modeled. However, the reduction of the conduction losses through the use of the current shaping is applied. In the simulation the clamping switches $T_{Clamp,a/b}$ are turned on with a constant delay (t_{dead}) after the rising edge of the rectified voltage v_{rect} . This simplifies the control and additionally supports the body diodes of the clamping switches during the charging phase of the clamping capacitors. The clamping switches are turned off with a variable delay, calculated with the equation 6.3, starting at the end of the energy transfer phase with the rising edge of the condition

$$FW = G(T_{1,a/b}) \wedge G(T_{3,a/b}) \vee G(T_{2,a/b}) \wedge G(T_{4,a/b}), \quad (6.16)$$

where FW marks the freewheeling phase.

6.4.2 Waveforms at the transition from parallel to series configuration

Figure 6.13 shows the waveforms of the primary-side transformer voltage, rectified voltage, output voltage as well as primary-side and output inductor current during the transition from parallel to series connected output stages. It can be observed that the output voltage remains constant, only the voltage ripple increases slightly since the rectified voltage doubles, resulting in a higher current ripple ΔI_{L_f} through the inductor L_f . The transition takes place

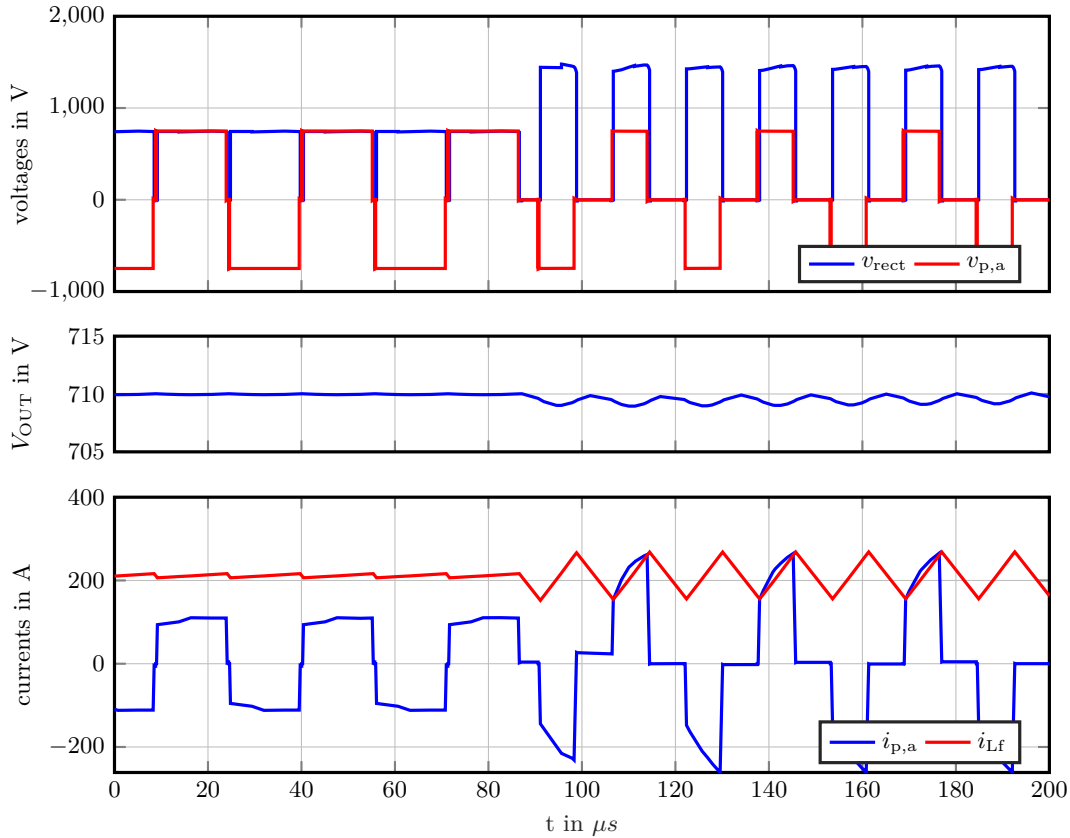


Figure 6.13 – Simulated waveforms at the transition from parallel to series configuration at $t = 90 \mu s$ with $V_{IN} = 750 \text{ V}$, $V_{OUT} = 710 \text{ V}$, and $P_{OUT} = 150 \text{ kW}$. Top: primary-side transformer voltage and rectified voltage. Middle: output voltage. Bottom: primary-side current and output inductor current

at $t = 90 \mu s$ during the freewheeling phase of the rectifier resulting in a zero voltage switch off for the switches $T_{9,a}$ and $T_{10,b}$ and also in a zero voltage switch on of $T_{10,a}$ and $T_{9,b}$. From the primary-side transformer voltage/current waveforms can be seen that the phase-shift has to be halved to reach the same output voltage. This has to be ensured by the modulator so that the transition can be realized in a smooth way. Since the delivered output power before and after the transition remains the same the current-time area of i_p must be equal (assuming ideal current shaping), which results in a higher amplitude for the series configuration. At this point (after the transition), the current shaping shows a high impact since the freewheeling phase is longer than in any other operating point for the series configuration.

6.4.3 Efficiency and comparison to mechanical changeover switches

With the electrical and thermal simulation the efficiency of the converter at different operating points can be determined. The efficiency of the converter with solid-state changeover switches is also compared to a converter with mechanical changeover switches (relays). The converter has been simulated in three different configurations of the changeover switches:

- either inner or outer switches always on (standard)
- advanced control strategy for the outer switches (advanced)
- mechanical switches instead of MOSFETs (mechanical)

For the mechanical switches relays with a contact resistance of $1\text{m}\Omega$ (assumed for this power class) have been considered and simulated as shown in fig. 6.2. Figure 6.14 shows the efficiency of the converter in dependency of the output voltage at full output power. The transition point voltage $V_{\text{tr,p/s}}$ lays at 710 V . Since the output current is the same before and after the transition, the efficiency drops because the same current is carried by series-connected switches instead of parallel switches. For the series configuration, the advanced control strategy results in a higher efficiency than for the converter with mechanical switches, even though the on-state resistance of the relay is significantly lower than the $R_{\text{DS,on}}$ of the SiC MOSFETs ($1\text{m}\Omega$ vs. $6\text{m}\Omega$ MOSFETs). Since the advanced control strategy is not applicable for the parallel configuration, the mechanical switch converter shows a higher efficiency at the lower output voltages.

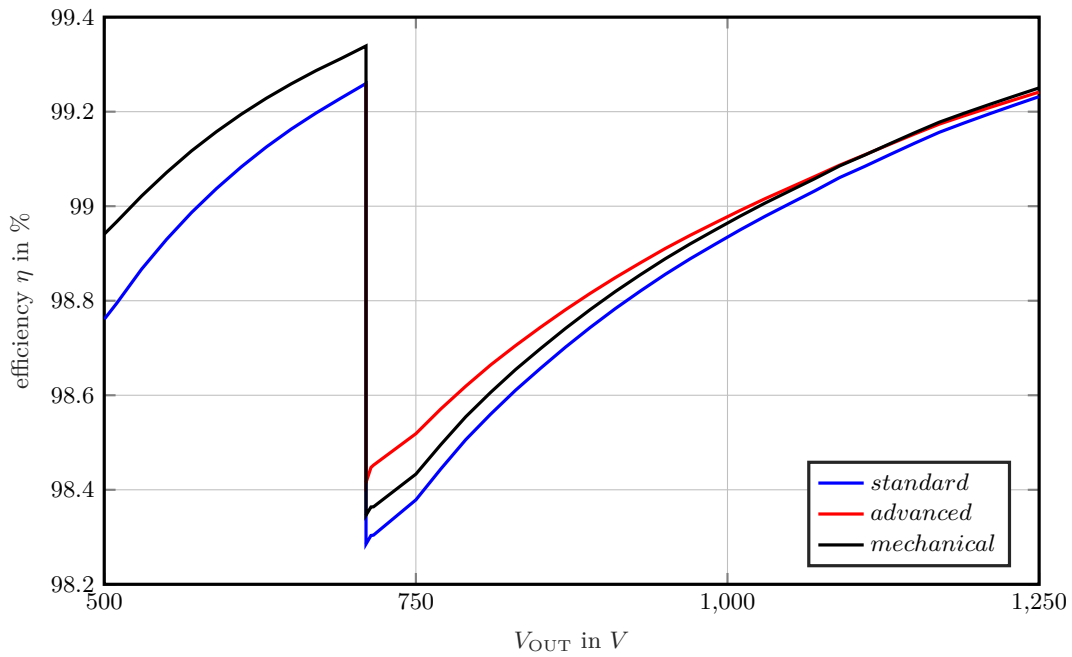


Figure 6.14 – Simulated efficiency in dependency of the output voltage at constant output power.
standard: outer changeover switches $T_{9,a}$ and $T_{10,b}$ are on for the parallel configuration and inner switches $T_{10,a}$ and $T_{9,b}$ for the series configuration.
advanced: advanced control method for the outer changeover switches $T_{9,a}$ and $T_{10,b}$.
mechanical: mechanical changeover switches (relays).

6.4.4 Loss distribution of the semiconductors

The switches, the transformers and the inductor are considered in the simulation for the losses in the converter. The losses in the capacitors are neglected, as it is seen in 5.5 that these losses are relatively small compared to the other losses. The losses of the MOSFETs from the different functional blocks primary side, rectifier, changeover switches and clamping switches are summed. Fig. 6.15 shows the distribution of the simulated losses in the semiconductors and the passives in dependency of the output voltage with current shaping and the advanced control method for the changeover switches in series configuration.

For the primary-side switches, the conduction losses dominate because all switches turn on at zero voltage (at full output power). Due to the nearly ideal current shaping, the switches $T_{1,a/b}$ and $T_{2,a/b}$ turn off at almost zero current, leaving the turn-off losses of $T_{3,a/b}$ and $T_{4,a/b}$ as practically the only contributors to the switching losses on the primary side (totaling less than a third of the losses of these switches for the full output voltage range). There are no switching losses for the rectifier switches $T_{5-8,a/b}$. Therefore, the losses are directly related to the output current, which is highest at the lower voltages of the series configuration. In parallel configuration, losses occur only in $T_{9,a}$ and $T_{10,b}$ of the changeover switches, which are conduction losses and are also directly related to the output current. In series configuration, conduction losses occur for all changeover switches when the advanced control strategy is used. The inner switches $T_{10,a}$ and $T_{9,b}$ are the main contributors to the losses of the changeover switches in series configuration. With increasing output voltage the share of the losses in $T_{9,a}$ and $T_{10,b}$ decreases as the freewheeling phase becomes shorter. The turn-off losses dominate the total losses of the clamping switches $T_{\text{Clamp},a/b}$ because the high current pulse required to bring $i_{p,a/b}$ to zero, is turned off. Because of the higher peak current of the primary side the clamping losses are higher when the converter operates in series configuration. In the inductor, the winding losses dominate, which is why the losses are higher at lower output voltages, due to the higher output current. For the transformer, the behavior of the losses for different output voltages is the same as for the PSFB converter: the core losses increase with increasing phase shift, and the winding losses increase with increasing output current of the submodule.

6.4.5 Comparison to the design results of chapter 5

Comparing the proposed converter with the results of chapter 5, it can be seen that the losses in the components and therefore the efficiency are similar to those of the PSFB converter. However, a direct comparison of the PSFB converter designs of configuration **A** with the simulation results of the proposed converter is difficult, as there are several differences. For a simpler design, the transformer turns ratio here is chosen to be $n = 1$. This requires the transition voltage $V_{\text{tr},p/s}$ to be lower than the input voltage V_{IN} and therefore a higher maximum output current must be provided (see section 4.1), resulting in a lower efficiency for the lower voltages in series configuration. The simulation of the proposed topology uses different MOSFETs (FF6MR12W2M1) compared to configuration **A** in chapter 5 (FF4MR12W2M1H). The reason is that for the hardware prototype presented below, only the FF6MR12W2M1 module was available at the time of realization. Other aspects are, that the losses of the relays for parallel/series configuration are not considered in chapter 5 and

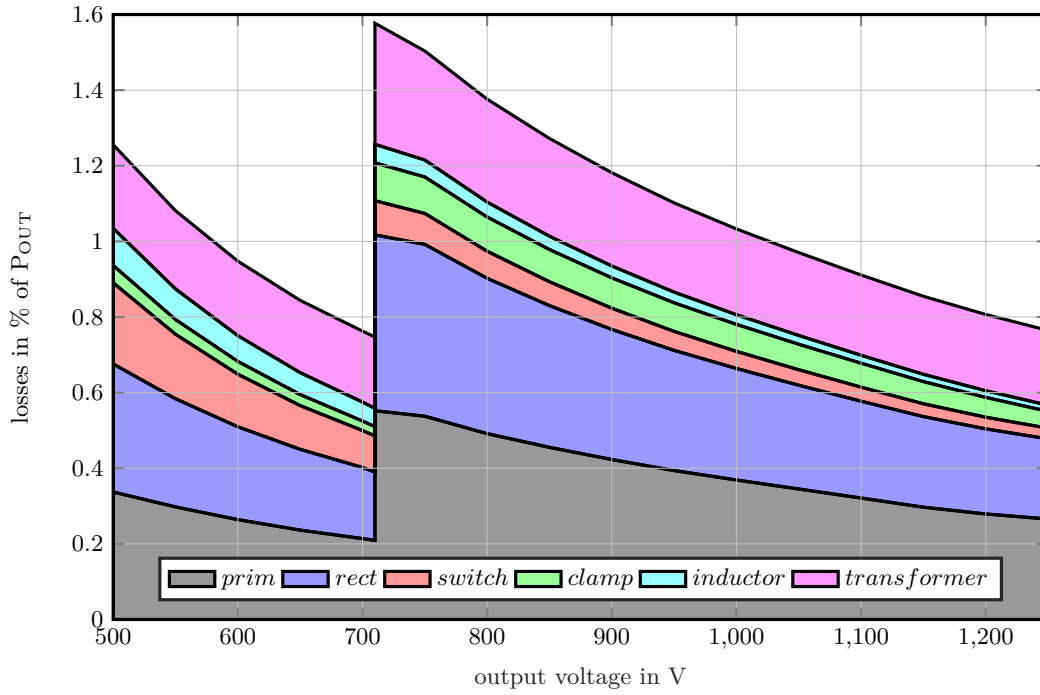


Figure 6.15 – Simulated loss distribution in dependency of the output voltage at constant output power for the proposed topology with current shaping and the advanced control method. *prim*: primary side, *rect*: rectifier, *switch*: changeover switches, *clamp*: clamping switches, *inductor*: output inductor core and winding losses, *transformer*: combined core and winding losses of both transformers

the loss reduction in the primary-side switches using current shaping is not considered, and the mechanical switches cannot be used to increase the efficiency in series configuration.

In summary, the cost of the proposed converter is higher than the conventional PSFB converter due to the additional semiconductor devices. This higher cost is justified by the higher output voltage flexibility. If the proposed converter is designed exactly like the PSFB converters in chapter 5, the efficiency is lower to equal (depending on the relays) in parallel configuration and higher in series configuration.

6.5 Experimental validation

A hardware demonstrator is realized to demonstrate the basic function of the DC-DC converter with a solid-state changeover switch. This section discusses the design of the passive components, using the values from the simulation in the previous section and the realization of the prototype. Finally, the measurement results obtained are presented.

6.5.1 Hardware prototype

Figure 6.16 shows a rendered image of the complete prototype, showing its overall design and assembly. The various functional components of the prototype are labeled.

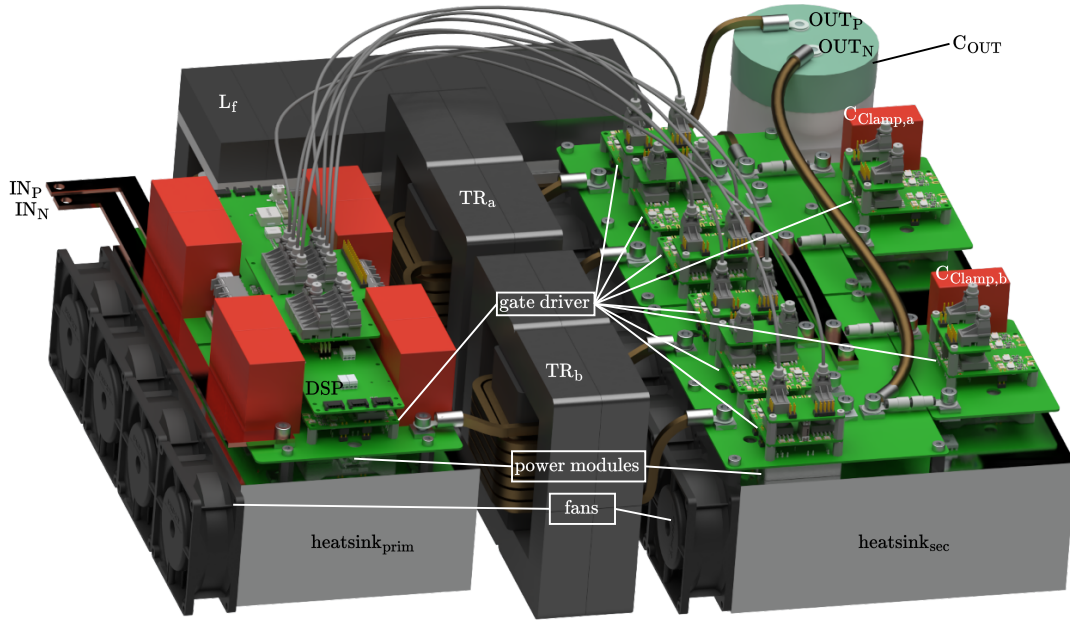


Figure 6.16 – Rendered image of the 3D model of the hardware prototype with labeled functional components

Table 6.2 – Components used for the hardware prototype

Parameter	Value
SiC MOSFETs	FF6MR12W2M1
$Tr_{a/b}$	8xU93 (N87, in E configuration), $n = 6 : 6$
L_f	$50 \mu\text{H}$, 9xU93+I93 (N87), $n = 7$
$L_{r,a}$	$1.8 \mu\text{H}$ (integrated in Tr_a)
$L_{r,b}$	$1.6 \mu\text{H}$ (integrated in Tr_b)
C_{OUT}	$240 \mu\text{F}$, 1300 V
C_{Clamp}	$3 \mu\text{F}$, 1600 V
f_{sw}	32 kHz

Power semiconductors

As in the simulation, SiC MOSFETs with a $R_{DS,on} = 6 \text{ m}\Omega$ and a blocking voltage of 1200 V are used for the power semiconductors. Infineon’s FF6MR12W2M1 half-bridge power module is chosen for this purpose (a picture of the power module can be seen in 6.19b).

Design of the passive components

For the passive components, the same values as for the simulation are used. The system variables (voltages and currents) needed to design the components are also exported from the simulation. The design of the transformer is done for the two most critical operating points at full output power for $V_{OUT} = V_{tr,p/s}$, both in parallel (resulting in highest core losses) and in series configuration (highest current and therefore winding losses). The transformer design routine from 5.2 is employed for this purpose. From the set of valid solutions one design is

selected. It represents a double stacked EE core transformer, where each E core is realized with two U93 cores, thus using eight identical U93 (N87) cores. Each winding (primary and secondary) consists of six turns of two litz wires connected in parallel. This design is chosen not only because of the lowest price, but also because of the availability of cores and litz wire. The parameters of the transformers $Tr_{a/b}$ are measured using a network analyzer (Keysight E5061B). The results of the open-loop measurement of impedance, phase, and inductance are shown in fig. 6.17. The magnetizing inductance at the switching frequency $f_{sw} = 32 \text{ kHz}$ is $L_m = 320 \mu\text{H}$. To estimate the parasitic winding capacitance, the Self Resonant Frequency (SRF) is determined from the graph to be $SRF = 440 \text{ kHz}$. With [106]

$$C_T = \frac{1}{L_m \cdot (2\pi SRF)^2}, \quad (6.17)$$

the effective winding capacitance is determined to be $C_T = 0.4 \text{ nF}$. The stray inductance is obtained by measuring the inductance of the primary winding when the secondary winding is shorted. This gives moderately different inductances $L_{r,a} = 1.8 \mu\text{H}$ and $L_{r,b} = 1.6 \mu\text{H}$ for the transformers $Tr_{a/b}$. The difference is explained by the different isolation of the two wires used, which results in a different distance from primary to secondary. How this affects the function will be analyzed below.

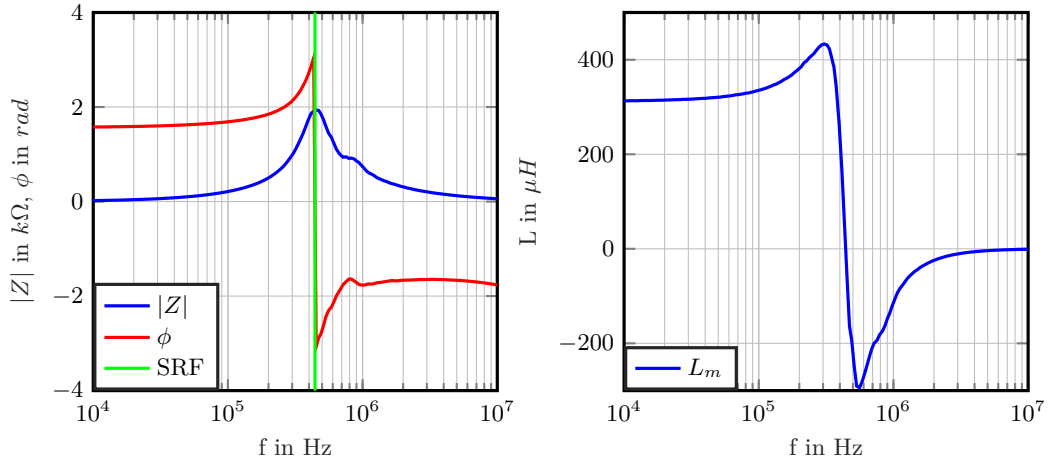


Figure 6.17 – Open-loop measurement of the realized transformer. Left: impedance and phase with highlighted Self Resonant Frequency SRF. Right: inductance in dependency of the frequency

There are also two operating points to consider when designing the inductor L_f . These are the maximum output current in both, parallel and series configuration. Since the operating point at maximum output current in the parallel configuration is worse for the inductor (the winding losses are higher than the core losses due to the high DC portion of the inductor current), the design is done at this operating point using the inductor design routine. This results in a design with nine stacked U93+I93 (N87) cores with a winding consisting of seven turns of litz wire. Again, for reasons of availability, the number of strands of the realized inductor is less than the calculated ($5000 \times 0.1 \text{ mm}$ instead of $8000 \times 0.1 \text{ mm}$), so the winding losses could be further reduced by using a more suitable wire. The inductor must not saturate during operation. Therefore, an inductance vs. current measurement is performed with a power choke tester (ed-k DPG10-2000B). Figure 6.18 shows the measurement results at room temperature. According to the simulation the maximum current is 325 A (DC + ripple). Since

the maximum flux density decreases with increasing temperature, a margin must be kept. According to the N87 material datasheet, the inductance would drop less than 10 % for the maximum current at a core temperature of 100 °C, meaning the inductor will not saturate at that high temperature.

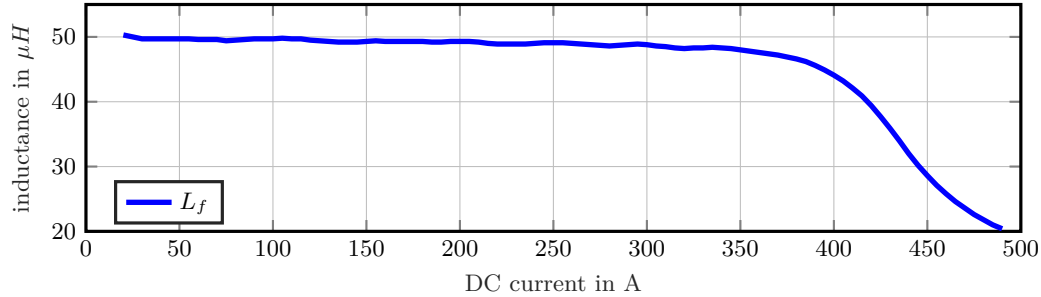


Figure 6.18 – Measured inductance of the realized inductor L_f versus DC current at room temperature.

Two different types of heatsinks are used for the prototype. For the primary side, two identical custom vapor chamber heatsinks (from Cooler Master) with a $R_{th} = 0.1 \text{ K/W}$ are used, one for each full bridge. A single high performance heatsink (fischer elektronik SK 441) with a cooling performance of $R_{th} = 0.033 \text{ K/W}$ is used for the secondary side. All active secondary-side components on the (rectifier, changeover and clamping switches) are thermally connected to this heatsink.

Gate driver, DSP and control

Each power MOSFET in the circuit must be driven from a single potential. Therefore an isolated driver is required. Since the power module has a half bridge topology, two drivers are required per module. Therefore, the gate driver board includes two isolated outputs. The power supply for the output stage is realized with a full-bridge isolation stage and two buck converters for the positive and negative gate voltages of 18 V and -3 V , respectively. The gate is driven by an integrated and isolated drive circuit with different gate resistances for turn on and turn off. The models of the gate driver board, as well as of the power module are shown in fig. 6.19.

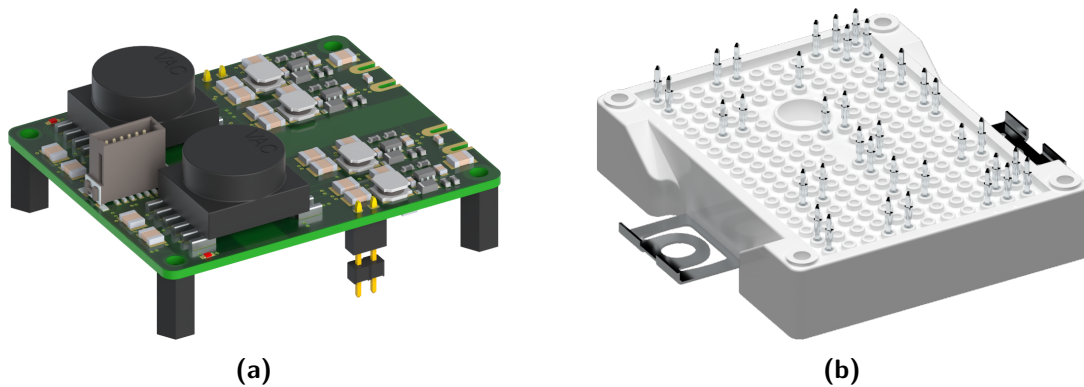


Figure 6.19 – a) gate driver board with two isolated outputs to drive one half-bridge power module. b) 6 m Ω , 1200 V SiC MOSFET half-bridge power module (Infineon)

A separate board is designed to control the DC-DC converter. It contains a microcontroller unit (MCU) and a field-programmable gate array (FPGA), as well as analog circuitry and auxiliary supplies for the low voltages (3.3 V and 5 V). The converter is controlled by the MCU, while the FPGA is used to generate the gate signals. The MCU used is the STM32G484 from STMicroelectronics, for the FPGA the device LCMXO2-4000HC from Lattice is used. Attached to the control board, a daughter board with signal to fiber optic transmitters is used to control the MOSFETs on the secondary side. A picture of this stack-up is shown in fig. 6.20.

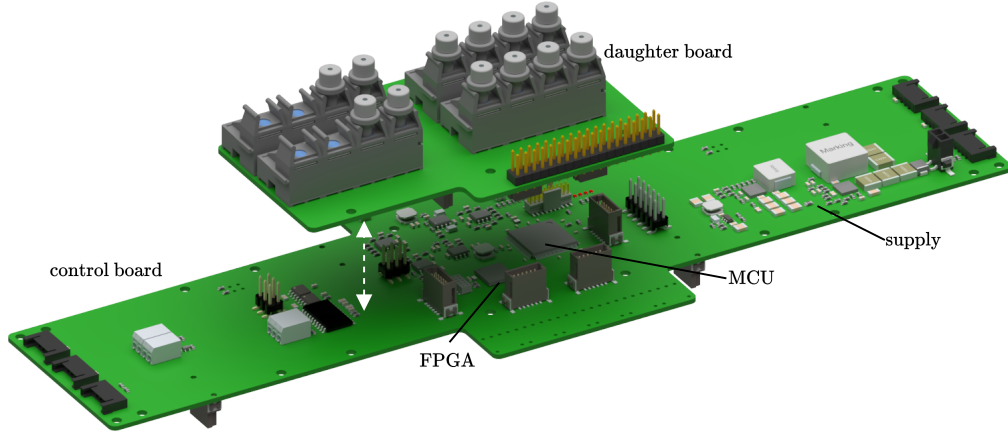


Figure 6.20 – Primary-side control board with corresponding daughter board for controlling the secondary-side semiconductors via fiber-optic signals. The board includes a low-voltage supply for the various auxiliary voltages, analog circuitry, and a microcontroller and FPGA combination for the DSP and control of the DC-DC converter.

For the overcurrent protection on the primary side, an AC current sensor is implemented on the primary side of the two transformers. The current sensor is realized with a PCB based Rogowski coil. The PCB is shaped to fit on the connector of the primary-side power board. To minimize noise, the coils on the PCB are designed bifilar (interleaved forward and return winding) [107]. The coil signal is then integrated and low pass filtered on the control board as in [108]. Fig. 6.21a shows an image of the PCB Rogowski current sensor, while 6.21b shows the measured current, sampled by the MCU.

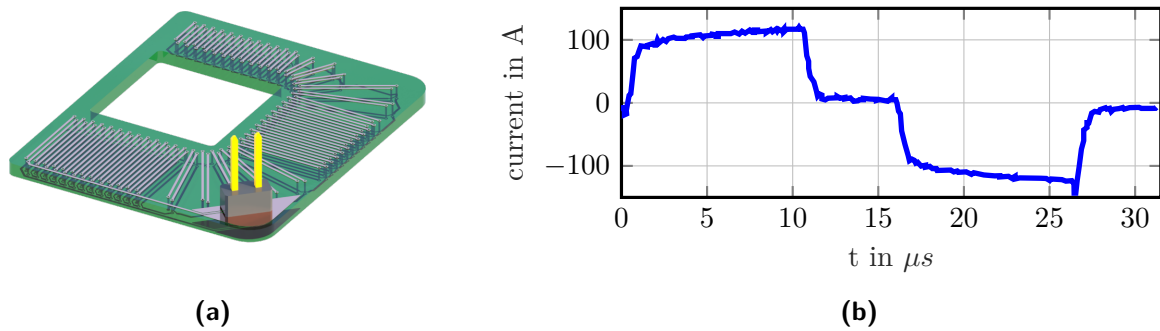


Figure 6.21 – PCB-based Rogowski current sensor for measuring the primary-side currents. a) transparently displayed PCB with interleaved forward and return winding, shaped to fit on the connector of the power board. b) integrated and conditioned coil signal sampled by the MCU, representing the measured current $i_{p,a/b}$.

Full prototype

Fig. 6.22 shows a photograph of the hardware prototype of the proposed DC-DC converter. On the left the primary side (1) can be seen. It consists of two identical power blocks, each

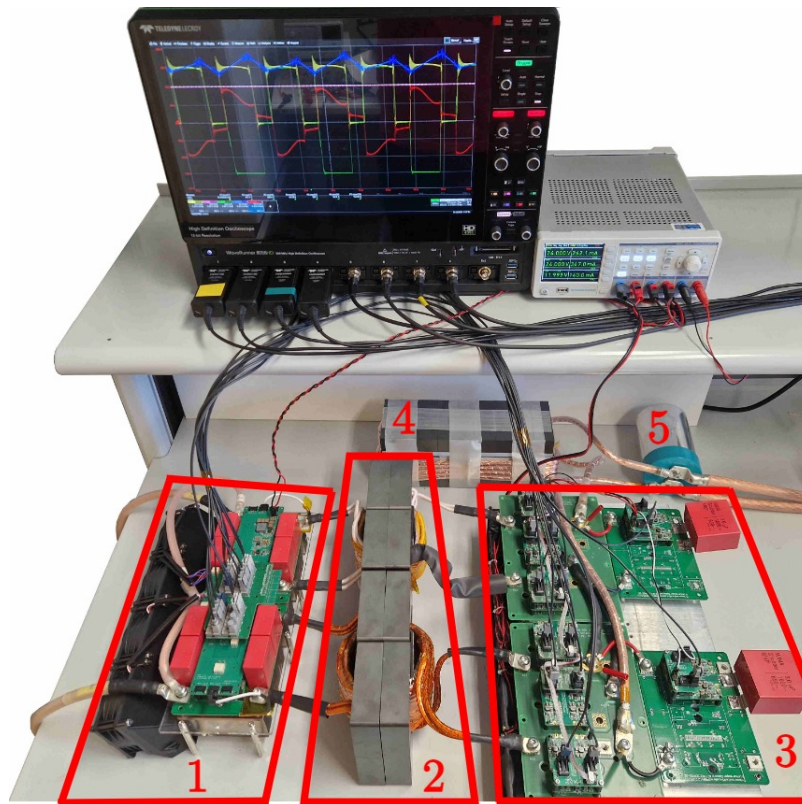


Figure 6.22 – Hardware prototype to validate the simulation results with: 1. primary side, 2. transformers, 3. secondary side, 4. output inductor and 5. output capacitor

of which comprising two half-bridge SiC-MOSFET modules and DC-link capacitors. The gate-drivers are mounted directly on the power boards and controlled by the DSP board, which is located above the drivers and connects the two primary-side power blocks. The two full bridges are connected in parallel. The secondary-side switches are controlled by the same DSP board as well via fibre optic cables. The two transformers (2), each of which consisting of eight U93 ferrite cores and six turns (for the primary and secondary side respectively) have been implemented with two different types of litz wire.

The secondary side is assembled of four boards mounted on a common heat sink (3). The two main boards on the left side of (3) contain three half-bridge modules each, two for the active rectification and one for the parallel/series changeover switches. The two active clamping boards on the right side of (3) consist of a power MOSFET and the clamp capacitor, each. For every half-bridge module a gate driver board (identical to the primary side) is used, driven by optical to electrical signal adapters.

The output inductor (4) has been implemented using nine U93+I93 ferrite cores and a litz wire winding. The output capacitor (5) is realized with a screw mounted film capacitor. For the control loop, input and output voltage and current are measured by the DSP board.

6.5.2 Experimental results

For testing, the prototype is powered by a laboratory power supply and operated back-to-back with another DC-DC converter. Therefore, the power supply is only required to deliver a power equal to the losses of the two converters instead of the full power. In fig. 6.23 the test setup is shown. Tab. 6.3 shows the equipment used for the test setup.

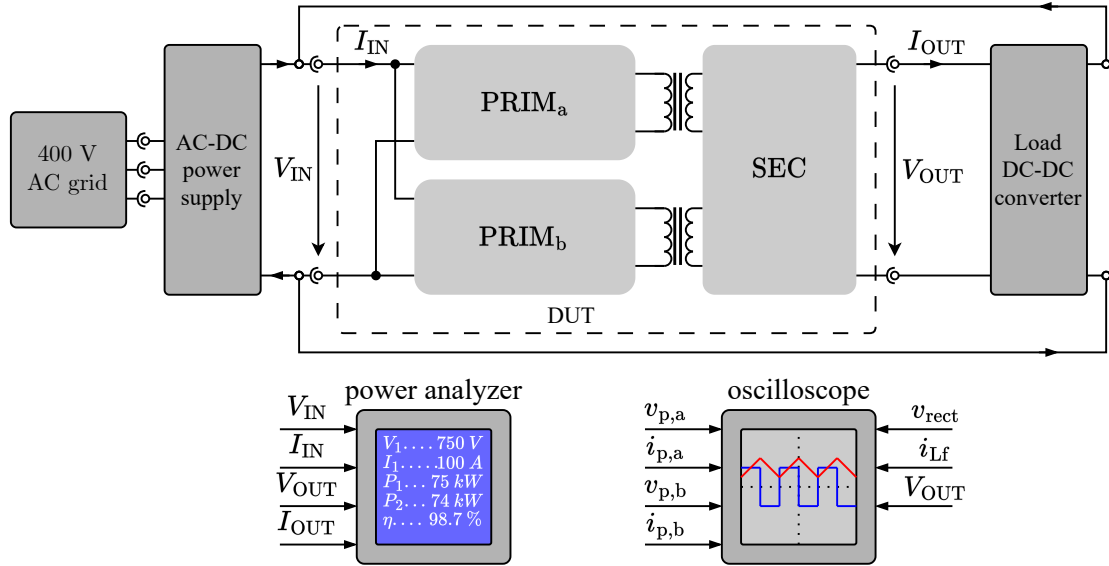


Figure 6.23 – Test setup with the hardware prototype as device under test (DUT)

Table 6.3 – Equipment used for the test setup

Parameter	Value
Power supply	Delta Elektronika SM1500-CP-30
Load	DC-DC converter
Power analyzer	Yokogawa PX8000
Voltage probes	Teledyne LeCroy HVD3206A
Current probes	PEM CWTMini50HF/1
Oscilloscope	Teledyne LeCroy WaveRunner 8058HD

Transition from parallel to series configuration

The first test is to measure the transition from parallel to series configuration. With an input voltage of $V_{IN} = 750$ V, the output voltage is set to $V_{OUT} = V_{tr,p/s} = 700$ V, the converter operates in constant voltage mode. With the load a constant current of $I_{OUT} = 110$ A is settled, resulting in an output power of $P_{OUT} = 77$ kW. The converter is in parallel configuration with the switches $T_{9,a}$ and $T_{10,b}$ on (and $T_{10,a}$ and $T_{9,b}$ off). At the transition $T_{9,a}$ and $T_{10,b}$ are turned off during the freewheeling phase and simultaneously $T_{10,a}$ and $T_{9,b}$ are turned on. To keep the output voltage constant, the phase shift ps is halved. Fig. 6.24 shows the measured waveforms of the primary-side voltage, the rectified voltage, the output voltage, the two primary-side currents, as well as the inductor current at the transition from parallel

to series configuration. After the transition the rectified voltage v_{rect} doubles, leading to a higher ripple in the output inductor current i_{L_f} . It can be seen that the output voltage remains constant during the transition resulting in a continuous energy transfer. Table 6.4 shows the parameters for the operating point used for the measurements in figure 6.24.

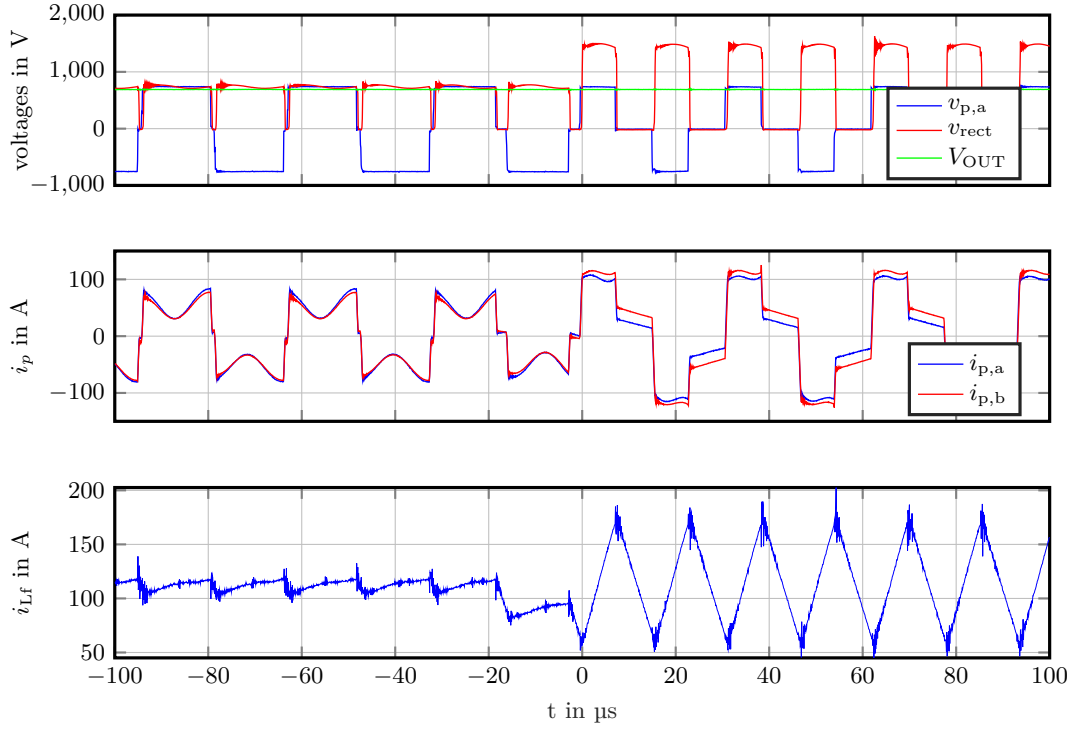


Figure 6.24 – Measured waveforms at the transition from parallel to series configuration: primary-side transformer voltage, rectified voltage, output voltage and primary-side and inductor current at the operating point $V_{\text{IN}} = 750\text{ V}$, $V_{\text{OUT}} = V_{\text{tr,p/s}} = 700\text{ V}$ and $I_{\text{OUT}} = 110\text{ A}$.

Table 6.4 – Operating point used for the measurements in figure 6.24

Parameter	Value
f_{sw}	32 kHz
V_{IN}	750 V
V_{OUT}	700 V
I_{OUT}	110 A
P_{OUT}	77 kW

Continuous operation

Fig. 6.25 shows the waveforms of the voltages $v_{p,a}$, v_{rect} , and V_{OUT} and the currents i_{L_f} and $i_{p,a}$ for the converter operating in parallel configuration at $V_{\text{IN}} = 750\text{ V}$, $V_{\text{OUT}} = 500\text{ V}$, $I_{\text{OUT}} = 150\text{ A}$ and $P_{\text{OUT}} = 75\text{ kW}$. The parameters are shown in tab. 6.5. Comparing this plot with the simulation, several differences, caused by the parasitic elements of the components, can be observed. These differences will be analyzed below.

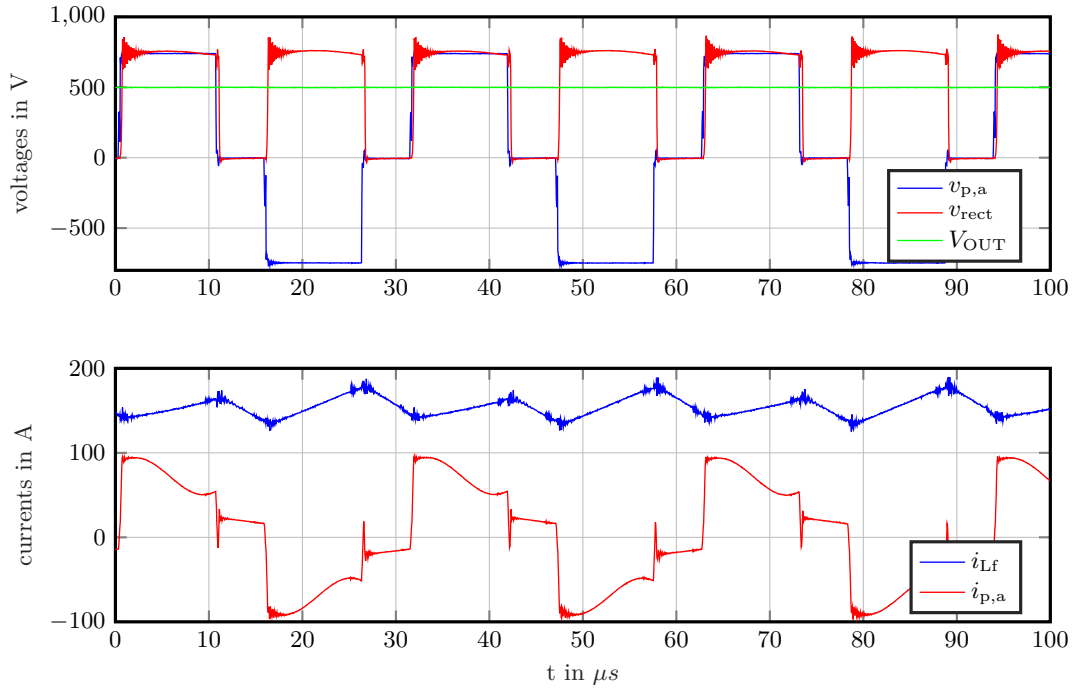


Figure 6.25 – Measured waveforms of the voltages $v_{p,a}$, v_{rect} , and V_{OUT} (top) and the currents i_{Lf} and $i_{p,a}$ (bottom) in parallel configuration during continuous operation at the operating point specified in tab. 6.5

Table 6.5 – Operating point used for the measurements in figure 6.25

Parameter	Value
f_{sw}	32 kHz
V_{IN}	750 V
V_{OUT}	500 V
I_{OUT}	150 A
P_{OUT}	75 kW

Ringing on the rectified voltage

With a closer look at the upper plot in fig. 6.25, a ringing can be observed on the rectified voltage v_{rect} , following the rising edge. To find the cause of this oscillation, the circuit is analyzed in more detail. Since this ringing is not present in the simulation with ideal components, the parasitic elements of the components must also be considered. The first step is to examine the current flow path of the circuit in parallel configuration and during energy transfer (when the ringing occurs). Fig. 6.26 shows this current flow path. The primary-side full bridges are ignored and a voltage step with a defined slope is applied. The transformers $Tr_{a/b}$ are modeled with $L_{r,a/b}$ and the parasitic winding capacitance C_T (since the turns ratio is $n = 1$, the primary-side impedances can be directly reflected to the secondary side). For the rectifier, the conducting switches $T_{5,a/b}$ and $T_{8,a/b}$ are replaced by their on-state resistance R_{ON} , the switches in the off state $T_{6,a/b}$ and $T_{7,a/b}$ by their parasitic output capacitance C_{OSS} . The same applies to the changeover switches $T_{9,a/b}$ and $T_{10,a/b}$. The clamping switches $T_{Clamp,a/b}$ are conducting (first through the body diode and after the blanking time also

through the channel) and are replaced by the parasitic inductance to the clamping circuit while neglecting the on-state resistance.

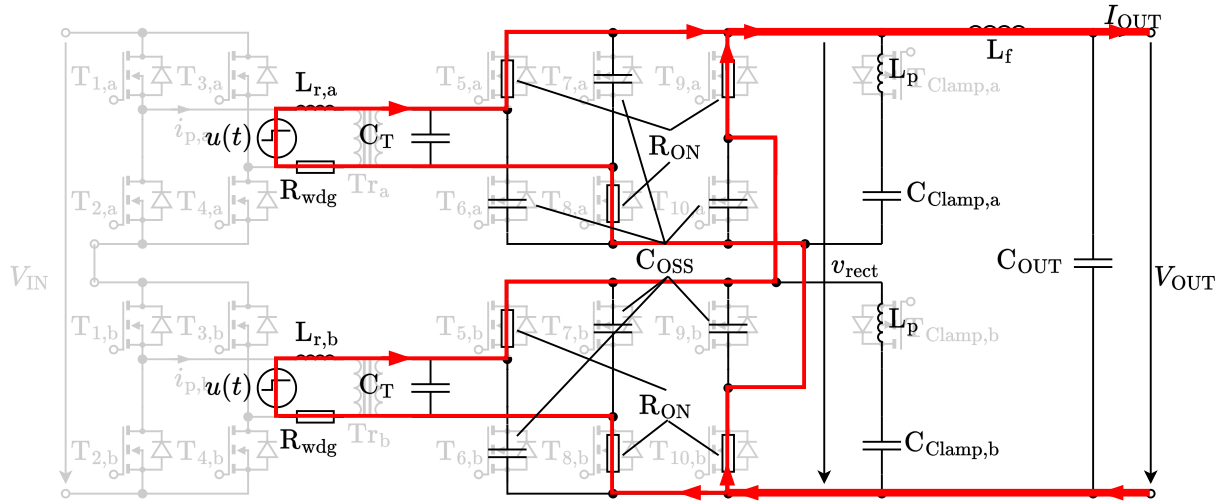


Figure 6.26 – Current flow path in parallel configuration during energy transfer with parasitic elements. Switches in on state are modeled as resistor R_{ON} , switches in off state as capacitor C_{OSS} . The parasitic inductance between rectifier and clamping circuit is modeled as L_p

The equivalent circuit for the converter in parallel configuration and during energy transfer is shown in fig. 6.27a. For the small-signal model, the DC voltages are considered to be zero, so the capacitors C_{OUT} and C_{Clamp} are replaced by a short circuit.

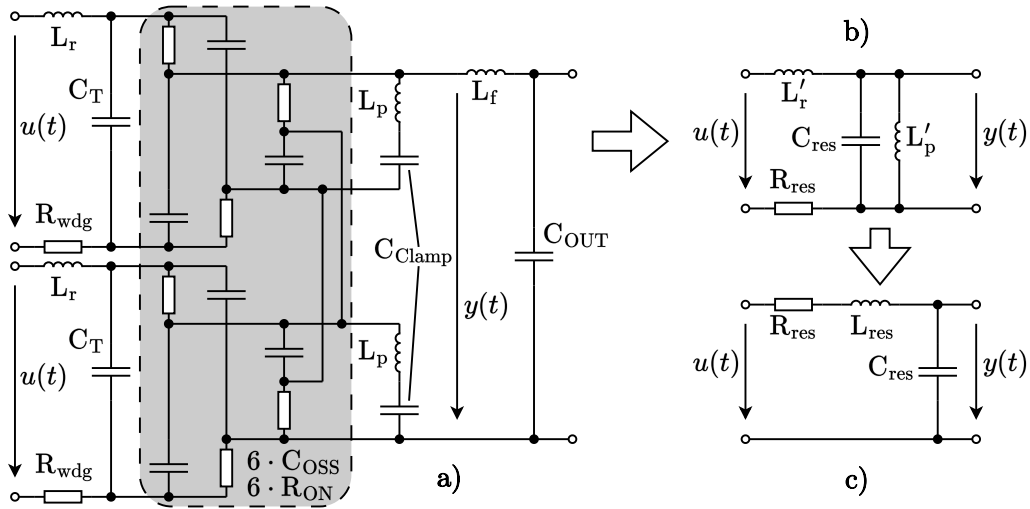


Figure 6.27 – Equivalent circuit for the the converter in parallel configuration and energy transfer (a). The circuit can be redrawn as a small-signal model (b) if only the AC behavior is considered and simplified to an RLC circuit (c).

Neglecting the on-state resistance R_{ON} of the switches for simplicity (as in [109, chapter 4]), the remaining capacitors can be summarized to $C_{res} = 2 \cdot C_T + 6 \cdot C_{OSS}$. Since $L_f \gg L_p$,

the remaining parasitic inductance can be assumed to be $L'_p = L_p/2$, while the inductance of the stray inductors is connected in parallel resulting in $L'_r = L_{r,a} || L_{r,b}$. Fig. 6.27b shows this simplified circuit. The circuit can be further simplified by modeling it as an RLC circuit (6.27c) with $L_{\text{res}} = L'_r || L'_p$. With the determined variables the resonant frequency

$$\omega_0 = \frac{1}{\sqrt{L_{\text{res}} \cdot C_{\text{res}}}} \quad (6.18)$$

of this RLC circuit can be determined. The damping coefficient

$$\alpha = \frac{R_{\text{res}}}{2L_{\text{res}}} \quad (6.19)$$

determines how fast the ringing subsides. The resulting ringing model can be described by the simplified equation for the series resonant circuit [110, Chapter 6]

$$y(t) = Ae^{-\alpha t} \cos(\omega t + \varphi) + nV_{\text{IN}}, \quad (6.20)$$

with $\omega = \sqrt{\omega_0^2 - \alpha^2}$ and $\varphi = -\pi/2$. The coefficient A can be read out from the measured waveform and depends on the slope ($\frac{dV}{dt}$) of the step $u(t)$ applied to the model. Fig. 6.28 shows the step $u(t)$, the rectified voltage v_{rect} , and the output of the small-signal model $y(t)$. It can be seen that the simple model describes the ringing very accurately.

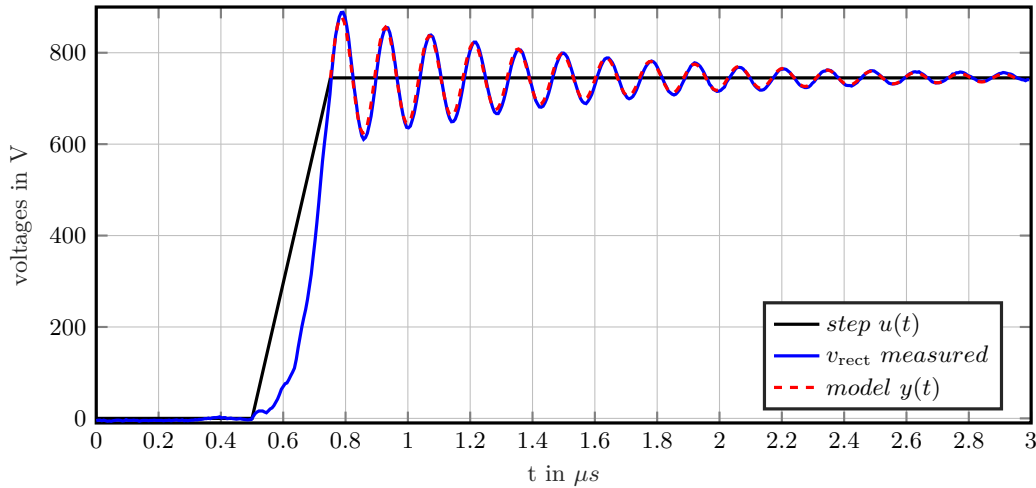


Figure 6.28 – Ringing of the rectified voltage v_{rect} at the beginning of the energy transfer phase. The measured voltage, as well as the input and output of the small-signal model can be seen, proving that this ringing is caused by the parasitic elements such as MOSFET and transformer capacitance and parasitic inductance of the setup.

Since the peak voltage of v_{rect} is well below the blocking voltage of the semiconductors, the clamping circuit serves its purpose. In order to further reduce the amplitude of the ringing, the parasitic inductance L_r can be reduced. This can be done by moving the clamping circuit physically closer to the rectifier switches, e.g. by placing them on the same PCB.

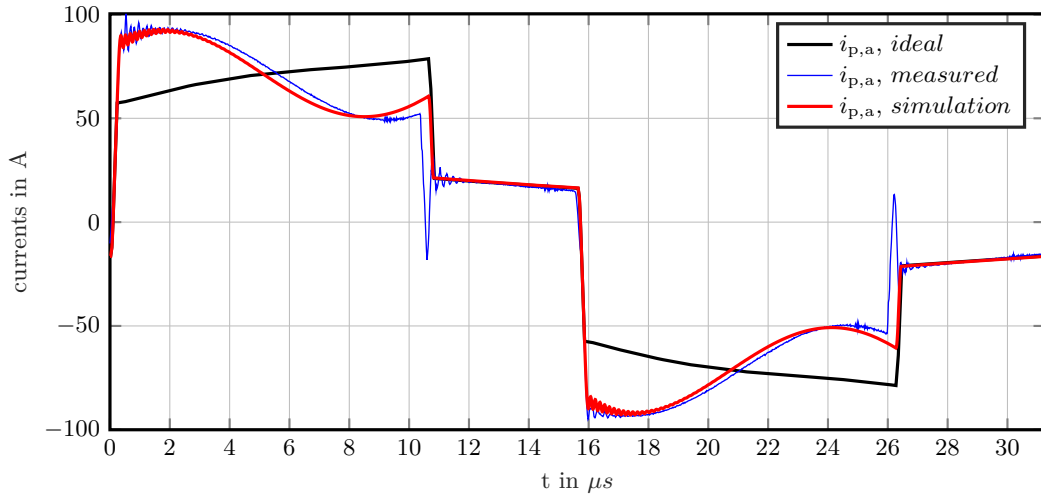
Tab. 6.6 shows the values used for the small-signal RLC circuit with the measured winding capacitance C_T and the value for C_{res} coming from the data sheet of the MOSFET.

Table 6.6 – Parasitic elements and resulting component values for the RLC circuit

Parameter	Value
C_T	0.4 nF
C_{OSS}	0.88 nF
C_{res}	6.08 nF
L_{res}	83 nH
R_{res}	220 m Ω
$\omega_0/2\pi$	7.06 MHz

Deviation of the primary-side current waveform from its ideal form

From the measurement results in the figures 6.24 and 6.25 it can be seen that the primary-side current differs from the simulated waveform of 6.13. In the simulation, $i_{p,a}$ shows a continuously increasing slope ($di/dt \approx (nV_{IN} - V_{OUT})/L_f$) during the energy transfer phase, while in the real converter an oscillation can be observed. This oscillation is also caused by the parasitic capacitors of the switches and the transformer. Together with the stray inductance $L_{r,a/b}$ of the transformers $Tr_{a/b}$, this leads to a voltage overshoot and is the reason for the necessary clamping circuit (as described in 4.2 and 6.2.3). The energy of this oscillation causes a voltage ripple across the clamping capacitor $C_{Clamp,a}$, as the capacitor is charged and discharged twice per switching period. Fig. 6.29 shows simulated ideal, measured real and simulated real (parasitics taken into account) waveforms of $i_{p,a}$ for the operating point of tab. 6.5.


Figure 6.29 – Simulated and measured primary-side current $i_{p,a}$ with and without the parasitics of the components

It can be seen that the current waveform from the simulation with the parasitics is very close to the measured one. Fig. 6.30 (top) shows the difference in the voltage ripple of $C_{Clamp,a}$ between the simulation with ideal components and the simulation with considered parasitics. While in the ideal simulation only the energy required for the current shaping charges and discharges the capacitor, in the simulation with parasitics the energy for the parasitics comes on top and causes a larger voltage ripple. Looking at the current through the clamping switch

$i_{T_{\text{clamp},a}}$, which charges and discharges $C_{\text{Clamp},a}$ (fig. 6.30 bottom), it can be seen that the oscillatory component of $i_{p,a}$ during the energy transfer phase is equal to $i_{T_{\text{clamp},a}}$ (except for the high-frequency ringing caused by the parasitic inductor L_p) and flows to the capacitor $C_{\text{Clamp},a}$. The spike in $i_{T_{\text{clamp},a}}$ at the transition from energy transfer to freewheeling phase comes from the current shaping.

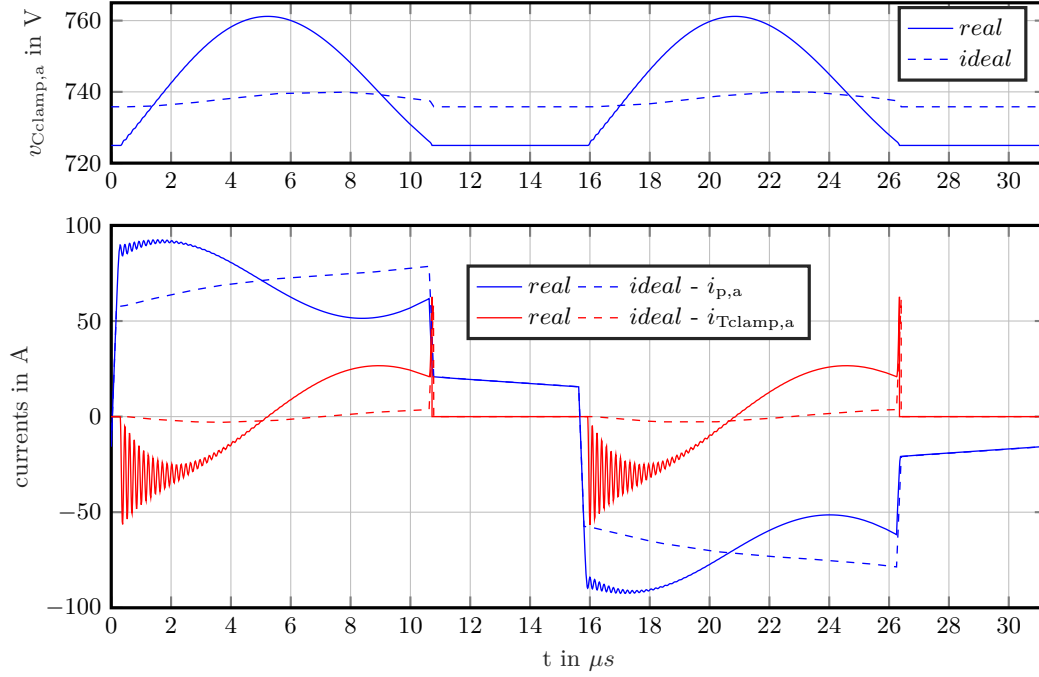


Figure 6.30 – Simulated waveforms of the clamping circuit with the voltage across the clamping capacitor $v_{C_{\text{clamp},a}}$ (top) and the primary-side current $i_{p,a}$ and the current through the clamping switch $i_{T_{\text{clamp},a}}$ (bottom) for the cases *real* (parasitic capacitors are considered) and *ideal* (parasitic capacitors are not considered)

Difference of the two primary-side currents

Since the stray inductances of the two transformers $\text{Tr}_{a/b}$ do not exactly match ($L_{r,a} = 1.8 \mu\text{H}$ and $L_{r,b} = 1.6 \mu\text{H}$), the primary-side currents are not perfectly balanced. This can be observed in figure 6.24, especially during the freewheeling phase when the currents differ due to the different energy levels stored in the stray inductance, as with $t_{\text{clamp},a} = t_{\text{clamp},b}$ a different residual freewheeling current is produced. To improve this, the stray inductances of the transformers should be better matched, or a different clamping time can be applied to the two clamping switches.

ZVS

The exact switching behavior of the MOSFETs can only be determined by measuring the voltage across and the current through the devices. In the setup, the current through the individual switches cannot be measured because the used half-bridge modules are pressed directly into the PCB. Therefore, the primary-side voltage and current are used to determine whether or not the switches switch at zero voltage. Fig. 6.31 shows one switching period of the primary-side voltage $v_{p,a}$ and current $i_{p,a}$ (a) and a closer look at the transition to the energy transfer phase (b) and the transition to the freewheeling phase (c).

In 6.31b it can be seen that after $T_{2,a}$ is turned off, the voltage starts to rise as the MOSFET output capacitors C_{OSS} are charged for $T_{2,a}$ and discharged for $T_{1,a}$ by the negative current $i_{p,a}$. After the current crosses zero, the voltage starts to decrease until $T_{1,a}$ is turned on at a primary-side voltage of about 150 V, which is about 600 V turn-on voltage for $T_{1,a}$. This means, that only an incomplete ZVS is achieved for $T_{1,a}$. By reducing the clamping time t_{clamp} a higher (in this case negative) freewheeling current remains and the circulating energy is sufficient to enable ZVS. According to equation 4.10, a primary-side current of at least 29 A (actual current is 15 A) would be required during freewheeling to achieve complete ZVS. However, this higher freewheeling current also leads to higher conduction losses. A compromise must be found to minimize the total losses.

In 6.31c the transition from energy transfer phase to the freewheeling phase is shown. After $T_{4,a}$ is turned off, the voltage drops immediately because the high current provides a fast charge/discharge of the MOSFET output capacitors. Then $T_{3,a}$ is turned on at almost zero voltage. For the negative half-wave, the switching behavior is similar for turning off of the high-side switches and turning on the low-side switches.

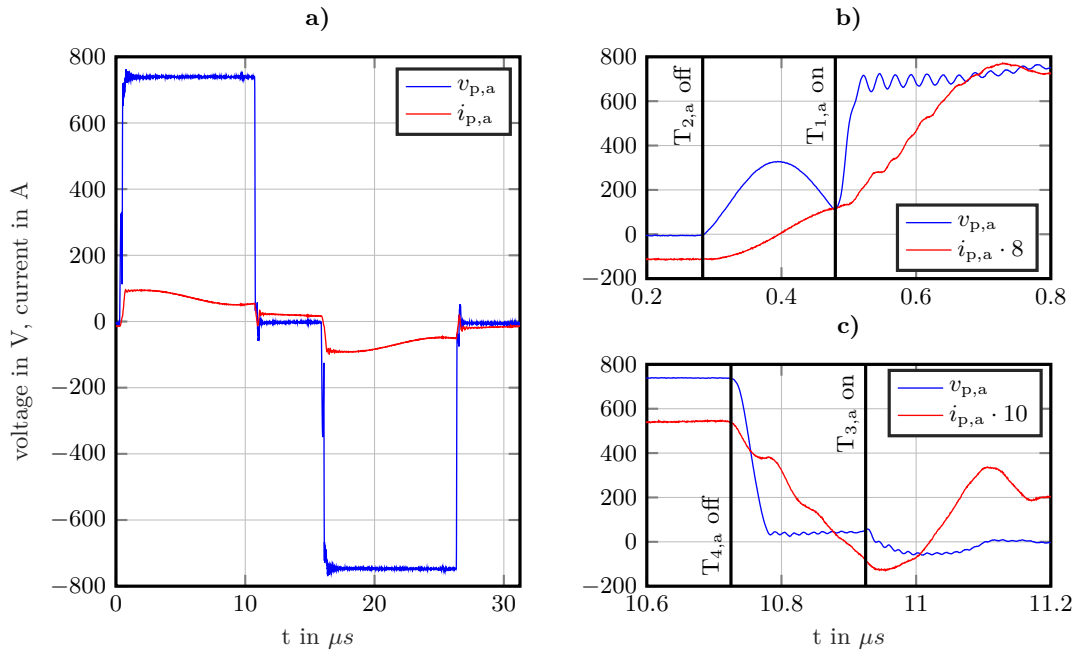


Figure 6.31 – Switching behavior of the primary side in operating point from tab. 6.5. One period of the primary-side voltage $v_{p,a}$ and current $i_{p,a}$ (a) and a closer look at the rising (b) and falling (c) edges of $v_{p,a}$.

Efficiency

An efficiency measurement of the entire converter is performed with a Yokogawa PX8000 power analyzer. The measured efficiency for the operating point from tab. 6.5, $V_{IN} = 750V$, $V_{OUT} = 500V$, $I_{OUT} = 150A$ and $P_{OUT} = 75kW$ is $\eta_{meas} = 98.3\%$. Comparing this measured value with the simulation at this operating point ($\eta_{sim} = 98.8\%$) shows that the measured losses are about 375 W higher than in the simulation. However, a direct comparison of the converter efficiency with the simulation is not very meaningful because the passives for the hardware prototypes are not designed for full power operation and therefore show higher losses. The largest deviation from the prototype to the simulation comes from the core losses of the transformer. The simulation assumes the same core configuration (8xU93 cores in E configuration), but with a higher number of turns of $n = 9 : 9$ (instead of $n = 6 : 6$). This results in about 150 W higher core losses for the two transformers in the prototype at this operating point. Also, the winding losses of the transformers and the inductor are higher than assumed in the simulation because fewer strands are used. Together they account for about 160 W to 180 W for the three components. The rest of the additional losses in the hardware prototype compared to the simulation are mostly due to the incomplete ZVS of the primary-side switches and not considered losses from the capacitors and resistive parts of the setup such as cables and connectors.

6.6 Conclusion and outlook

In this chapter, a DC-DC converter topology based on the PSFB converter and a switchable parallel/series configuration of the secondary side using semiconductor switches is proposed and analyzed by showing the current flow paths for the different configurations and phases of the switching periods. The active and passive components of the converter are dimensioned and the active clamping circuit is used to reduce the conduction losses of the primary-side switches by shaping the primary-side current. A simulation of the converter is performed to show the principle of operation and to calculate the losses of the active and passive components of the converter. It is shown that the proposed advanced modulation for the changeover switches can increase the overall efficiency in series configuration, even exceeding the efficiency of a system with a mechanical switch. A hardware prototype is realized and used to demonstrate the operating principle and the seamless transition from parallel to series configuration during power flow. Several aspects of the hardware prototype, such as oscillations in the measured values, differences to the simulation, ZVS and efficiency of the converter are analyzed and discussed.

With the suggested improvements in the converters design and control, the hardware prototype can be further optimized. Due to the modularity of isolated DC-DC converters, the proposed converter topology can be used in the high-power charging park for power conversion from the DC grid to the EV for the different power levels of MCS, HPC, and NCS.

7 Conclusion and outlook

As the electrification of road transport is essential to achieving net-zero CO₂ emissions, the supporting infrastructure must meet the growing demand for EV charging. A particular challenge lies in the power conversion process from the electrical grid to the EV, which must be not only highly efficient, but also cost effective and sustainable.

Therefore, the focus of this thesis was to develop and evaluate power electronic DC-DC converter concepts that meet these requirements. Using the standards of high power DC charging (chapter 2), a case study of a charging park in a highway service area in 2035 was considered (chapter 3). An analysis of the power distribution grid within the charging park was carried out, resulting in the recognition that the DC grid with a voltage of 1500 V is the most suitable distribution grid for this particular application. In contrast to today's chargers that use AC or long charging cables, this allows for a reduced cost of conductors and enables a more efficient power distribution within the charging park.

Following the introduction of isolated DC-DC converters and the different modular system configurations they allow (including a switchable secondary side configuration), four topologies suitable for this high power application were presented: PSFB converter, LLC converter, DAB and TSC (chapter 4). By studying the different operating principles, modulation schemes, and the system variables, the basis for an automated design process (chapter 5) was developed. In this design process, all the individual components of the converter, such as semiconductors, transformer, inductor, capacitors and cooling system, are dimensioned and designed to provide a complete DC-DC converter system design for each of the four different topologies.

Considering the scenario of the charging park a connection to the 1500 V DC grid and a charging voltage range of 500 V to 1250 V according to the MCS standard was assumed for the converters and the design routine was employed to generate a large number of valid DC-DC converter designs in different configurations. In a second step, a multi-objective optimization was used to identify the optimal designs, with the result that all four topologies represent a global optimum in terms of the considered parameters of efficiency and cost. A closer look at the performance and cost distribution was taken to point out the advantages and disadvantages of the different topologies. Depending on the voltage or load profile, additional measures can be taken into account to select the best design. For the latter, the PSFB converter was found to provide the best design in terms of life-cycle cost.

Given this best PSFB converter design, a new topology using two PSFB converter submodules and a solid-state changeover switch has been proposed and presented (chapter 6). It takes advantages of the switchable secondary side configuration and combines it with the fast switching capability of semiconductors to cover the full MCS voltage range without interrupting the power flow. This topology has been analyzed in detail and design rules for the components have been found. The operation was verified by the use of a simulation and an advanced modulation scheme of the solid-state switch was presented, which allows a higher

efficiency compared to a converter using mechanical switches. A hardware prototype was realized and tested to demonstrate the operation of the topology.

Outlook

The high simultaneous power demand for fast and MCS charging within a charging park requires a relatively high voltage of the distribution grid to enable high efficiencies and reduce the demand for conductor material. As the considerations in this thesis are only for the partially-electrified year 2035, the power levels will continue to increase in the years after, making even higher voltages useful. The modular DC-DC converters can be adapted to these higher voltage levels and the presented method of the automated design process combined with the multi-objective optimization can be used to find the best designs.

A Appendix

A.1 Partial discharge in DC-DC converter transformers

The transformer of the DC-DC converter must provide a reinforced isolation between the grid and the EV. Partial-discharge-free operation is required, challenging the insulation of the transformer. To verify the transformer, a partial discharge test is performed, by applying a voltage between the primary and secondary windings. Figure A.1 shows the applied voltage for the partial discharge test according to [111]. V_{pd} is the repetitive peak working voltage across the device. The voltage is ramped up from 0 to t_1 to $1.875 V_{pd}$ and held for a maximum of five seconds. From t_2 the voltage is reduced to $1.5 V_{pd}$ and held for ≤ 15 s. The partial discharge is measured between t_3 and t_4 , where the maximum allowed value is 10 pC.

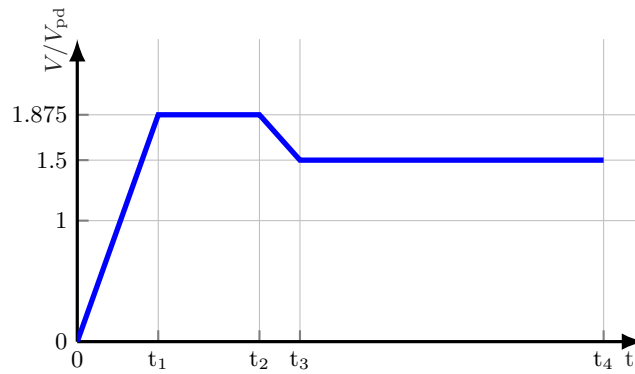


Figure A.1 – Voltage for the partial discharge test

As this applied voltage depends on the operating voltage of the converter system and thus on the voltage of the DC grid, the transformer design becomes more difficult as the voltage increases. The space for insulation in the transformer is limited because the winding window inside the core is mostly occupied by the windings. Increasing the insulation thickness is therefore not always possible and also increases the stray inductance, which is often undesirable (e.g. higher duty cycle loss for the PSFB converter) and can lead to higher winding losses. Partial discharge occurs, when the electric field exceeds the dielectric strength in parts of the insulation between the primary and secondary windings. Since this electric field can be inhomogeneous when different insulation materials are used, the effective dielectric strength is reduced. As the dielectric strength of most insulation materials is higher than that of air, the space between the two windings must be free of voids and bubbles [112]. In [113] the design of a DC-DC converter transformer with high isolation capability is shown, achieving partial-discharge-free voltages of about 30 kV by using potting material applied under vacuum to remove the air.

A.2 Design routine scripts

Table A.1 gives a detailed breakdown of the individual contributions to the design routine scripts used for the design and optimization of the DC-DC converters of chapter 5. The different design scripts are highlighted in three different colors, depending on whether they were created by me (author), by one or more of my colleagues, or in collaboration (team). For example, the universal semiconductor design scripts, such as the fundamental loss calculations and the database, were created by the team to ensure proper functioning for all the different topologies, not only for isolated DC-DC converters, but also for different other converters such as DC-AC or AC/DC.

Table A.1 – Breakdown of individual contributions on design scripts

Color scheme	author	team	colleagues
Semiconductors	database	losses	evaluation
Passives	DC link capacitors	resonant capacitors	cooling system
Magnetics	inductor	transformer	LLC transformer
PSFB converter	system variables	design	evaluation
LLC converter	system variables	design	evaluation
DAB	system variables	design	evaluation
TSC	system variables	design	evaluation

A.3 Calculation of the demand for copper

This section shows the calculation of the copper demand, required for the different distribution grids and voltages from chapter 3 with the intermediate results. The results are displayed in figure 3.6. Table A.2 shows the calculation of copper demand for Layout 1 in Scenario 1, while A.3 shows the calculation for Layout 2.

Table A.2 – Calculation of copper demand for Layout 1 in Scenario 1 for the different distribution grid types and voltages. The charging power P for each double charging point and the distance l to the substation, identical for the different grid types and voltages, are shown. For each grid type and each voltage level, the current (per phase), required cross-section, and copper demand between two charging points are shown. The figures given are for one lane and must be multiplied by the number of lanes (four for Scenario 1).

Grid type	Parameter	MCS										HPC										NCS									
		1800	1800	1800	1800	1800	700	700	700	700	400	200	200	200	200	200	200	200	200	200	200	200	200	200	200	200	200	200	200	200	200
AC 400 V	P in kW	20	30	40	9093	6495	5485	4474	3464	80	80	90	100	110	120	130	140	150	160	170	180	200	200	200	200	200	200	200	200	200	200
	I in A	14289	11691	9093	6495	5485	4474	3464	80	80	90	100	110	120	130	140	150	160	170	180	200	200	200	200	200	200	200	200	200	200	200
	A in mm ²	38569	12909	7809	10246	7306	4862	5100	7083	5737	4533	3471	2550	1771	1133	637	283	71	19	4.8	125	125	125	125	125	125	125	125	125	125	125
	m in kg	20734.6	3470	2099.2	2754	1963.8	1307	1370.9	1904	1542.2	1218.6	933	685.4	476	304.6	171.4	76.2	19	4.8	125	125	125	125	125	125	125	125	125	125	125	125
AC 690 V	I in A	8284	6778	5271	3765	3180	2594	1634	1714	2380	1928	1523	1166	857	595	381	214	95	24	6.4	144	144	144	144	144	144	144	144	144	144	144
	A in mm ²	12962	4338	2624	3443	2455	1634	1714	2380	1928	1523	1166	857	595	381	214	95	24	6.4	144	144	144	144	144	144	144	144	144	144	144	144
	m in kg	6968.1	1166.2	705.5	925.5	660	439.2	460.7	639.9	518.3	409.5	313.5	230.4	160	102.4	57.6	25.6	6.4	1.8	4.8	125	125	125	125	125	125	125	125	125	125	125
	I in A	7145	5846	4547	3248	2742	2237	1732	1443	1299	1155	1010	866	722	577	433	289	144	36	9.1	22.1	22.1	22.1	22.1	22.1	22.1	22.1	22.1	22.1	22.1	22.1
AC 800 V	A in mm ²	9642	3227	1952	2561	1826	1216	1275	1771	1434	1133	868	637	443	283	159	71	18	4.8	125	125	125	125	125	125	125	125	125	125	125	125
	m in kg	5183.6	867.5	524.8	688.5	491	326.7	342.7	476	385.6	304.6	233.2	171.4	119	76.2	42.8	19	4.8	125	125	125	125	125	125	125	125	125	125	125	125	125
	I in A	1125	1125	1125	438	438	438	250	283	250	283	159	177	195	212	230	248	266	283	301	319	337	355	373	391	409	427	445	463	481	500
	A in mm ²	319	478	637	310	372	434	283	3200	2667	2400	2133	1867	1600	1333	1067	800	533	267	2056	1625	1428	1244	1073	914	768	635	514	409	319	256
disp. 800 V	m in kg	228	514	914	555	800	1088	812	514	635	768	914	1073	1244	1428	1625	1834	2056	228	514	914	1333	1867	2400	2979	3558	4137	4716	5295	5874	6453
	I in A	13200	10800	8400	6000	5067	4133	3200	2667	2400	2133	1867	1600	1333	1067	800	533	267	2056	1625	1428	1244	1073	914	768	635	514	409	319	256	205
	A in mm ²	21941	7344	4443	5829	4156	2766	2901	4030	3264	2579	1975	1451	1007	645	363	214	95	24	6.4	144	144	144	144	144	144	144	144	144	144	144
	m in kg	7863.8	1316	796.1	1044.5	744.8	495.7	519.9	722.1	584.9	462.2	353.8	260	180.5	115.5	65	28.9	7.2	1.8	4.8	125	125	125	125	125	125	125	125	125	125	125
DC 750 V	I in A	6600	5400	4200	3000	2533	2067	1600	1333	1200	1067	933	800	667	533	400	267	133	10	2.5	6.4	6.4	6.4	6.4	6.4	6.4	6.4	6.4	6.4	6.4	6.4
	A in mm ²	5485	1836	1111	1457	1039	692	725	1007	816	645	494	363	252	161	91	40	10	2.5	6.4	6.4	6.4	6.4	6.4	6.4	6.4	6.4	6.4	6.4	6.4	6.4
	m in kg	1965.9	329	199	261.1	186.2	123.9	130	180.5	146.2	115.5	88.5	65	45.1	28.9	16.2	7.2	1.8	0.5	1.8	4.8	4.8	4.8	4.8	4.8	4.8	4.8	4.8	4.8	4.8	4.8
	I in A	3300	2700	2100	1500	1267	1033	800	667	600	533	467	400	333	267	200	133	67	3	0.8	2.5	2.5	2.5	2.5	2.5	2.5	2.5	2.5	2.5	2.5	2.5
DC 3000 V	A in mm ²	1371	459	278	364	260	173	181	252	204	161	123	91	63	40	23	10	3	0.8	2.5	2.5	2.5	2.5	2.5	2.5	2.5	2.5	2.5	2.5	2.5	2.5
	m in kg	491.5	82.3	49.8	65.3	46.6	31	32.5	45.1	36.6	28.9	22.1	16.2	11.3	7.2	4.1	1.8	0.5	0.5	1.8	4.8	4.8	4.8	4.8	4.8	4.8	4.8	4.8	4.8	4.8	4.8

Table A.3 – Calculation of copper demand for Layout 2 in Scenario 1 for the different distribution grid types and voltages with the charging power P for each charging point and the distance l to the substation. For each grid type and each voltage level, the current (per phase), required cross-section, and copper demand between two charging points are shown. The figures given are for one lane and must be multiplied by the number of lanes (four for Scenario 1).

Grid type	Parameter	MCS						HPC			
	P in kW	900	900	900	900	900	900	700	700	700	400
AC 400 V	l in m	20	28	36	44	52	60	20	26	32	38
	I in A	7794	6495	5196	3897	2598	1299	3608	2598	1588	577
	A in mm ²	22950	6375	4080	2295	1020	255	6324	984	367	85
	m in kg	12337.9	1370.9	877.4	493.5	219.3	54.8	3400	158.6	59.2	13.7
AC 690 V	I in A	4518	3765	3012	2259	1506	753	2092	1506	920	335
	A in mm ²	7713	2142	1371	771	343	86	2125	331	123	29
	m in kg	4146.3	460.7	294.9	165.9	73.7	18.4	1142.6	53.3	19.9	4.6
AC 800 V	I in A	3897	3248	2598	1949	1299	650	1804	1299	794	289
	A in mm ²	5737	1594	1020	574	255	64	1581	246	92	21
	m in kg	3084.5	342.7	219.3	123.4	54.8	13.7	850	39.7	14.8	3.4
disp. 800 V	I in A	1125	1125	1125	1125	1125	1125	438	438	438	250
	A in mm ²	319	446	574	701	829	956	124	161	198	135
	m in kg	228	448	740	1106	1545	2056	89	150	227	183
DC 750 V	I in A	7200	6000	4800	3600	2400	1200	3333	2400	1467	533
	A in mm ²	13056	3627	2321	1306	580	145	3598	560	209	48
	m in kg	4679.3	519.9	332.7	187.2	83.2	20.8	1289.5	60.2	22.5	5.2
DC 1500 V	I in A	3600	3000	2400	1800	1200	600	1667	1200	733	267
	A in mm ²	3264	907	580	326	145	36	899	140	52	12
	m in kg	1169.8	130	83.2	46.8	20.8	5.2	322.4	15	5.6	1.3
DC 3000 V	I in A	1800	1500	1200	900	600	300	833	600	367	133
	A in mm ²	816	227	145	82	36	9	225	35	13	3
	m in kg	292.5	32.5	20.8	11.7	5.2	1.3	80.6	3.8	1.4	0.3

Grid type	Parameter	NCS									
	P in kW	200	200	200	200	200	200	200	200	200	200
AC 400 V	l in m	20	32	44	56	68	80	92	104	116	128
	I in A	2887	2598	2309	2021	1732	1443	1155	866	577	289
	A in mm ²	14167	6885	5440	4165	3060	2125	1360	765	340	85
	m in kg	7616	2220.8	1754.7	1343.5	987	685.4	438.7	246.8	109.7	27.4
AC 690 V	I in A	1673	1506	1339	1171	1004	837	669	502	335	167
	A in mm ²	4761	2314	1828	1400	1028	714	457	257	114	29
	m in kg	2559.5	746.3	589.7	451.5	331.7	230.4	147.4	82.9	36.9	9.2
AC 800 V	I in A	1443	1299	1155	1010	866	722	577	433	289	144
	A in mm ²	3542	1721	1360	1041	765	531	340	191	85	21
	m in kg	1904	555.2	438.7	335.9	246.8	171.4	109.7	61.7	27.4	6.9
disp. 800 V	I in A	125	125	125	125	125	125	125	125	125	125
	A in mm ²	35	57	78	99	120	142	163	184	205	227
	m in kg	25	65	123	199	293	406	537	686	854	1040
DC 750 V	I in A	2667	2400	2133	1867	1600	1333	1067	800	533	267
	A in mm ²	8059	3917	3095	2369	1741	1209	774	435	193	48
	m in kg	2888.4	842.3	665.5	509.5	374.3	260	166.4	93.6	41.6	10.4
DC 1500 V	I in A	1333	1200	1067	933	800	667	533	400	267	133
	A in mm ²	2015	979	774	592	435	302	193	109	48	12
	m in kg	722.1	210.6	166.4	127.4	93.6	65	41.6	23.4	10.4	2.6
DC 3000 V	I in A	667	600	533	467	400	333	267	200	133	67
	A in mm ²	504	245	193	148	109	76	48	27	12	3
	m in kg	180.5	52.6	41.6	31.8	23.4	16.2	10.4	5.8	2.6	0.6

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Acronyms

AC	Alternating current
BMS	Battery Management System
CCM	Continuous Conduction Mode
CCS	Combined Charging System
CHAdemo	CHArge de MOve
CO ₂	Carbon Dioxide
DAB	Dual Active Bridge
DC	Direct Current
DCM	Discontinuous Conduction Mode
DSP	Digital Signal Processor
DUT	Device under Test
ESR	Equivalent Series Resistance
EU	European Union
EV	Electric Vehicle
EVSE	Electric Vehicle Supply Equipment
FFT	Fast Fourier Transformation
FHA	Fundamental Harmonic Approximation
FPGA	Field Programmable Gate Array
GaN	Gallium Nitride
GHG	Greenhouse Gas
HPC	High Power Charging
HV	High Voltage
ICE	Internal Combustion Engine
IEC	International Electrotechnical Commission
IGBT	Insulated-Gate Bipolar Transistor
ISO	International Organization for Standardization
LFP	Lithium Iron Phosphate
LLC	LLC Resonant Converter
LUT	Lookup Table
LV	Low Voltage
MCS	Megawatt Charging System
MCU	Micro Controller Unit
MOO	Multi-Objective Optimization
MOSFET	Metal-Oxide Semiconductor Field-Effect Transistor
MV	Medium Voltage
NCS	Night Charging System
NMC	Nickel Manganese Cobalt oxide
OBC	On-board Charger
PCB	Printed Circuit Board

PSFB	Phase-Shift Full Bridge
PWM	Pulse-Width Modulation
RMS	Root Mean Square
Si	Silicon
SiC	Silicon Carbide
SOC	State Of Charge
SPS	Single Phase Shift
TRAM	Trapezoidal Modulation
TRIM	Triangular Modulation
TSC	Two Stage Converter
V2G	Vehicle-to-Grid
V2H	Vehicle-to-Home
V2L	Vehicle-to-Load
XML	Extensible Markup Language
ZCS	Zero Current Switching
ZVS	Zero Voltage Switching

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