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Selektive Epitaxie für Quantenbauelemente

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Zusammenfassung

Die vorliegende Arbeit befasst sich mit der Prozessentwicklung von p- und n-dotierter selektiver Epitaxie (SE) für die Herstellung von hochdotierten source/drain-extensions in der höchstintegrierten CMOS-Produktion. Die kontinuierliche Verkleinerung von CMOS- und DRAM-Strukturen erfordert sehr abrupte Dotierübergänge, vor allem an den Grenzen von halo/extension. Weil die Diffusion von Dotierstoffen (vor allem von Bor) exponentiell temperaturabhängig ist, muss das thermische Budget von Dotier- und nachfolgenden Prozessen stark verringert werden, um die Anforderungen der IRTS[1] an die kommenden Technologienoden zu erfüllen. Das ist für die bisher benutzte Ionenimplantation nicht möglich, weil sie einen nachfolgenden Hochtemperaturschritt zum Ausheilen des Kristallgitters benötigt. Die selektive Epitaxie hat sich als eine vielversprechende Technology erwiesen, um die Ionenimplantation in Zukunft zu ersetzen.

Das minimal notwendige thermische Budget zur kontaminationsfreien Vorreinigung wurde für das AMAT Centura Epi System ermittelt. Die minimal mögliche Temperatur zum Entfernen von Siliziumdioxid und Kohlenstoff von Si(100)-Oberflächen wurde auf zu 775 °C bestimmt. Je grösser der Sauerstoffpartialdruck, desto höher muss die Temperatur bei der Vorreinigung sein. Es konnte gezeigt werden dass dieses Gleichgewicht zwischen Sauerstoffpartialdruck und Temperatur nicht nur im Ultrahochvakuum (UHV), sondern auch bei Einleitung von Argon oder Wasserstoff gilt. Die Zugabe von Wasserstoff bei der Reinigung führt zu einem Ausweichen des Gleichgewichtes in Richtung kleinerer Temperaturen und höheren Sauerstoffpartialdruckes. Für Prozesstemperaturen $\leq$ 900 °C kann eine Ätzwirkung des Wasserstoffs auf Siliziumdioxid ausgeschlossen werden. Die thermische Desorptionsreaktion $Si + SiO_2 = 2SiO$ wird deshalb als fundamental für die Siliziumsubstratreinigung sowohl mit den Gasen Wasserstoff, Argon als auch im UHV vorgeschlagen. Ausserdem werden Kohlenstoffverunreinigungen durch den Wasserstoff entfernt. Die Entfernung von Siliziumdioxid durch Reduktion mit Silan wurde untersucht, konnte aber nicht erfolgreich durchgeführt werden. Als Ursache wurde der (zu hohe) Sauerstoffpartialdruck durch die Leckrate der Epitaxieanlage identifiziert. Es wurden auch Versuche zur Oxidreduktion mit German ermittelt, aber die gleichzeitige Abscheidung von Germanium auf der Si(100)-Oberfläche liess sich für die betrachteten Prozessparameter nicht unterdrücken.

Durch die systematische Untersuchung der Bor-Dotierung mit Diboran wurde es möglich einen CMOS kompatiblen selektiven Epitaxieprozess für die industrielle Produktion von source/drain-extensions in PMOS vorzustellen. Dieser erfüllt die Anforderungen der IRTS an die kommenden Technologienoden. Diclorsilan (DCS) ohne zusätzliches HCl wurde für die Abscheidung verwendet. Selektivität gegenüber Siliziumdioxid wurde für i-Si und i-$Si_{1-x}Ge_x$ bei kleinen Prozessdrücken (10 und 20 Torr) festgestellt. Die gemessenen

[1] International Technology Roadmap for Semiconductors

Schichtdicken sind über den gesamten Wafer homogen. Selektivität gegenüber Siliziumdioxid wurde auch für Si:B and $Si_{1-x}Ge_x$:B beobachtet. Die selektiv gewachsenen Schichtdicken waren für alle durch-geführten Prozesse über 50 nm. Auch für Si:B und $Si_{1-x}Ge_x$:B sind die gemessenen Schichtdicken über den gesamten Wafer homogen. Die Zugabe von German zum Epitaxieprozess führt zu stark erhöhten Wachstumsraten, v. a. für Temperaturen unter 700 °C. Durch TEM[2]-Aufnahmen und PIN-dioden wurden sehr kleine Defektdichten festgestellt. Die Verringerung der Prozesstemperatur auf 625-550 °C resultiert in atomar glatten Oberflächen, sogar für Germanium-Konzentrationen von 30%. Dieser Effekt kann auf die starke (exponentielle) Temperaturabhängigkeit der Kristallgitterrelaxation zurückgeführt werden. Bis zu einer Konzentration von 18% Germanium sinkt der spezifische elektrische Widerstand mit steigendem Germaniumgehalt. Dasselbe gilt für das Verhalten von epitaktischen $Si_{1-x}Ge_x$:B-Schichten, die mit den Prozessgasen Silan-German-Diboran gewachsen wurden. sind vermutlich unabhängig von der Wahl der Prozessgase. Die gemessenen spezifischen Widerstände (0.8 mΩ cm für Si:B and 0.6 mΩ cm für $Si_{1-x}Ge_x$:B) erfüllen die Anforderungen der IRTS an die kommenden Technologienoden. Zusammen mit hoher Kristallqualität, Schichtdickenhomogenität und ausreichender Wachstumsrate (ca. 5 A°/s) erfüllt der vorgestellte Prozess alle Anforderungen einer industriellen Produktionsumgebung.

Die n-Dotierung von Si/ $Si_{1-x}Ge_x$ mit Arsin zur Herstellung von source/drain-extensions in NMOS wurde für DCS und Silan untersucht. Für LPCVD bei 10 Torr Prozessdruck bleibt die eingebaute Arsen-Konzentration sehr klein ($10^{17}/cm^3$). Für 640 Torr zeigt die eingebaute Arsen-Konzentration eine Temperaturabhängigkeit von $10^{19}/cm^3$ (775 °C) bis $2*10^{21}/cm^3$ (600 °C). Die Zugabe von 4 sccm German bei einer Prozesstemperatur von 700 °C führt zu einer starken Verringerung des spezifischen Widerstandes (5 mΩ cm) während die Abscheiderate ausreichend hoch bleibt. Somit verhält sich die Dotierung mit Arsin ähnlich wie die Dotierung mit Phosphin. Die Länge der Übergänge in den Dotierprofilen wurde von etwa 20 nm (DCS/German) bis über 50nm (Silan) gemessen. Durch Vorbelegung durch Si(100)-Oberfläche mit Arsin konnte eine Verkleinerung der Länge unter 5 nm erreicht werden. Dieses Verhalten wird mit den elektrischen Eigenschaften der Si(100)-Oberfläche erklärt. Selektivität gegenüber Siliziumdioxid konnte für die Epitaxie von Si:As and $Si_{1-x}Ge_x$:As beobachtet werden. Die Zugabe von German zum Abscheideprozess lösst die hauptsächlichen Probleme in der Dotierung mit Gruppe-V-Hydriden, d. h. kleine Wachstumsrate und Dotierstärke.
Starke Ladungseffekte wurden gemessen sobald Arsin eingeleitet wurde. Die (selektiven) Schichtdicken werden sehr viel grösser mit kleinerer Strukturgrösse. Der Übergang vom Diffusionskontrollierten zum Oberflächenkontrollierten Wachstum konnte als Ursache identifiziert werden. Durch die Prozesschemie enstehen die sehr reaktiven Radikale SiH_3, SiH_2. Diese werden als die limitierenden Spezies in der Dotierung mit Arsin betrachtet.

Das Potential von Disilan als Prozessgas für die Siliziumepitaxie von vertikalen Bauelementen wurde bei sehr niedrigen Temperaturen (≤ 600 °C) wurde untersucht. Eingebaute Bor-Konzentrationen > $5*10^{20}/cm^3$ und sehr hohe Dotierstoffaktivierung bis zu

[2] Transmission Electron Microscopy

einem spezifischen Widerstand von 0.7 mΩ cm konnten erzielt werden. Das ist der kleinste in der Literatur veröffentlichte Wert für epitaktisches Si:B nach dem besten Wissen des Autors. Die Bor-Konzentrationen in der Niedertemperaturepitaxie übertreffen das thermodynamische Löslichkeitslimit. Der Disilan-Diboran-Prozess liefert selbst bei 600 °C ausreichende Wachstumsraten (ca. 8 A°/s) für industriellen Durchsatz. Es wurden keine Ladungseffekte beobachtet. Haze-freie Schichtoberflächen deuten auf gute Kristallqualität hin.
In der As-Dotierung wurden eingebaute Arsen-Konzentrationen > $10^{20}/cm^3$ und sehr hohe Dotierstoffaktivierung bis zu einem spezifischen Widerstand von 0.7 mΩ cm erreicht. Das ist der kleinste in der Literatur veröffentlichte Wert für epitaktisches Si:As nach dem besten Wissen des Autors. Die Arsen-Konzentrationen in der Niedertemperaturepitaxie übertreffen das thermodynamische Löslichkeitslimit. Der Disilan-Arsin-Prozess liefert selbst bei 600 °C ausreichend hohe Wachstumsraten (ca. 5 A°/s) für industriellen Durchsatz. Es wurden keine Ladungseffekte beobachtet. Haze-freie Schichtoberflächen deuten auf gute Kristallqualität hin. Bei der thermischen Dekomposition liefert Disilan hohe Konzentrationen der sehr reaktiven Radikale SiH_3 und SiH_2. Dieser Umstand wird als Ursache für die gegenüber dem DCS-Arsin-Prozess hervorragenden Ergebnisse bei Wachstumsraten, Arsen-Dotierung und Schichtdickenhomogenität betrachtet.

In der vorliegenden Arbeit wird gezeigt dass selektive Epitaxie das Potential hat die Ionenimplantation als Standarddotiermethode in der PMOS-Herstellung zu ersetzen. Die selektive Epitaxie mit n-Dotierung (für die Herstellung von NMOS) weißt inhomogene Schichtdicken und mangelnden Dotierstoffeinbau auf. Das Ersetzen von DCS durch Disilan lösst diese Probleme, aber in der LPCVD konnte Selektivität bisher nur mit clorhaltigen Siliziumgasen erreicht werden. Aus der Diskussion der Ergebnisse wurde geschlossen dass der Sauerstoffpartialdruck aus der Leckrate des Prozessreaktors die Hauptursache für die mangelnde Selektivität ist. Mit kleinerem Sauerstoffpartialdruck wird auch das notwendige thermische Budget für die Vorreinigung niedriger. Aus beiden Gründen muss der Sauerstoffpartialdruck (bzw. die Leckrate) in zukünftigen LPCVD-Produktionsanlagen deutlich verringert werden.

Abstract

This work focuses on the potential of Selective Epitaxial Growth (SEG) for the fabrication of highly doped source/drain-extensions in VLSI[1] CMOS production. SEG is considered to replace ion implantation as the common doping method. The aggressive downscaling of CMOS- and DRAM-structures puts strict requirements on doping shallowness and abruptness of source/drain-junctions. Because diffusion of dopants (especially boron) is strongly temperature activated, the temperature for doping (and subsequent processes) has to be lowered considerably to fulfill the IRTS[2]-requirements for the coming technology nodes. This is not possible for the high-temperature anneal required after conventional ion implantation, but in-situ doped SEG seems to be a promising technology.

The minimum thermal budget to achieve contamination-free silicon surfaces prior to expitaxy could be estimated in an AMAT Centura Epi system. The O_2 partial pressure renders silicon dioxide desorption and enhances reoxidation for temperatures $\leq$ 775 °C in the AMAT Centura Epi System. Hence the cleaning temperature for thermal desorption could not be lowered below 775 °C. For silicon dioxide removal the oxygen pressure could be identified as the most relevant factor. Etching of 1 nm thick silicon dioxide by hydrogen can be ruled out as the main reaction of a 5 min cleaning step at 900 °C. The well known thermal desorption reaction $Si + SiO_2 = 2SiO$ is considered to be fundamental for silicon substrate cleaning under hydrogen, argon and UHV ambient. It was possible to show that the presence of H_2 in the growth enviroment leads to a shift in the steady-state-boundary for achieving oxide free silicon (100) surfaces to less stringent requirements. H_2 also completely removes C impurities. The O_2 partial pressure is also the reason why a silane-assisted cleaning step could not be defined. Germane-assisted cleaning steps were also investigated but growth of germanium on the bare silicon surface could not be avoided and made subsequent low defect epitaxy impossible.

An industrial CMOS compatible selective epitaxial process for the fabrication of source/drain-extensions in PMOS fulfilling the IRTS requirements of the coming technology nodes is demonstrated. A dichlorosilane (DCS) chemistry without additional HCl has been used. Selectivity with respect to silicon dioxide was achieved for DCS at low pressures (10 and 20 Torr). For i-Si and i-$Si_{1-x}Ge_x$ homogeneity over the patterned wafer could be achieved within accuracy of the thickness measurements. Selectivity with respect to silicon dioxide was also achieved for Si:B and SiGe:B. The selectively deposited layer thickness was always above 50 nm. For Si:B and SiGe:B homogeneity over the patterned wafer could be achieved within the accuracy of the thickness measurements. It was found that the addition of germane to the growth enviroment improves deposition rate, especially at temperatures below 700 °C. With TEM[3] investigations and the fabrication of pin-diodes

[1] Very large scale integration
[2] International Technology Roadmap for Semiconductors
[3] Transmission Electron Microscopy

very low defect levels could be confirmed. Dropping the process temperature to 625-550 °C leads to very smooth surfaces, even for Ge-concentrations of 30%; this is attributed to the temperature-activated lattice relaxation. Up to 18% germanium the resistivity drops with rising Ge-content. This agrees with the results for a silane-germane-diborane chemistry and may be independent of precursor choice. The resistivity achieved (0.8 mΩ cm for Si:B and 0.6 mΩ cm for SiGe:B) meets the ITRS requirements of the coming technology nodes. Therefore this process fulfills the requirements of an industrial production sequence.

The results on n-type doping with arsine in silicon epitaxial growth are presented for different process temperatures and precursor chemistries. For LPCVD at 10 Torr the arsenic dopant concentration was always very low ($10^{17}/cm^3$). For 640 Torr the arsenic dopant incorporation shows a temperature dependence ranging from $10^{19}/cm^3$ (775 °C) up to $2*10^{21}/cm^3$ (600 °C). Adding 4 sccm germane at 700 °C drastically reduces the resistivity (5 mΩ cm) while keeping a much higher deposition rate. Therefore the arsine-doping follows a similar trend as reported for phosphine. The doping transition lenghts ranged from about 20 nm (DCS/germane) up to more than 50 nm for silane. They are drasically reduced by an arsine build-up process. The doping behaviour can be explained in terms of the electronic behaviour of the surface.
Selective growth with respect to silicon dioxide has also been achieved for Si:As and $Si_{1-x}Ge_x$:As layers. The addition of germane to the growth enviroment tackles the major problems of n-type doping with the group-V-hydrides, e.g. low deposition rate and doping efficiency.
However, considerably loading effects have been observed as soon as arsine has been added. The growth rates increase strongly with decreasing window size. The shift from the surface controlled growth regime to the mass transport dominated growth regime could be identified as the cause. The deposition chemistry involves production of the very reactive radicals SiH_3, SiH_2. These are considered to be the rate limiting species in doping from arsine.

The potential of disilane as a silicon precursor for very low temperature($\leq$ 600 °C) processes is evaluated. B incorporation in the range $> 5*10^{20}/cm^3$ is shown to be possible. Very high dopant activation down to a resistivity of 0.7 mΩ cm can be achieved. This value is the lowest resistivity published for epitaxially grown B-doped silicon to the best of the author's knowledge. Low-temperature B-doped epitaxy is able to outnumber the thermodynamic solid-solubility limit for B. The disilane-diborane-system provides reasonable deposition rates for industrial throughput even for the low-temperature of 600 °C. Sufficient homogeneity over the wafers is demonstrated (no loading effects). Specular surfaces indicate reasonable crystal quality.
As incorporation in the range $> 10^{20}/cm^3$ is also shown to be possible. Very high dopant activation down to a resistivity of 0.7 mΩ cm can be achieved. This value is the lowest resistivity published for epitaxially grown As-doped silicon to the best of the author's knowledge. Low-temperature As-doped epitaxy is able to outnumber the thermodynamic solid-solubility limit for As. The disilane-arsine-system provides reasonable deposition

rates for industrial throughput even for low-temperatures below 600 °C. Sufficient homogeneity over the wafers (no loading effects) is also demonstrated. Specular surfaces indicate reasonable crystal quality. The disilane molecule decomposes delivering high concentrations of the very reactive radicals SiH_3 and SiH_2. This is proposed to be the reason for the excellent As doping behaviour and the absence of loading effects.

It will be demonstrated that SEG has to potential to replace ion implantation as common doping method in PMOS. SEG with n-type doping for the production of NMOS still lacks the layer homogeneity across the wafer and doping efficiency. Replacing dichlorosilane by disilane is shown to solve these problems, but in LPCVD selectivity can be achieved only with clorinated silicon precursors until now. The O_2 partial pressure stemming from reactor leakage is shown to be the main reason for this. The requirements of the low temperature pre-epitaxial cleaning step are another reason to ower the O_2 partial pressure stemming from reactor leakage considerably in future commercial LPCVD systems.

Contents

1. Introduction

The computing power and speed of integrated circuits made from silicon has increased monotonously and quickly since their introduction more than thirty years ago. The main reason for this trend is the shrinking dimension of the single device (ULSI[1]). This aggressive downscaling of CMOS- and DRAM-structures puts strict requirements on doping shallowness and abruptness of source/drain-junctions. The existing ion implanted profiles result in a gaussian profile and not in a box-shaped profile. Additionally, a high-temperature thermal anneal is required. This thermal budget significantly enhances boron outdiffusion leading to unsharp doping profiles that don't fulfill the requirements of the ITRS[2] for the coming technology nodes.

Increasing use of pseudomorphically grown metastable $Si_{1-x}Ge_x$-structures for strain engineering enhancing hole/electron mobilities in the channel of MOSFET's requires reduced thermal budget to avoid lattice relaxation induced defect generation.

Due to the large lattice misfit of 4% between Si and Ge crystals there is a significant amount of strain energy built up during growth of $Si_{1-x}Ge_x$-alloys. Depending on Ge concentration and layer thickness this energy is relaxed through generation of misfit dislocations. The lattice relaxation is a highly temperature activated process. Thickness and Ge concentration determine the temperature at which the layer can be deposited without starting lattice-mismatch relaxation. Thus lowering growth temperature below 700 °C is necessary to reduce roughness for $Si_{1-x}Ge_x$-epitaxy. This dislocation network generates surface undulations on top of the corresponding $Si_{1-x}Ge_x$-layer. The resulting morphology, known as "cross-hatch", is known to have a bad influence on lateral MOSFET's fabricated on Si/ $Si_{1-x}Ge_x$-heterostructures. Also, layers grown over the $Si_{1-x}Ge_x$-layer like silicides for contacts are known to get a rough surface. This is urgent in the fabrication of vertical devices that are based on $Si/Si_{1-x}Ge_x$ epitaxial layer stacks. For these reasons, epitaxial surfaces should be as flat as possible. However, it should be mentioned that lattice relaxation induced defect generation may also be activated by the thermal budget of following processes.

Another important consequence of the downscaling of CMOS is the necessity for alternative gate dielectrics, so called high-k materials. The thermal stability of the material has to withstand the thermal budget of all following processes. A high-temperature annealing step after ion implantation will drastically limit the possible choice of the material.

To cut a long story short the need for an alternative low temperature doping capable production method is getting more and more urgent.

Epitaxy in CVD provides a way to deposit Si/ $Si_{1-x}Ge_x$ source/drain-junctions with high and abrupt doping levels and low thermal budget. Howewer, epitaxy used to be an areal deposition technique not capable of doping with respect to a specific mask layout as ion implantation does. The key issue is the appropriate choice of growth parameters so that the

[1] Ultra Large Scale Integration
[2] International Roadmap for Semiconductors

deposition on the dielectric mask (e.g. silicon dioxide) is rendered, but not on the Si(100)-surface. This additional requirement considerably limits the process parameter space.
The first part of this work is an introduction into the properties of the Si and $Si_{1-x}Ge_x$ crystals, thin films, followed by a short description of the lateral MOSFET in **chapter 2**. It will be outlined what purpose source/drain-extensions have to fulfill. The chapter ends with the introduction of the vertical pin-diode as a tool for evaluating electrical properties of deposited layers.
In **chapter 3** the Low Pressure Chemical Vapour Deposition (LPCVD)-method the different growth regimes possible are outlined. After that kinetics and the Arrhenius plot will be introduced followed by a presentation of the Applied Materials Centura Epi System. The used precursor gases are listed with the connected growth chemistries. Process conditions necessary for achieving selective epitaxial growth are outlined and the influence of the growth regime on layer thickness homogeneity across the wafer is shown.
Chapter 4 contains the main characterization techniques used in this work and the difficulties that are connected with measuring the properties of SiGe-layers on the nanoscale. These properties are mainly film thickness, doping profiles and crystal quality. Extra focus is laid on Spectral Ellipsometry since it is widely used in this work and some procedures to evaluate layer properties from the raw data were invented by the author. Representative data gained during this work is shown for most techniques.
In **chapter 5** the minimum thermal budget for pre epitaxial cleaning will be considered. For the growth of high-quality epitaxial layers atomically clean surfaces are essential. Contaminations on substrates prevent surface migration of adatoms and act as impurities and/or nucleation centers for defects. The most important are oxygen, carbon, boron and metal contaminants stemming from the air. After insertion of the wafer into the reactor, oxide and carbon impurities will be removed by a heating step that is in Chemical Vapour Deposition normally supported by hydrogen ambient. It will be investigated to remove oxygen, carbon by reductive species like silane or germane to further reduce thermal budget.
Since controlled doping in selective epitaxial growth is the major part of this work **chapter 6** is focused on p-type doping from diborane (B_2H_6) and **chapter 7** on n-type doping from arsine (AsH_3).
A target of the present work is the development of an industrial CMOS compatible selective epitaxial process for the fabrication of source/drain-extensions in PMOS. The specifications have to fulfill the IRTS requirements of the coming technology nodes. This is especially true for the influence of the mask layout on deposition. Increased use of strain engineering for enhanced hole/electron mobilities in CMOS requires reduced thermal budget for the metastable $Si_{1-x}Ge_x$-structures to avoid lattice relaxation induced defect generation. This is closely connected with boron doping. The thermal budget is also closely connected with boron outdiffusion.
Selective epitaxy also provides a method to deposit n-type doped Si/ $Si_{1-x}Ge_x$ source/drain-junctions for NMOS. In this work arsine (AsH_3) is investigated as dopant source. It is well known that n-type doping from group-V-hydrides is difficult because of strong reduction of the growth rate, while doping efficiency is insufficient in most cases. Rough surfaces are also a common problem. The exact doping mechanism is still unclear. It was suggested that

the electronic nature of the surface impacts adsorption behaviour. A semiconductor surface is generally p-type due to a large density of dangling bonds. By heavy adsorption of phosphorus the Fermi level shifts rapidly towards the conduction band. Boron doping caused the Fermi level to shift towards the valence band. Changes in surface adsorption may be expressed as changes in Fermi level and surface band bending. It was also proposed that the number of active adsorption sites is related to the Fermi level which is given from arsenic concentration in the semiconductor bulk and the growth temperature. The transition from an intrinsic semiconductor to an extrinsic semiconductor may also play a role in explaining doping incorporation. Data on homogeneity over the patterned wafer, growth rate and doping efficiency, are still lacking for PH_3 and AsH_3.

Another requirement is the deposition of highly doped Si films on already fabricated structures (e.g. vertical SiGe-diodes or poly-electrodes) that require reduced thermal budget processes. The vertical stacks of SiGe-tunnel diodes or transistors require highly conducting Si top electrodes that must be deposited without degrading the sharpness of the underlying structures. For n-type doping very high doped layers are not provided by CVD yet.

Chapter 8 contains the experiments on low temperature Si deposition from disilane (Si_2H_6). Doping with diborane (B_2H_6) and arsine (AsH_3) is investigated. The doping efficiency is compared to thermodynamically solid-solubility and discussed in terms of metastable structures.

The work finishes with conclusion & outlook in **chapter 9**.

2. $Si_{1-x}Ge_x$/Si(100)-Heterostructures

2.1 The silicon crystal

The silicon bulk structure is determined by sp^3-hybridization of the silicon atoms, leading to four equivalent covalent bonds to nearest neighbours in a tetrahedral coordination. The bulk lattice is diamond like, that is, face-centered cubic with a basis formed of two Si atoms at (0,0,0) and (1/4,1/4,1/4), respectively. The cubic lattice constant is 0.543 nm at room temperature, corresponding to a Si-Si bond length of 0.235 nm. An image of the unit cell is depicted in Fig. 2.1.1 (left hand side).
All low-index surfaces build reconstructions. The reordering of the surface atoms is induced by a partial rebounding of their highly directional dangling orbitals, lowering the surface free energy. Within the scope of this work, the discussion will be restricted to the (100)-surface. It is technologically the most important because of the low interface state density at the Si/SiO_2-interface. For this reason it has been investigated intensively. The formation of dimers lowers the surface energy by about two eV per dimer, reducing the number of dangling bounds by one per surface atom. The expense is the introduction of an additional anisotropical surface stress. The dimerization was first directly "viewed" using STM[1] by Tromp et al. [1]. The dimers form rows along the (110)-directions perpendicular to the dimer bonds. This leads to pronounced anisotropies in surface properties that are relevant to growth, e.g. adatom diffusion and interaction between adatoms and substrate steps. Fig. 2.1.1 (right hand side) shows the most important (2× 1)-reconstruction from the top view.

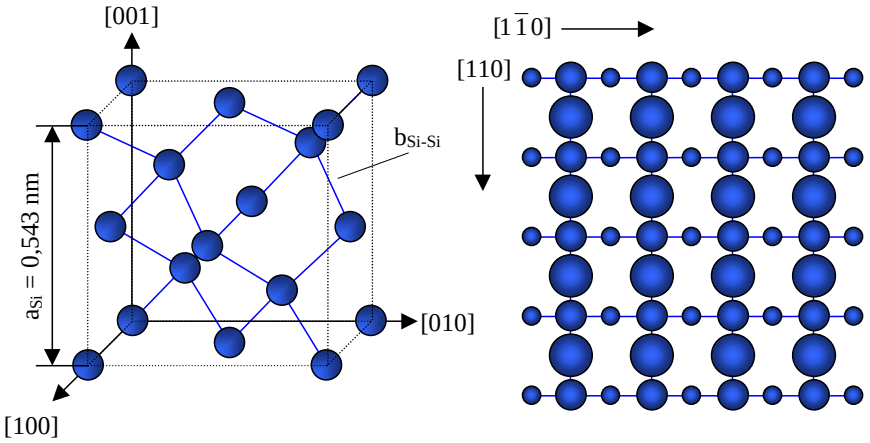

Fig. 2.1.1: View of the silicon bulk lattice. Right: Top view on the Si(100)-surface.

[1] Scanning Tunneling Microscope

2.2 $Si_{1-x}Ge_x$-Heterostructures on silicon (100)

Silicon and germanium are miscible over the entire binary alloy composition range, showing a nearly ideal solid solution behaviour. The lattice constants of $Si_{1-x}Ge_x$ may be estimated with reasonable accuracy by linear interpolation of the lattice constants of Si and Ge. The strain in a $Si_{1-x}Ge_x$/Si-heterostructure is caused from lattice parameter differences (misfit). The lattice constants of Si and Ge at room temperature are 0.5431 nm and 0.5658 nm, respectively. The $Si_{1-x}Ge_x$ lattice parameters have been tabulated by Dismukes et al. [2] for bulk crystals. They found slight deviations from Vegard's law ($a(x)=a_{Si}+x(a_{Ge}-a_{Si})$):

$$a(x) = 0.5431 + 0.0227x \text{ [nm]}.$$

Unequal thermal expansion coefficients are responsible for a second-order effect that is usually much smaller.
Following this discussion, the lattice misfit between germanium and silicon can be varied by the alloy composition in heteroepitaxial growth of $Si_{1-x}Ge_x$-layers. The elastic strain energy that is connected with the lattice misfit can be accomodated in several ways. There are four primary mechanism for strain accommodation:

1. Plastic relaxation by misfit dislocations.
2. Roughening of the layer surface (see chapter 6.2, 6.3).
3. Interdiffusion at the interface.
4. Elasic distortion of the $Si_{1-x}Ge_x$-layer.

1. Strain may be accomodated via the formation of a misfit dislocation array. This allows the epitaxial layer to relax towards its bulk lattice parameter (see Fig. 2.2.1). This is a very prevalent mechanism for strain relief in $Si_{1-x}Ge_x$-layer–based heterostructures. It is experimentally observed and theoretically predicted that plastic relaxation requires a minimum layer thickness ("critical thickness") to operate. Since a misfit dislocation is a significant lattice damage it is generally unwanted.

2. Surface roughening starts earlier, especially at higher temperatures and Ge concentrations. Roughening of the surface allows atomic bonds near the surface to relax towards their equilibrium length and orientation. The basic energetic competition in this process is between the surface energy of the epitaxial layer (representing an increase in the system energy as surface roughening increases the total surface area of the epitaxial layer) and elastic energy. This is reduced by roughening, therefore representing a decrease in the system energy. The resulting surface structures are called "undulations" (see chapter 6).

3. Interdiffusion is only valid for superlattices with a thickness of a few monolayers and will not be discussed within the scope of this work.

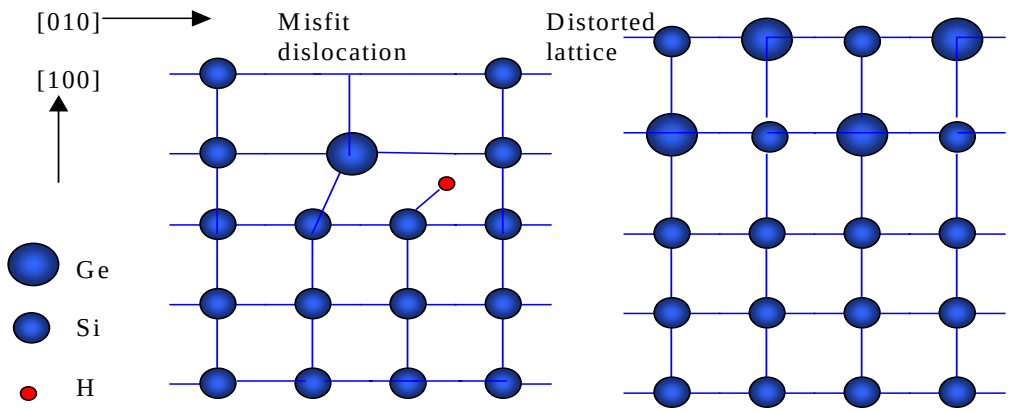

Fig. 2.2.1: Schematics illustration of mechanisms for accomodation of lattice mismatch strain. Left hand side: plastic relaxation by misfit dislocation, the remaining danglind bond is normally occupied by a hydrogen atom. Right hand side: elastic distortion.

4. Strain not accommodated by these mechanisms is relieved by elastic distortion. In this case the in-plane lattice parameter a_{ep} of the epitaxial layer is distorted to that of the substrate. The epilayer lattice parameter perpendicular to the interface a_{en} then relaxes along the interface normal (see Fig. 2.2.1). This produces a tetragonal distortion of the unit cell and its magnitude is given by the ratio of a_{ep}/a_{en}. Such a configuration stores an enormous amount of elastic strain energy of the order of $2*10^7$ [Jm^3] for a lattice mismatch strain of 0.01.

During the initial growth of the alloy a (2×1)-reconstruction forms in order to relieve the surface stress. Approximately one monolayer of Ge segregates to the surface [3,4]. Surface segregation of Ge is suppressed as hydrogen occupies the dangling bonds. CVD[2] from H-containing precursors like dichlorosilane (SiH_2Cl_2) and germane (GeH_4) will result in a H-terminated surface. This is the case at temperatures at which H-desorption from the surface is the growth rate limiting step.
The amount of stress and hence the thermodynamics of the heteroepitaxial system can be varied by growing $Si_{1-x}Ge_x$-layers of different compositions. Under given growth conditions (temperature, deposition rate), the mode of stress relaxation depends critically on misfit strain. Competing paths of stress relaxation have been verified by growth of $Si_{1-x}Ge_x$-alloys on Si(100) [5]. At low Ge concentrations with misfits below 1%, dislocations form before noticeable surface roughening, whereas at high Ge concentration coherent 3d-islands appear before dislocations form. Deposition temperature also plays a role: alloy films grown at lower temperatures first remain smooth until dislocation formation starts later than for higher temperatures [5]. These dislocation network generates surface undulations on top of the corresponding $Si_{1-x}Ge_x$-layer. These morphology is known as “cross-hatch” (see Fig. 2.2.2).

[2] Chemical Vapour Deposition

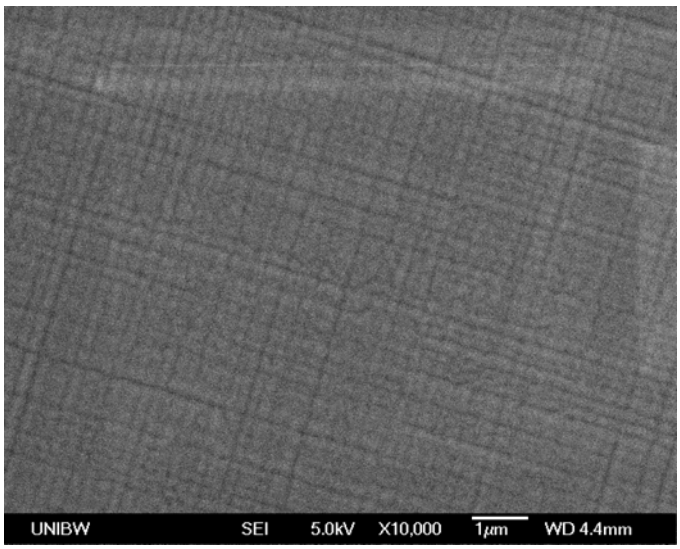

Fig. 2.2.2: SEM-Image of a 250 nm SEG-$Si_{0.65}Ge_{35}$ -layer, showing the typical "cross-hatch".

In Fig. 2.2.3 experimental data from Kasper et al. [6], Bean et al. [7] are compared with equilibrium modeling of critical thickness performed by Matthew and Blakeslee [8] for $Si_{1-x}Ge_x$/Si(100)-heterostructures. It is obvious that the experimentally evaluated critical thicknesses are much higher, especially for smaller growth temperatures, than the theoretical predicted ones.

There are significant kinetic effects associated with the generation of misfit dislocation arrays. These arise primarily from the substantial energetic barriers connected with dislocation nucleation and propagation. The activation energies have to be overcome by thermal activation. In other words, the lower the deposition temperature, the more difficult is the generation of misfit dislocations. It has to be noted, however, that the thermal budget of after-epitaxial processes may also enhance dislocation formation.

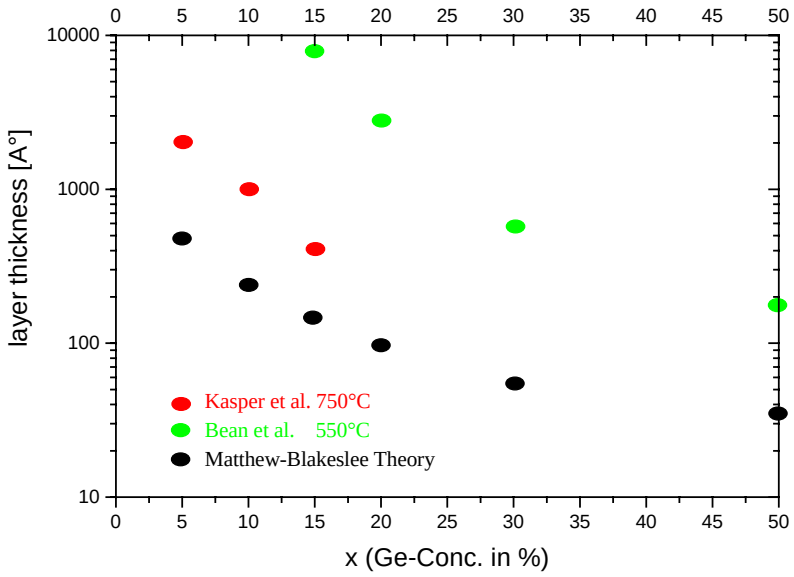

Fig. 2.2.3: Critical thickness as function of lattice mismatch. From [6,7].

2.3 The lateral MOSFET

2.3.1 Basic device concept

The metal-oxide-semiconductor field effect transistor (MOSFET) is the most important device for ultra-large-scale integrated circuits like CMOS based logic devices and semiconductor memories. The principle was first proposed in the early thirtys by Lilienfeld [9] and Heil [10]. It was studied by Shockley and Pearson [11] in the late fourties. The first MOSFET was realized in 1960 by Kahng and Attala using a thermally oxidized silicon structure [12].
The MOSFET is called a unipolar device because the current is transported predominantly by one polarity, electrons in an n-channel device, holes in a p-channel device. It can be made from different semiconductors (e.g. Si, Ge, SiC, GaAs) and different insulators (e.g. SiO_2, Si_3N_4, Al_2O_3, HfO_2), but the most important system is still Si/SiO_2, but alternative gatedielectrica, particularly HfO_2 are under intense investigation. The reason for this development is the continously shrinking device dimension since 1960. The number of components per integrated circuit chip has grown exponentially since 1960, but not the price as is depicted in Fig. 2.3.1 [13].

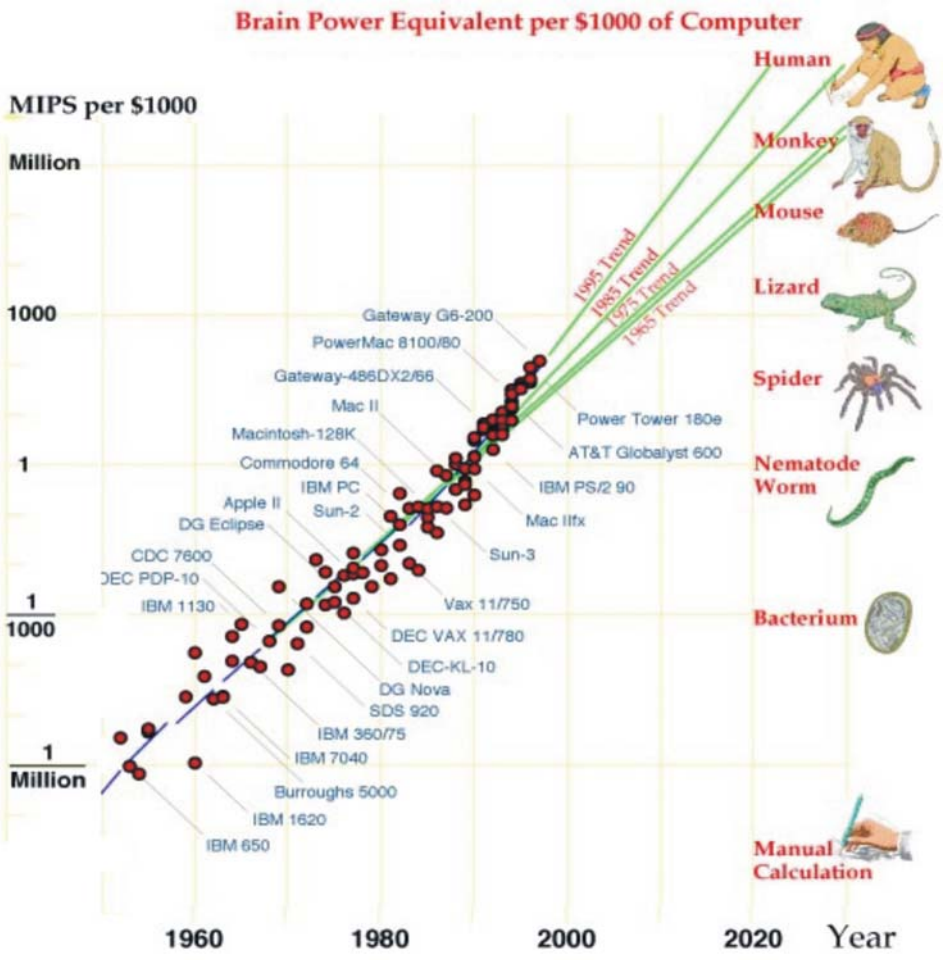

Fig. 2.3.1: Number of devices per $1000.

The most common application is the CMOS-inverter which is the fundamental technological element of all logic IC's. The basic structure of a CMOS-inverter is shown in Fig. 2.3.2. It consists of two connected MOSFETs, one n-channel (NMOS), one p-channel (PMOS) device.

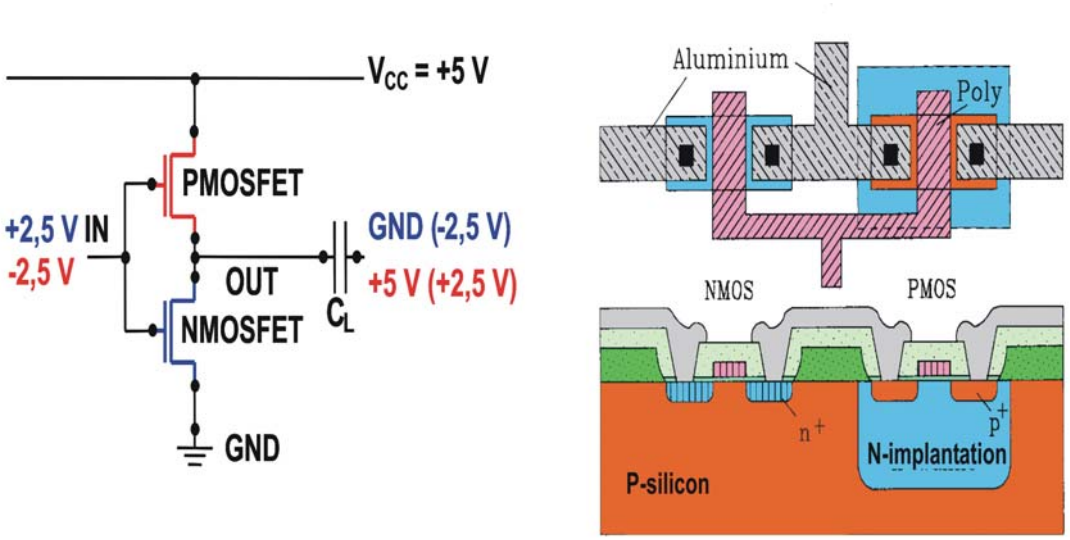

Fig. 2.3.2: Schematics of a CMOS-inverter.

The single transistor is depicted in Fig. 2.3.3 (NMOS in this case). It is made on a p-type silicon substrate with two n^+-regions called source and drain, and a p^--doped area between them. On top of the p^--region is a layer of SiO_2 with an electrode. This is named the gate stack. The gate contact is commonly formed of highly doped polysilicon or a silicide. For the coming technology nodes metal gates are under investigation. There are three other contacts for source, drain and substrate. The basic device parameter are the channel length, the channel width, the gate oxide thickness, the junction depth and the substrate doping.

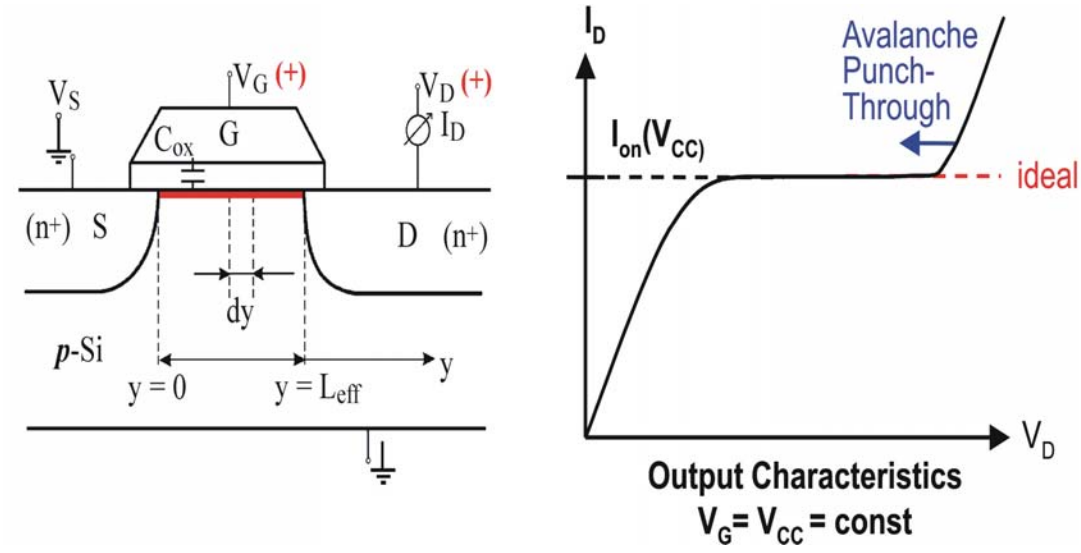

Fig. 2.3.3: Left hand side: diagram of an NMOS, right hand side: I_D-V_D-curve for the inversion case.

When no bias is applied to the gate, the source-to-drain electrodes are equal to biased reverse p-n-junctions. Only the reverse leckage current can flow from source to drain. When a sufficiently large posetive bias (for n-channel device) is applied to the gate, an inversion layer with electrons (called the channel) is built up at the Si/SiO_2-interface. This is called the threshold voltage or V_T. Through this conducting channel now a current can flow between source and drain. The conductance of the channel is a strong function of the gate bias.
The output characteristic (I_D-V_D-curve) has a linear part for small drain bias V_D. For increasing V_D the drain current I_D reaches a saturation region. This is the so called driving current or I_{on}, which obeys the following equation:

$$I_{on} = \mu \cdot C_{Oxide} \cdot \frac{W_{eff}}{L_{eff}(V_D)} \cdot \frac{(V_G - V_T)^2}{2} \qquad [14]$$

C_{Oxide} is normalized with respect to the area and is inverse proportional to the thickness d of the silicon dioxide: $C_{Oxide} = \varepsilon\varepsilon_0/d$, where ε is the dielectric constant. The driving current I_{on} can be increased with higher mobility μ, smaller gateoxide thickness d and smaller channel length L. The further down scaling of d and L is limited as mentioned earlier. A widely investigated approach for enhancing the carrier mobility μ in silicon exploits the fact that compressive strain leads to a higher mobility for electrons (useful for NMOS), and tensile for holes (useful for PMOS), respectively. Compressive (tensile) uniaxial strain can be induced in the channel by fabrication of source/drains from $Si_{1-x}Ge_x$/Si-heterostructures (SiC/Si-heterostructures). Another method is the deposition of a stress liner on top of the device. This is a film that induces compressive or tensile biaxial stress to the underlying MOS channel. E. g. CVD-grown Si_3N_4 induces biaxial tensile strain to underlying films because of the lattice misfit to Si. Applications of strain engineering with liners and heterostructures are found in [14,15,16,17].
It should be noted that the above current equation is derived from a simplied drift model, and does not take into account the more sophisticated drift-diffusion model. Applying a current means leaving thermodynamic equilibrium of the free carriers and hence a “Quasi Fermi level” has to be introduced. Discussing nonequilibrium thermodynamics goes beyond the scope of this work. A more detailed description of MOSFET device physics is given in [18].

2.3.2 Source/Drain-extensions

Since there are no sources and/or drains in the channel the current is conserved as is expressed by the continuity equation. This means $j = Q^*\mu^*E$ is constant, where j is the current density, Q is the inversion charge in the channel normalized with respect to the area, μ is the free carrier mobility and E the electric field strength. The charge in the channel is given by: $Q = C_{Oxide}*(V_G-V_T-V_D(x))$, where V_G is the gate voltage and V_T the

threshold voltage. Hence the inversion charge density near the drain gets smaller with rising bias $V_D(x)$ and the electric field strength near the drain gets higher.
If the field strength gets above $2*10^4$ [V/cm], hot electrons are generated. This leads to degradation of the gate oxide. At $2*10^5$ [V/cm] the critical field strength for impact-ionization in silicon is reached. In this case the drain current I_D is rising exponentially leading to shortage (see Fig. 2.3.3).
The so called avalanche breaktrough depends on the electric field strength near drain. Because the channel lengt is aggressively down scaled [19], the abruptness of the junctions from channel to source/drain is getting more critical with every coming technology node. To overcome this problem technologically graded junctions are fabricated between channel and source/drain. These so called source/drain-extensions (see Fig. 2.3.4) are commonly made by ion implantation. These doping method is dependent on a high-temperature anneal that enhances dopant diffusion, especially for boron in PMOS. Because of that, the necessary junction abruptness cannot ba fabricated this way in future. As an alternative technology the selective doped epitaxy (SDE), which is the subject of this work, will be described in chapter 3.

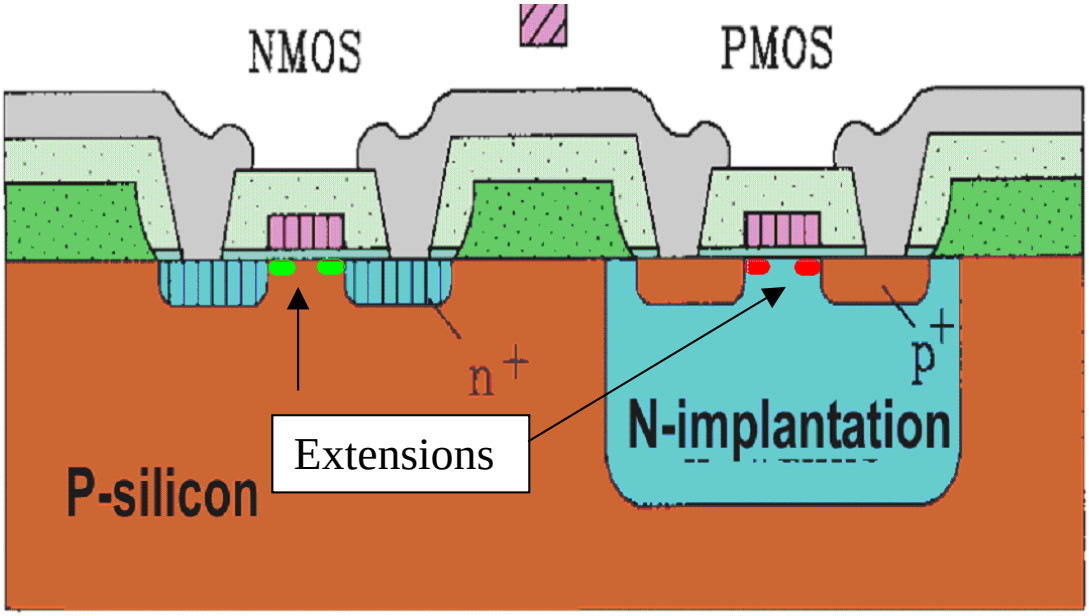

Fig. 2.3.4: Source/Drain-extensions in CMOS.Left hand side: NMOS (extensions are green), right hand side: PMOS (extensions are red).

2.4 The vertical PIN-diode

A vertical pin-diode consists of a vertical pn-junction sandwiching an i-zone (see Fig. 2.4.1). In this work the layer stack is grown areal by LPCVD[1] on a blanket n+-Si(100)-substrate. Then mesas are etched by RIE[2]. After depositing a passivation layer at the sidewalls consisting of LPCVD[1]-grown Si_3N_4 or SiO_2, metal contacts are formed at the top and at the substrate.

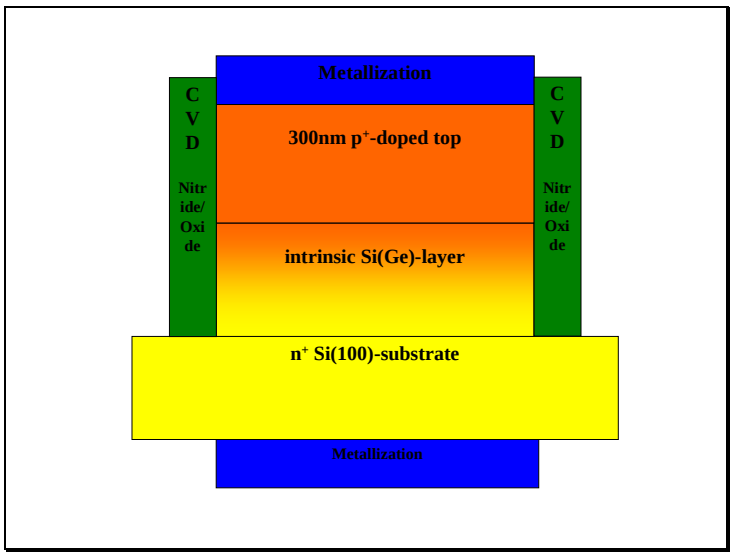

Fig. 2.4.1: Schema of a vertical PIN-diode.

PIN-diodes a very good tool for evaluating the electrical properties of epitaxial grown intrinsic layers (see chapter 4.6) [20,21,22]. A detailed description of the I-V-characteristic is found in [23], with Shockley's equation:

$$I_d = I_{\mathrm{Re}\,verse} * \left[\exp\left(\frac{eV}{nk_BT} \right) - 1 \right]$$

where e is the elementary charge, V is the bias, k_B is the Boltzmann's constant, T is the temperature and n is the ideality factor. With $\frac{eV}{nk_BT} >> 1$, n can be derived from:

$$n = \frac{e}{k_BT} * \frac{d\log(I)}{dV}$$

The ideality factor is an indicator for point defects causing generation- and recombination currents. If n is close to 1 a low density of point defects may be indicated [23].

Reverse bias:

Any extended defect in the i-zone (particularly dislocations) causes a current path increasing the leakage current. This is especially true for misfit dislocations caused by elasic strain relaxation in intrinsic SiGe-layers. Hence a very low leakage current implies a very low (extended) defect density.
In summary two attributes characterize a low-defect pin-diode:

- Ideality factor is close to 1 (forward bias) for pure Si-diodes.
- Very low leakage current (reverse bias). Since the bandgap narrows with rising Ge-content the carrier generation gets larger. Hence SiGe-diodes will always have a larger leakage current as compared to high quality pin-diodes made from pure Si.

The total leakage current of a pin-diode consists of:

1. The reverse thermal current of the ideal pin-diode $I_{Thermal}$ [23].
2. The current through extended lattice defects $I_{Defects}$.
3. The current flowing through the surface passivation $I_{Passivation}$.

1. $I_{Thermal}$ is treated as a constant, because all measurements were done at a constant temperature of 20 °C.

2. $I_{Defects}$ is proportional to the total amount of defects in a vertical pin-diode. These defects are statistically distributed across the mesa area A. For large mesa sizes the amount of defects is large enough to define a mean defect density per unit area. In this case the contribution to I_{Defect} can be measured. For small mesa sizes it is possible that there is no defect and hence no contribution to I_{Defect} at all. With increasing mesa size A the probability for an extended defect increases and due to I_{Defect} the reverse bias current $I_{Reverse}$ will increase abruptly.

3. Any surface passivation contains defects at the interface to the nip-mesa. Hence there is a current flowing at the mesa surface. It is proportional to the circumference of the mesa. Since the vertical pin-diodes used in this work are circular-shaped or quadratic, the mesa area A is proportional to r^2, with r being the radius (circular-shape) or the side length (quadratic shaped). Hence the current $I_{Passivation}$ is proportional to $\sqrt{A}$.

The total reverse current is: $I_{Reverse} = I_{Thermal} + K_{Defects}*A + K_{Passivation} * \sqrt{A}$. $K_{Defects}$ and $K_{Passivation}$ are constants of proportionality.

The measured reverse current per unit area is plotted versus the mesa area A on a logarithmic scale: $I_{Reverse}/A = I_{Thermal}/A + K_{Defects} + K_{Passivation} *(1/\sqrt{A})$.

If no extended defects are present then $I_{Passivation}$ is the dominant current. In that case the graph exhibits a straight line with a slope of –0.5. A straight line with a slope of zero means that $I_{Defects}$ is the dominant current and the extended defect density is constant. If $I_{Reverse}/A$ is rising abruptly with larger A then the amount of extended defects per mesa area A gets bigger with larger A. The transition from a slope of –0.5 to a slope of zero or bigger is connected with the mesa area A where extended defects start to occur.
Fig. 2.4.2 contains a typical example of a pin-diode with an i-zone grown at 775 °C. The slopes are close to zero indicating a constant extended defect density.

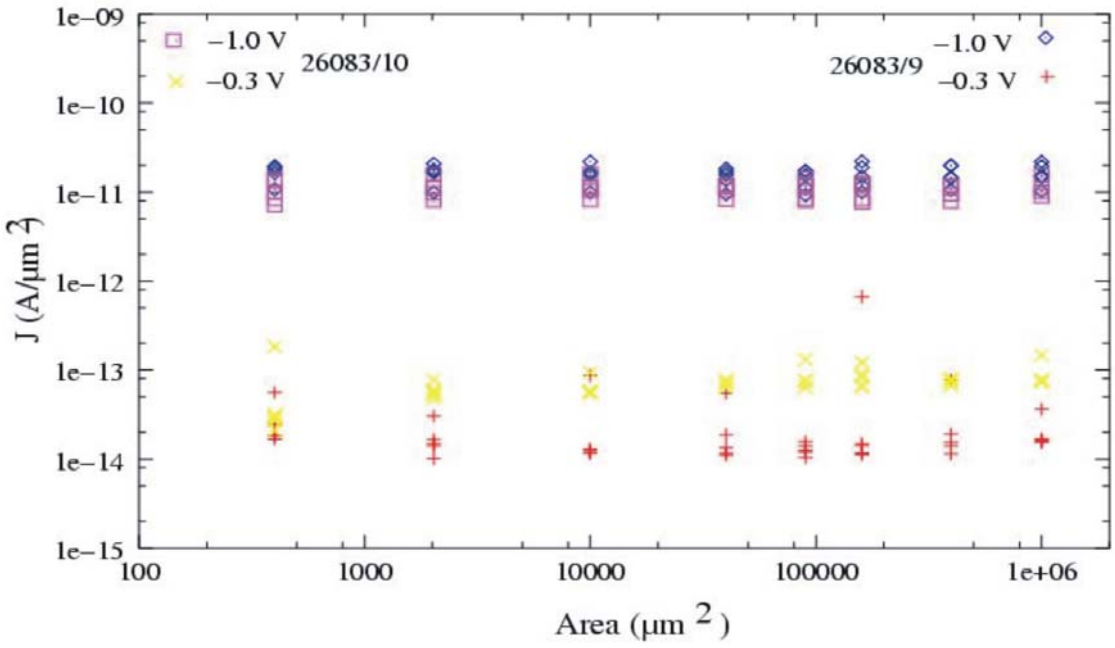

Fig. 2.4.2: Reverse current density over mesa area size. The slope is nearly zero indicating a constant extended defect density.

3. Chemical Vapour Deposition

The urgent need for the deposition of all types of thin layers in modern semiconductor technology leads to many different production techniques. The most common are chemical vapour deposition (CVD), physical vapour deposition (PVD), this includes sputtering and evaporation, electrochemical deposition (ECD) and liquid phase epitaxy (LPE). Advantages of CVD compared to other deposition methods are the possibilities of conformal deposition over patterned substrates (e.g. DRAM trench filling) and selective deposition on dielectric masked substrates. Homogeneous growth over large wafers (up to 300 mm diameter) and good throughput possibilities (drift zones for power devices) make CVD to a very production oriented process.
The different types of CVD-reactors may be divided into (the respective attributes of the Applied Materials Centura Epi System are in bold letters):

- Wafer size possible: up to **200 mm**, 300 mm diameter
- Load: **single-wafer** or multi-wafer (batch)
- Process pressure: athmospheric, **low pressure: 1-100 Torr**, very low pressure: 10-1000 mTorr, ultra-high-vacuum CVD: below 10 mTorr.
- Heating: **radiation (lamps)**, electric resistance, inductive
- Reactor Material: **quartz**, metal
- Temperature distribution: **cold wall**, hot wall
- Susceptor: rapid thermal processing (RTP) with quartz lift pins: 100-300 °c/s, **susceptor with moderate thermal mass: 5-30 °C/s**, batch oven: 10 °C/min

3.1. Overview

Chemical Vapour Deposition means in principle the thermal activated chemical reaction of precursors deposited out of the gas phase onto a catalytic wafer surface, in this work always Si(100). The different processes occuring are as follows:

- Transport of the gases through pipes into the reactor.
- Laminar transport of the gases horizontally across the wafer. Because of the friction between gas phase molecules and wafer the gas velocity gets very small at the surface. The area with velocity gradient is the so called *boundary layer*.
- Homogenous gas phase reactions near the hot substrate.
- Diffusion of the process gases, reactants to the substrate surface through the boundary layer.
- Adsorption of the molecules on the substrate surface.
- Surface diffusion und thermal activated chemical reactions of the gas molecules.

- Surface diffusion and positioning of Si, Ge and dopant atomes at crystal lattice sites.
- Desorption of the by-products and transport out of the reactor.

The process with the largest time constant (the slowest process) is the rate-limiting step. E.g. the deposition rate for dichlorosilane (DCS) related silicon epitaxy is connected to hydrogen desorption from the growing Si(100)-surface as rate-limiting step (see chapter 3.3).

Dependence of growth rate on the process temperature T:

The rate of the slowest surface chemical reaction F_{Chem} (see chapter 3.3 kinetics) is in linear approximation: $F_{Chem} = k*C_S$, where the reaction constant $k \approx \exp\left(\frac{E_A}{k_B * T}\right)$. E_A is the activation energy and k_B the Boltzmann constant.
The chemical surface reactions lead to a decrease of surface precursor concentration C_S on the surface and hence to a concentration gradient between C_S and gas phase concentration C_{Gas}.
This leads to a gas phase molecular flux F_{Diff} through the boundary layer of thickness ρ according to Fick's diffusion law: $F_{Diff} = (D/\rho)*(C_{gas}-C_0)$.
In steady-state the particle flux of diffusion F_{Diff} and the chemical reaction "flux" F_{Chem} on the surface equal each other and hence we get:

$$C_0 = \frac{C_{gas}}{1 + \frac{k * \rho}{D}}$$

k is an exponential function of T and gets very small for low temperatures. Hence the surface chemical reactions are much slower than the gas species diffusion through the boundary layer. This is the so called surface kinetic limited range (see Fig. 3.1.1) with an exponential dependence of deposition rate on temperature. Because the growth is not affected by mass transport it is also not affected by the shape of the wafer surface. Applications are homogenous selective epitaxial growth without loading effects (see chapter 7) and conformal deposition on structures like vertical transistor mesas or DRAM trenches.
For higher temperatures the surface reactions are fast and all precursor molecules transported through the boundary layer react. The growth rate is determined by the diffusion flux $F_{Diff.}$ This is the so called mass transport limited range (see Fig. 3.1.1). Mass transport limited range is governed by higher throughput and a very precise control of growth rate, because there's only a weak temperature dependency. Applications are drift zones for power devices and epitaxial layers on top of wafers.

Dependence of growth rate on the carrier gas pressure P:

The kinetic theory of gases predicts that the diffusion coefficient D is proportional to $T^{\frac{3}{2}}P^{-1}$ [2].
D is rising with decreasing P. This means that the equilibrium between F_{Diff} and F_{Chem} is shifted to higher temperatures. Hence the transition between mass transport limited and kinetic limited region occurs at higher temperatures and higher growth rates (see Fig. 3.1.1) [3].

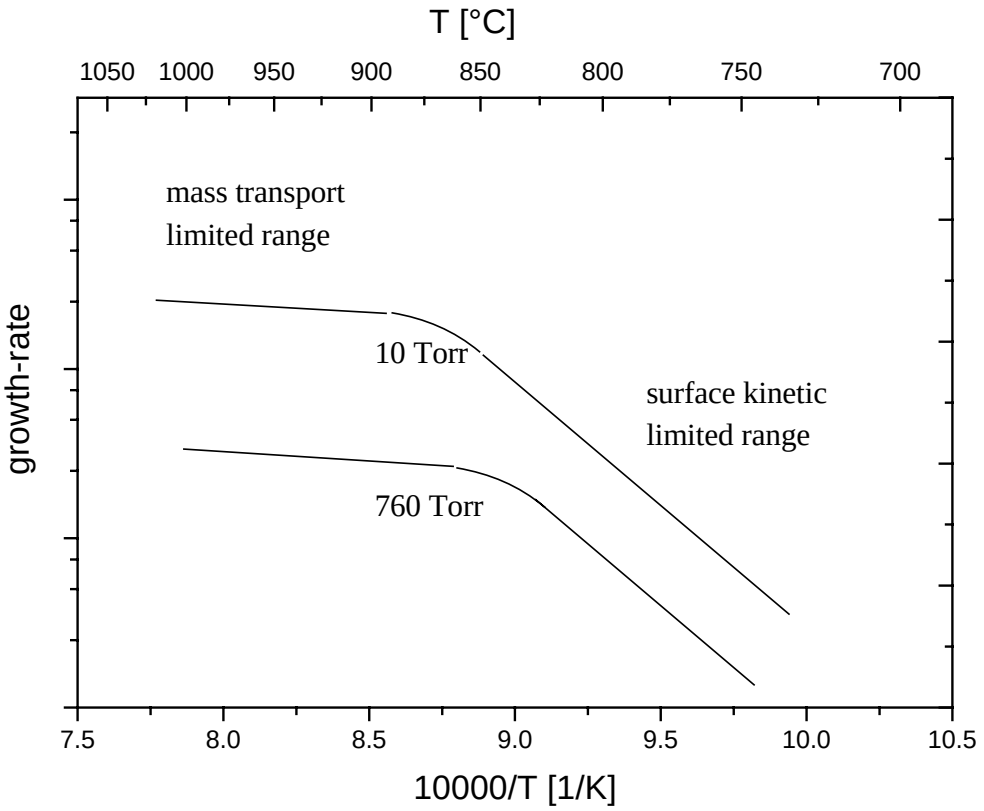

Fig. 3.1.1: Schema of temperature and total process pressure dependence of the growth rate for constant partial pressure of the silicon precursor gas.

3.2 Hydrodynamics and mass transport

The flow-, concentration- and temperature profiles in the reactor determine the structural, electric and optic attributes of the growing layer. They can be described by a system of partial differential equations containg the continuous equation, the Navier-Stokes-equation, Fick's law of diffusion and thermal diffusion (Soret-effect) [4].
The solutions for all relevant reactor geometries can only be obtained by numerical methods. The problem gets even more complex because mass transport and reaction kinetics cannot be decoupled in general [5]. A numeric simulation of the Applied Materials

(AMAT) Centura Epi system goes beyond the scope of this work. For a more detailed approach [6,7] is recommended.
For process pressures between 5-20 Torr used in this work the mean free path of the gas molecules is much smaller than the reactor and wafer dimensions (200 mm diameter). This means that the molecules are interacting with each other and the reactor walls. The gas behaves like a continuous medium and a pressure gradient in the reactor causes a so called viscous flow. The AMAT Centura Epi system is a cold wall reactor with a significant temperature gradient in the growth enviroment. The interaction of the gas molecules with the cold walls of the reactor are responsible for forced convection and the molecules are getting slower at the reactor walls. The gas flow has a laminar profile. For very high velocities the flow becomes turbulent. This is not desired because it leads to inhomogenous deposition across the wafer. Therefor the reactor design has to be sophisticated in terms of the used carrier gas, wafer size and process requirements [1,8].

3.3 Kinetics

The reaction velocity of chemical processes can be described by the theory after Eyring et al. [9]. In this theory, chemical reactions are occuring via an intermediate species as follows:

$$AB \Leftrightarrow AB^* \rightarrow A + B$$

With the equilibrium constant $K = \frac{[AB^*]}{[A][B]}$ of this equation, where [A], [B] and [AB^*] are the respective concentrations, it is possible to calculate the reaction velocity k_1:

$$k_1 = A * \exp\left(\frac{-\Delta H}{kT}\right)$$

This temperature dependence was found experimentally by S. Arrhenius for a lot of chemical reactions. ΔH is the thermodynamic equivalent of an activation energy. The factor A is mostly determined by the structure of the intermediate AB^* and the change in entropy ΔS^*.
Fig. 3.3.1 shows the reaction velocities (growth rates) for a typical CVD-process (Dichlorosilane related silicon epitaxy) used in this work. Because of the exponential temperature dependence the activation energy can be determined as 184 kJ/mol. Sinniah [10] reported an activation energy of 197 kJ/mol for hydrogen desorption from a Si(100)-surface. This may imply that the deposition rate for DCS related silicon epitaxy is connected to hydrogen desorption from the growing surface as rate-limiting step. These results may be used to get a better understanding of the growth process kinetics. It may be

noted that for keeping the surface limited growth regime at temperatures >= 900 °C the DCS flow has to be raised.

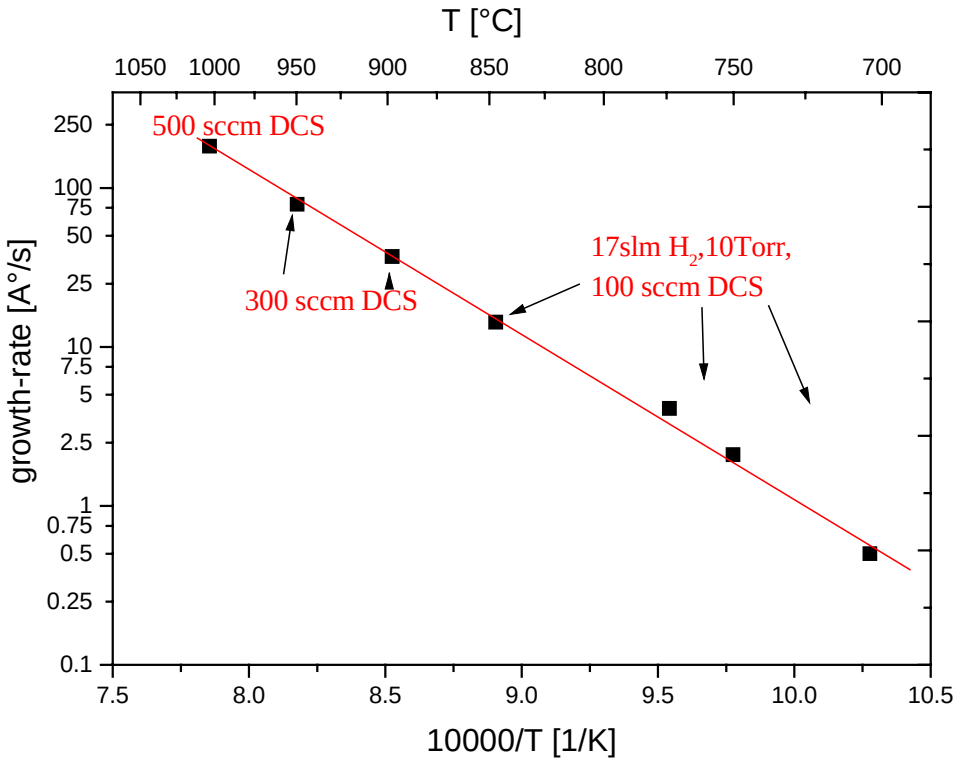

Fig. 3.3.1: Arrhenius plot for for Si-layers grown with dichlorosilane as precursor.

The adsorption of gas species on the Si(100)-surface can be described with a simplified model. A part a_i of a fixed number of adsorption places is covered with an adsorbate i. It is assumed that the adsorption energy is equal for all places and there's no interaction between the adsorbed species. Then the adsorption grade a_i for constant temperature and partial pressure p_i can be described with the Langmuir adsorption isotherm [11]:

$$a_i = \frac{b_i p_i}{1 + b_i p_i}$$

The adsorption coefficient b_i is an equilibrium constant between adsorption and desorption. For chemisorption on polar surfaces the electron transfer from the adsorbed molecule to the surface (surface donor), or otherwise (surface acceptor), has to be taken into account. The molecule is then in a weakly bound neutral state due to dipol interactions (physisorbed) or a strongly bound charged state due to electron exchange (chemisorbed).

This case is described by the Volkenstein-isotherm [12], where E_F is the Fermi level, E_C the conduction band edge, ν^0 and ν^- the phonon frequencies of the adsorbed molecule and N^-, N^0 the number of strong, respectively weak bound molecules.

$$a_i = \frac{N^- + N^+}{N_{chem}} = \frac{\beta p}{1+\beta p}$$

$$\beta = b * \left(\frac{1}{1+\frac{1}{2}\exp\left(E_F - E_a^- + E_a^0\right)} * \left(1+\frac{\nu^-}{2\nu^0} * \exp\left(\frac{E_F - E_C}{k_B T}\right)\right)\right)^{-1}$$

The reaction velocity (growth rate) is determined by the electronic state of the system and not only by temperature and partial pressure.
An example for the influence of the Fermi level on reaction kinetics will be shown in chapter 7: the n-type doping of silicon with arsine as doping gas in CVD.

3.4 The Applied Materials (AMAT) Centura Epi System

The growth equipment consists of an Epi Centura CVD industrial cluster tool manufactured by Applied Materials (Fig. 3.4.1 (a)). 6 Chambers are connected by a transfer chamber with a wafer robot suitable of handling 200mm-substrates: 2 loadlocks capable of storing 25 200mm-Si-wafer each , a cool-down-wafer centering wafer chamber and three growth chambers for SiGe-Epitaxie, Rapid Thermal Processing (RTP) and Metal Organic Chemical Vapour Deposition (MOCVD) for high-k material deposition. The RTP- and the MOCVD chamber are not used within the scope of this work and will not be mentioned anymore. Any chamber is purged with 6N nitrogen if not in use.
The epitaxy-chamber (Fig. 3.4.1 (b), 3.4.2) consists of a single wafer quartz reactor with a SiC-coated susceptor made of graphite. Substrate heating is done by lamp radiation modules with a total power of 50 kW. Together with the moderate thermal mass of the susceptor it is possible to run temperature ramps of 20 °C/s. Temperature controlling is done through a pyrometer on the backside of the susceptor. This means that the reading is independent of the substrate surface (fullsheet or patterned). There is a second pyrometer on top of the wafer to control the wafer surface temperature for silicon epitaxy. Pressure is controlled by Baratrons and may be regulated by a pressure control valve (PCV) built in the gas exhaust line. Process pressure ranges from 5 to 760 Torr with a pumpdown base pressure of 10 mTorr. The vacuum system is ensured via oil-free “dry-running” pumps made by Alcatel. These are only purged with 6N[1] nitrogen to avoid any reactor contamination through the gas exhaust line. The reactor is frequently cleaned from process deposits by etching with hydrogencloride HCL.

[1] 99,9999%

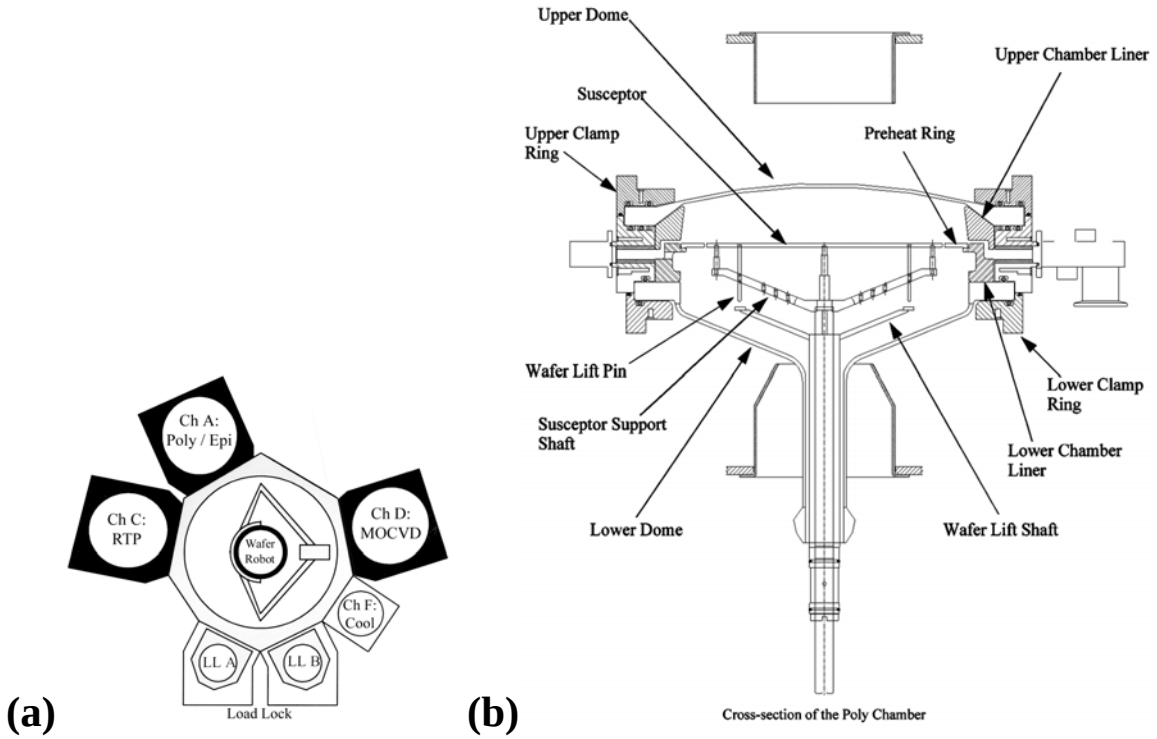

Fig. 3.4.1: Configuration of AMAT Centura platform (a), cross section (b) and **Fig. 3.4.2:** Picture of the Epi chamber.

The following gases are available: silane SiH_4, disilane Si_2H_6, dichlorosilane $SiCl_2H_2$, germane GeH_4, diborane B_2H_6 (p-type doping), phosphine PH_3 (n-type doping) and arsine AsH_3 (n-type doping). A useful precursor gas should fulfill the following attributes:

- Gas should not contain unwanted species like carbon, this could be built into the crystal layer. Because of this reason nearly only hydrides are used. E.g. SiH_4, Si_2H_6, germane etc (see chapters 3.6, 3.7 and 5).

- Very high purity in the ppb level, especially with respect to oxygen and moisture is necessary for low-temperature and selective epitaxy. This requires in-line purifiers in the gas pipes (see chapters 3.6, 3.7 and 5).

- High reactivity at low temperatures for a reasonable througput. On the other hand high thermal stability at room temperature is required to avoid reactions in the gas pipes and prereactions in the gas phase of the reactor. E.g. B_2H_6 tends to be unstable at room temperature after some months.
- Low flammability and toxicity.

- Since semiconductor production has to deal with economy the price of a process gas is always an issue. E.g. Si_2H_6 costs about twenty times the price of SiH_4. On the other hand the superior througput and n-type doping behaviour of Si_2H_6 compared to SiH_4 pays out especially for process temperatures below 650 °C (see chapter 8).

These different requirements cannot be fulfilled together. As mentioned above group-IV and group-V-hydrides don't contain carbon and can be purified to the sub-ppb level, but are self-igniting (silane, disilane) and some are very toxic (phosphine, arsine). This leads to stringent safety precautions in terms of gas leak detectors and waste process gas absorbing facilities.

3.5 Main growth reactions for different precursor gases

3.5.1 Silicon growth with silane (SiH_4)

The chemical reactions for silicon deposition from silane are well known from literature [13,14,15]. After Gates [13] the main feature is the dissociative adsorption of SiH_4 on two surface sites, followed by the fast decomposition of adsorbed SiH_3 in Si and three adsorbed hydrogen atoms. Subsequently hydrogen desorbs from the surface as molecular hydrogen. The kinetic analysis of the growth processes by Gates [13] showed that two regimes are possible. At temperatures above 600 °C the growth rate limiting step is the adsorption of

SiH_4. All following steps are much faster. For temperatures below 600 °C the desorption of hydrogen from the surface is rate-limiting. In both cases a lot of reactions leading to fourteen different silicon containing species are following, the most important are SiH, SiH_2, SiH_3, Si_2H_6,Si_2H_6, Si_3H_8. All are able to contribute to the Si crystal growth.

3.5.2 Silicon growth with disilane (Si_2H_6)

The Si_2H_6 molecule decomposes as follows [16]:

$$Si_2H_6 = SiH_3 + SiH_3$$
$$Si_2H_6 = SiH_2 + SiH_4$$

Both reactions are much faster than the rate-limiting adsorption step of the SiH_4 molecule providing the very reactive radicals SiH_2 and SiH_3. These radicals have a much higher sticking coefficient leading to a much faster adsorption than the SiH_4 molecule [16]. This difference is even bigger (three orders of magnitude) in the case of n-type doping from the group-V-hydrides PH_3 and AsH_3. So the growth rate and n-type doping capabilities of Si_2H_6 are superior to SiH_4 making it the precursor of choice for low-temperature processing (see chapter 7.3).

Here it should be noted that the deposition of Si from trisilane (Si_3H_8) is reported with an even higher growth rate [17]. This behaviour may be explained by a decomposition in two SiH_3 radicals and one SiH_2 radical. SiH_2 is even more reactive than SiH_3 and may contribute more to the Si deposition.

3.5.3 Epitaxial silicon growth with dichlorosilane ($SiCl_2H_2$)

The deposition of Si from chlorosilanes is well investigated. Bloem and Giling [18] investigated experimental growth rate data and reported that the activation energy is always near 47 kJ/mol. Because this matches with the desorption of hydrogen from the Si surface they suggested hydrogen desorption as the rate-limiting step. More complete models were realized by Hierlemann et al. [19] and Ho et al. [20]. In both works the main reactions are:

$$SiCl_2H_2(ads) = SiCl_2(ads) + 2H(ads)$$
$$SiCl_2(ads) + 2H(ads) = Si(ads) + 2HCl$$

It is important to note that the role of hydrogen is not only to occupy adsorption sites as rate-limiting step, but also to react with cloride yielding a desorbing HCl molecule. Thus hydrogen is necessary to remove clorine from the surface. HCl has the additional effect of etching silicon. The etch reaction is strongly temperature activated and does not show any effect in low-temperature deposition at 600 °C (see chapter 8.2). This

lowers the deposition rate, but can be exploited to backetch silicon nuclii on dielectric mask material in selective epitaxial growth (see chapter 3.6). On the other hand, the etch reaction is strongly temperature activated and does not show any effect in low-temperature deposition at 600 °C (see chapter 8.2).

3.5.4 Epitaxial silicon growth of $Si_{1-x}Ge_x$ with dichlorosilane ($SiCl_2H_2$) and germane (GeH_4)

It is well known that adding GeH_4 to an Si deposition process leads to a strong increase in growth rate. Even the rate of the Si growth itself is much higher. E.g. if a $Si_{75}Ge_{25}$-alloy of 100 nm thickness is grown, the deposition rate of the corresponding 75 nm of Si is much smaller for pure Si growth than for the $Si_{75}Ge_{25}$ alloy. This means that the GeH_4 molecule catalysis the Si growth. This behaviour is due to a lower H surface coverage when a limited amount of Ge is present on the surface. The Ge atoms act as desorption centers for adsorbed atomar hydrogen [21]. This means that the activation energy for hydrogen desorption is lower. The activation energy for hydrogen desorption from Si(001) is 47 kcal/mol [22] and from Ge(001) it is 37 kcal/mol [23]. It is interesting to note that high-quality $Si_{1-x}Ge_x$ –structures can be grown with very low oxygen levels even at atmospheric pressure [24,25]. The GeH_4 molecule reacts very fast with oxygen molecules in the process enviroment leading to GeO_x. Ge oxides are known to be unstable at temperatures above 450 °C and hence it will be pumped out of the reactor. This advantageous feature of GeH_4 will also be exploited for low temperature silicon surface cleaning (see chapter 5.3). Another important point is the occurance of inhomogenous layer thicknesses on patterned wafers in selective epitaxial growth, the so called loading effects (see chapter 3.6.3). These are especially strong in the mass transport limited growth regime. At temperatures usually used for $Si_{1-x}Ge_x$-deposition (600-800 °C), Ge growth from GeH_4 is shown to be mass transport limited while Si growth from DCS, SiH_4 and Si_2H_6 is shown to be surface reaction rate limited [26].

3.5.5 In-situ doping with diborane (B_2H_6) and group-V-hydrides

In epitaxial growth the common method of doping is to mix the silicon (and/or germanium) precursors with an additional gas that contains the dopant. After that, the gas composition enters the growth enviroment. Since the dopant is provided during growth of the crystal film, it is positioned and incorporated at lattice sites. This is named *in-situ doping*. The advantages compared to ion-implantation are the smaller thermal budget of the process (no annealing necessary) and the equal distribution of the dopant within the layer leading to shallow profiles. Both are strict requirements for the upcoming CMOS technology nodes.
The most common dopant sources in LPCVD are diborane (B_2H_6) for p-type doping and phosphine (PH_3) as well as arsine (AsH_3) for n-type doping. These are also the precursors discussed within the scope of this work and in the following chapters.

3.5.5.1 *Doping with diborane (B_2H_6)*

Adding B_2H_6 to the process enviroment leads to a slight enhancement of growth rate for temperatures below 750 °C [27-31]. The dependence of dopant incorporation from B_2H_6 partial pressure is linear up to a B concentration of 1E22/cm^3 [31]. An explanation for this behaviour may be that B_2H_6 decomposes in the gas phase into very reactive BH_3 radicals at low temperatures [32-34].

3.5.5.2 *Doping with group-V-hydrides*

Adding phosphine (PH_3) or arsine (AsH_3) to the process gas leads to a significant drop of growth rate [35-40, see also chapter 7]. This effect is for AsH_3 even stronger than for PH_3 [35,40]. To give an explanation for this behaviour, Maity et al. reported that PH_3 is adsorbed at the Si(100)-surface with an adsorption coefficient of nearly 1 [41]. A stable monolayer is built rendering SiH_4 from further adsorbing. In this case only the more reactive species like SiH_2, SiH_3 contribute to the growth (see chapter 3.5.1) because they have a much higher sticking coefficient on P poisoned Si(100)-surfaces. The reactions involving production of SiH_3, SiH_2 are not the rate limiting steps in the deposition of intrinsic silicon from SiH_4 and $SiCl_2H_2$, but they are if PH_3 is added. This behaviour shifts the reaction path from a surface reaction dominated by the decomposition of SiH_4 to a reaction dominated by a gas phase reaction of SiH_4 to SiH_3 and SiH_2. Hence the deposition of P-doped Si from SiH_4 and $SiCl_2H_2$ is mass transport controlled [42]. A similar behaviour and reaction mechanism is true for AsH_3, but the degradation of deposition rate for SiH_4 related growth is even more elonquent [36,41]. The decomposition of Si_2H_6 delivers much more SiH_2 and SiH_3 (see chapter 3.5.2). Because of this behaviour n-type doping with Si_2H_6 as silicon precursor exhibits promising potential and will be investigated in chapter 8.
It has to be noted that mass transport controlled selective epitaxial growth is strongly affected to inhomogeneities in growth rate, so called loading effects [M. Caymax].

3.6 Selective epitaxial growth (SEG)

3.6.1 Motivation

In chapter 2.3 it was outlined that the use of $Si_{1-x}Ge_x$/Si-heterostructures as source/drain-extensions and/or source/drain contacts would be useful for meeting the requirements of coming technology nodes. Source/drain is commonly fabricated by ion-implantation after the processing of the gate stack. If an epitaxial CVD-technique should be used because of the lower thermal budget, it is very useful to grow selectively in the preetched grooves for source/drain. Deposition on the gate stack, spacer material and all other structures like shallow trench isolation (STI) must be avoided. In principle selective epitaxial growth

means that such process conditions are chosen that deposition will take place at the semiconductor surface (in the preetched grooves), but not on the common mask materials SiO_2 and Si_3N_4. A possible process sequence is depicted in Fig. 3.6.1.:

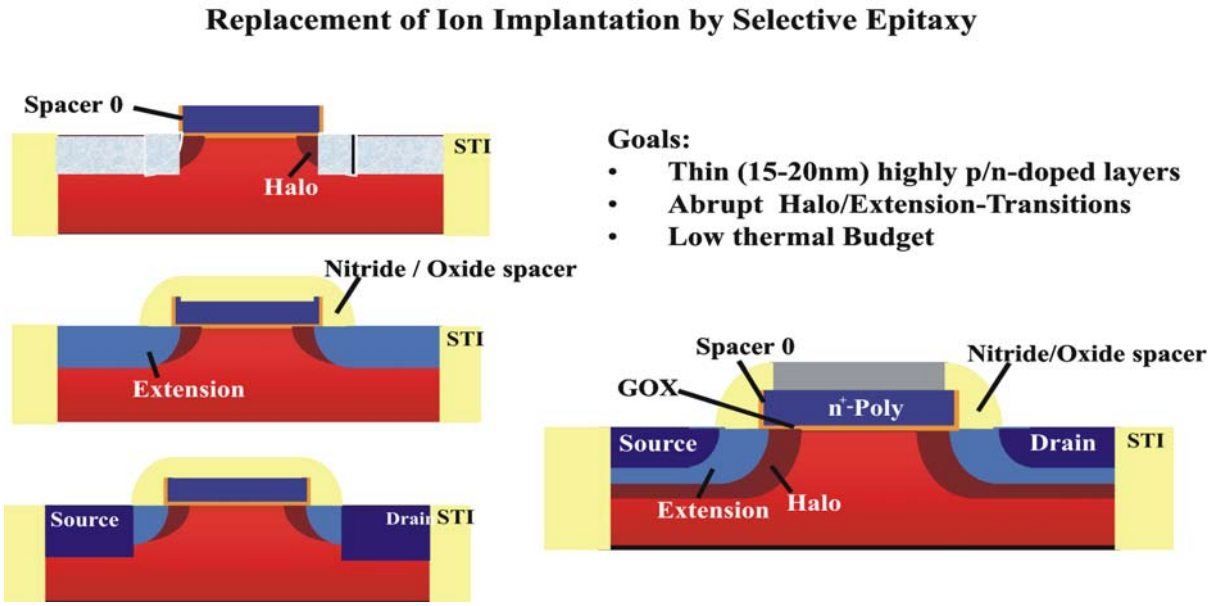

Fig. 3.6.1: MOSFET processing sequence. Left hand side: source/drain-extensions made by SEG. Right hand side: halo pockets, source/drain-extensions and source/drain made by SEG.

After completing the gate stack the grooves for the source/drain-extensions are selectively etched into the silicon substrate. Following a preepitaxial in-situ cleaning step (see chapter 5) the source/drain-extensions are selectively deposited into the grooves with a highly n/p-type doped epitaxy process (see chapter 6 for p-type, chapter 7 for n-type). Subsequently another spacer made of oxide or nitride is CVD-deposited as a mask for the following source/drain-implantation. In a further process sequence depicted on the right hand side of Fig. 3.6.1 halo, extensions and source/drain may be deposited by subsequent selective epitaxial growth.

3.6.2 Process parameters

To discuss selective epitaxy processes we remember the short description of the CVD reaction path illustrated in chapter 1. The process parameters have to be selected so that adsorption and chemical reaction are rendered on the mask material in contrast to the Si(100)-surface. It is known from literature that the deposition on SiO_2 and Si_3N_4 starts after the silicon nuclii reached a critical size (incubation time) [43]. This is performed by avoiding supersaturation of the gas phase [43,44]. Rendering the adsorption of precursor

molecules on the dielectricum may be done by saturating the dangling bonds on the dielectric surface with hydrogen [44,45]. Very low contamination levels for O, H_2O and C are also necessary [44,45,46,47], because these impurities enhance the number of adsorption sites. It is also possible to remove the silicon nuclii from the mask material by etching back with HCl [47,48] . This is performed by passing HCl into the growth enviroment. If DCS is used as silicon precursor then HCl is always present in the growth enviroment (see chapter 3.5.3). Achieving selectivity is much easier with DCS then with non-clorinated silicon sources.
The most important process parameters for avoiding growth on the mask materials SiO_2 and Si_3N_4 are:

- **Low partial pressures of the precursor gases.**
- **Very low contamination levels, partcularly oxygen, moisture, C compounds (see chapter 3.7).**
- **Use of DCS (see chapters 6,7) and HCL as an etching reactant.**

3.6.3 Loading effects

Inhomogenous deposition rates and layer compositions (Ge-content) over the wafer are called *loading effects*. These are related to variations in the wafer topology (see chapter 4.5 for the mask used for wafer patterning in this work) and don't occur during growth on full sheet substrates. The surface topology consists of fields of Si and several other materials, particularly silicon dioxide (fabricated thermally or by CVD), silicon nitride or poly silicon. These fields are arranged in different sizes, forms and areas, what is called the *mask layout*. The material used and the respective layer thicknesses is named the *wafer architecture*. Both mask layout and wafer architecture are connected with loading effects.
Literature divides between microloading and macroloading. Microloading occurs at the microscopic level of single islands or windows. This is leading to a local variation of deposition rate and/or Ge-concentration (see chapter 7.2) as a function of the structure size (in chapter 7.2 window size) and density []. It also occurs that the layer thickness is higher at the edge of Si windows (see also chapter 7.2, Fig. 7.5). Macroloading means an inhomogeneity in growth rate and/or Ge-content over the whole wafer scale. The reason is gas depletion in a horizontal CVD-reactor. The Si and/or Ge precursor is reacting and hence consumed during flowing over the wafer. This means that the partial pressures of the source gases get smaller until the end of the wafer is reached by the gas flow. From the different partial pressures a different deposition rate and/or layer composition results (see chapter 3.1). It is possible to avoid this effect by wafer rotation (10 rounds per minute in this work) and by carefully choosing the process parameters to grow in the surface reaction controlled regime. In the latter case only a little part of the precursors is consumed and hence partial pressure gradient over the wafer stays small.
There are two different reasons for microloading, *chemical leading* and *thermal loading*. Chemical loading is because of gradients in the source gas partial pressures. The

adsorption/desorption of gas molecules is strongly dependent on the different mask surfaces. E.g. DCS and GeH_4 have a tendency not to adsorb on silicon dioxide, this is the cause for selective epitaxial growth. Hence the respective partial pressures are higher than over the exposed Si(100)-surface in an open seed window. The resulting gas phase concentration gradient leads to an additional diffusion flow of Si and/or Ge species towards the windows. A higher deposition rate and different Ge concentration especially at the edges occurs. Chemical loading is particularly strong in the mass transport limited regime due to the rate-limiting precursor diffusion. Since GeH_4 is nearly always mass transport limited (see chapter 3.5.4), careful homogeneity tuning may be necessary.
Addition of doping gases is another issue. In chapter 3.5.5.2 it was mentioned that the addition of PH_3 or AsH_3 to a SiH_4 deposition process shifts the growth regime from surface controlled to mass transport controlled and causes significant loading effects this way [42]. In chapter 7.2 a similar model will be applied to n-type doping by AsH_3 in a $SiCl_2H_2$ process.
Thermal loading is according to inhomogeneities in substrate surface temperature. Heating is performed by lamp modules via direct radiation on the wafer and thermal conduction over the heated SiC-susceptor (see chapter 3.4). This process is heavily affected by the optical properties of the substrate surface defined by wafer architecture and mask layout. While blanket wafers are homogenous in this manner and hence easy to control, patterned surfaces may cause temperature gradients. Since deposition rate is exponentially dependent on surface temperature in the reaction controlled regime (see chapter 3.3), layer thickness and/or Ge-concentration may vary.

3.7 The influence of oxygen partial pressure on CVD

3.7.1 Estimation of oxygen partial pressure for the AMAT Centura Epi system

The main sources of oxygen and moisture in the enviroment of a commercial LPCVD reactor are:

- Hydrogen carrier gas impurities
- Leakage of the reactor

Hydrogen carrier gas impurities

The hydrogen used in this work was delivered from Linde AG with a specification of 5N purity and maximum oxygen/moisture concentrations of 3 ppm and 5 ppm, respectively. At a reactor pressure of 10 Torr the partial pressures of oxygen and moisture stemming from the hydrogen process gas are $3*10^{-5}$ Torr, $5*10^{-5}$ Torr, respectively. Additional experiments were performed after an inline purifier from Mykrolis was installed in the hydrogen pipe. According to the specification the oxygen and moisture levels are reduced

below 1ppb [49]. Hence we can estimate the carrier gas related level of oxygen and moisture to $3*10^{-9}$ Torr and $5*10^{-9}$ Torr, respectively.

Reactor leakage

The oxygen partial pressure caused by leakage may be estimated as follows:

1. Measuring leakage rate with Centura service software; this was always at 1 mTorr/min.

2. Calculating the flux F of air in moles/min following the procedure stated in AMAT Polysilicon-process manual Section 11.3:

$$F = (1mTorr/\min)*12l)/(0.08205*293K) = 0.67*10^{-6}[mol/\min]$$

   with a reactor volume of 12 l. Room temperature (293 K) and a factor containing the gas constant.

3. The air flow F into the reactor can be considered as an additional gas flow consisting of 21% oxygen and 70% nitrogen. Hence the oxygen flow can be estimated as $0.21*F = 0.14*10^{-6}$ [mol/min].
   This is the same order of magnitude Fitch et al. [50] estimated for a commercially avaible CVD-Epi-reactor.

The total process pressure P is set to 10 Torr. Hence the maximum oxygen partial pressure can be calculated as:

$$P_{Ox} = (F_{Ox}/F_{H2})*P(10Torr) = 1.6*10^{-6}[Torr]$$

From this discussion the following conclusions can be drawn:

- The leakage rate is the main source of gas impurities in AMAT-Centura LPCVD growth enviroment as long as process gases pass point-of-use-purifiing to 10 ppb or less.
- To lower the oxygen partial pressure, the smaller process pressures with the same hydrogen flux are required. This is consistent with the results Fitch et al. published in 1994 [50].

Fig. 3.7.1 presents the SIMS–profiles of an arsine doped sample grown at a deposition temperature of 775 °C:

- One can clearly see the oxygen and carbon peak at around 120nm which can be correlated with the layer-substrate interface.
- The plateau of the oxygen signal between 40 to 100 nm indicates the incorporation of oxygen during film growth.

From the above discussion we derive that the impurities in the epitaxial layer stem from the hydrogen carrier gas (water vapor and oxygen). Hence these signals are probably related to the carrier gases‘ purity.
The interface contamination is caused by an insufficient cleaning step that was not able to remove all O, C-impurities.

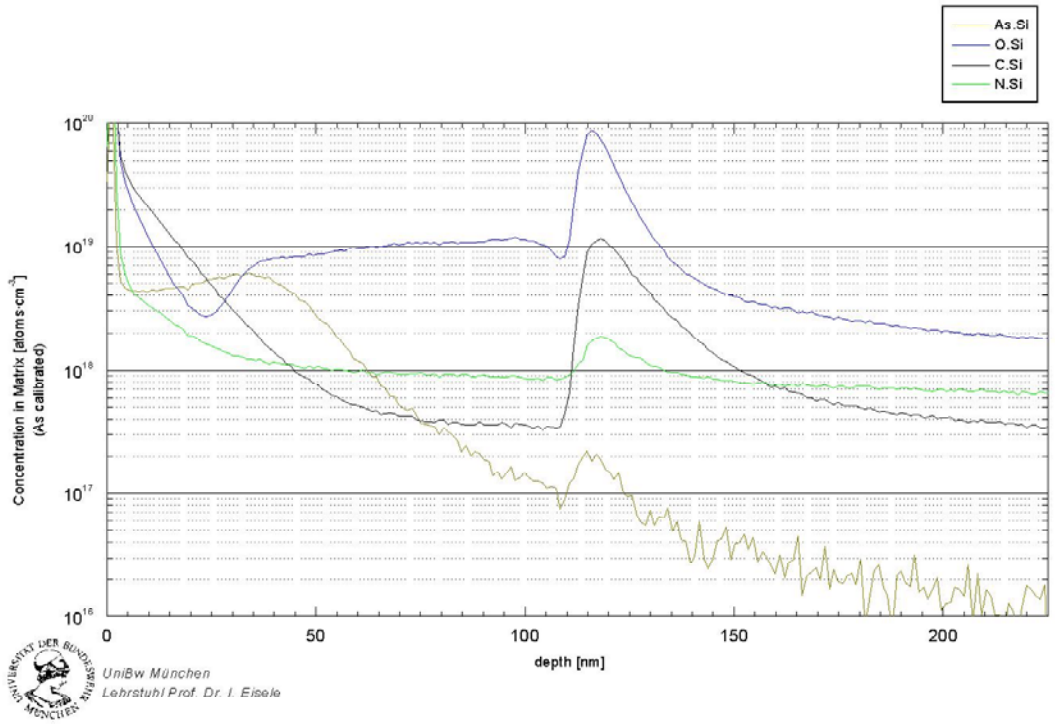

Fig. 3.7.1: SIMS-profiles (O,C,N,As) of an As doped epitaxial layer.

3.7.2 Impact of oxygen and moisture on selectivity

Selective epitaxial growth (SEG) means that process conditions can be chosen such that deposition occurs on an exposed semiconductor surface but not on the common mask materials SiO_2 and Si_3N_4. Hence we should consider the researchers observing full

selectivity (more than 25 nm selectively grown silicon) with respect to silicon dioxide. Most of them are working with ultrahigh vacuum (UHV) CVD–Systems [51-54] with the advantage of very low base pressures of 10^{-6} mTorr. Typical process pressures are in the area of 0.1-100 mTorr. This means that the main source of oxygen and moisture are the precursors. The above mentioned reports all use point–of–use–purifiers for the process gases with a specification of at most 50 ppb (7.5N) residual contaminents. Hence the impurity partial pressures are not higher than 10 mTorr*(1-7.5N), which means $5*10^{-7}$ mTorr. From these considerations, the purity of the carrier gas seems to be very important. They also investigated the correlation between cleanliness and selectivity and concluded that ultraclean reaction enviroment cannot be neglected for SEG. Fitch et al. [55,56] investigated SEG in 1990 for a commercial LPCVD system ($2.5*10^{-4}$-$2.5*10^{-5}$ mTorr) and predicted that selectivity is promoted by reduction of oxygen and water vapor impurity. Sedgwick et al. [57] observed selective growth in atmospheric pressure CVD only under ultrapure conditions (oxygen and moisture level under 50 ppb). With 760 Torr (1 atmosphere) of process pressure, the impurity level can be derived to: (7.5N)*760Torr = $3.8*10^{-2}$ mTorr. This is the same order of magnitude we derived for the AMAT Centura Epi chamber (see chapter 3.7.1).

From the above discussion we may conclude that providing high gas cleanness standards by installing inline gas purifiers for hydrogen and process gases, low reactor leakage and use of loadlocks must not be compromised.

4. Characterization Methods

The purpose of epitaxy is to grow silicon(germanium) layers of uniform and accurate thickness and electrical properties. It is therefore essential that the layer is defect-free and fulfills the structural and electrical specifications. It is the task of characterization to control layer properties and to supply data for process development and troubleshooting in industry and research. Additionally, for production purposes feedback for process control is urgent.
A lot of techniques have been developed ranging from cheap, fast and low accurate all the way to very accurate, time consuming and expensive. The most important features of epitaxial layers and the relevant techniques used in this work are:

- Thickness (see Table 4.1)
- Resistivity (4-point-probing) and doping concentrations (SIMS: Secondary Ion Mass Spectroscopy)
- Surface topography (optical microscopy-haze inspection, AFM: Atomic Force Microscopy, SEM: Scanning Electron Microscopy)
- Crystal quality (TEM: Transmission Electron Microscopy, vertical PIN-diodes)
- Impurity concentrations (SIMS)
- Alloy composition of $Si_{1-x}Ge_x$ layers (RBS: Rutherford Backscattering, SE: Spectral Ellipsometry, SIMS)

Tab. 4.1 lists the layer thickness measurement techniques used in this work and their advantages /disadvantages.

	Weight gain	Stylus profiler	RBS	SIMS	SE	SEM	TEM
Accuracy	0	0	0	+	+	+	+
througput	+	+	-	-	+	0	-
Sample damage	no	no	yes	yes	no	no	yes
Sample preparation	no	yes (patterning)	no	no	no	optional (sputtering)	yes (high effort)
Mapping	no	yes	no	yes (high effort)	yes	no	no
limitations	d > 200 nm Si or Ge	steps necessary	only SiGe		SiGe, Poly		
Depth profiling	no	yes	no	yes	graded layers	no	yes

Tab. 4.1: The measurement techniques for layer thickness used in this work

Weight gain and stylus profiler are the most simple and fastest ways to get an idea of as-grown layer thickness. They provide results within 5 minutes after unloading the wafer from the reactor enviroment. Knowing the layer thickness 4-point-probing delivers very fast date on resistivity. Together with visual haze-inpection it is possible to get first results on thickness, resistivity and crystal quality 10 minutes after unloading from the reactor (see chapter 4.1). In the everyday life of research & development such quick gained data can be very helpful, so the methods described in chapter 4.1 are performed on every sample. However, it has to be mentioned that the more sophisticated methods requiring more effort also give more accurate results.

Spectral ellipsometry (SE) has the capability of quick measurement, but a very good understanding of the underlying material system's optics is necessary to fit an appropriate model to the measured data. Once a layer system is understood, SE provides fast data for layer thickness, alloy composition, eventually interface roughness etc. Performing undestructive measurements make it a state of the art tool for today's industrial production control (see chapter 4.3).

The imaging methods of electron microscopy deliver excellent resolution due to the small wavelengths of high energy electrons (20-200 kV), see chapter 4.4.

4.1. Frequently used measurement techniques

4.1.1. Differential weight gain

This is a very fast and easy technique for areal homoepitaxy also used by other researchers [1,2] It relies on scaling the wafer just before and just after the epitaxy process. The average layer thickness deposited on an unpatterned wafer is then given by: $d = \frac{\Delta M}{\pi R^2 \rho}$, where $\triangle$M is the differential weight gain, R is the Radius of the wafer and ρ=2.328 g/cm^3 the mass density of silicon. E.g. a weight gain of 18.87E-3 g corresponds to a 1 micron thick silicon layer on a 100 mm-wafer. The micro-balance used in this work has an accuracy of 1E-4 g, so in the ideal case a resolution of around 6 nm is possible for a 100mm-wafer. However, there are several limitations:

- The wafer area is not exactly πR^2 because of flat, notch and also the tolerance of the radius has to be kept in mind.
- The mass density may differ from the literature value in case of heavy doping.
- CVD may lead to some deposition on the backside of the substrate, which leads to a slightly higher result for the layer thickness
- The air stream in the clean room enviroment may irritate the micro-balance. On the other hand cleanroom enviroment is necessary for this technique because the particles found in unfiltered air could lead to a higher weight gain than the deposited layer.
- Wafer handling by manual tweezers may also lead to a different weight gain.

It is obvious that the weight gain measurement becomes more reliable with thicker layers and the use of large area wafers. For our system a layer thickness of >=250 nm on a 100mm-wafer delivered reliable results.

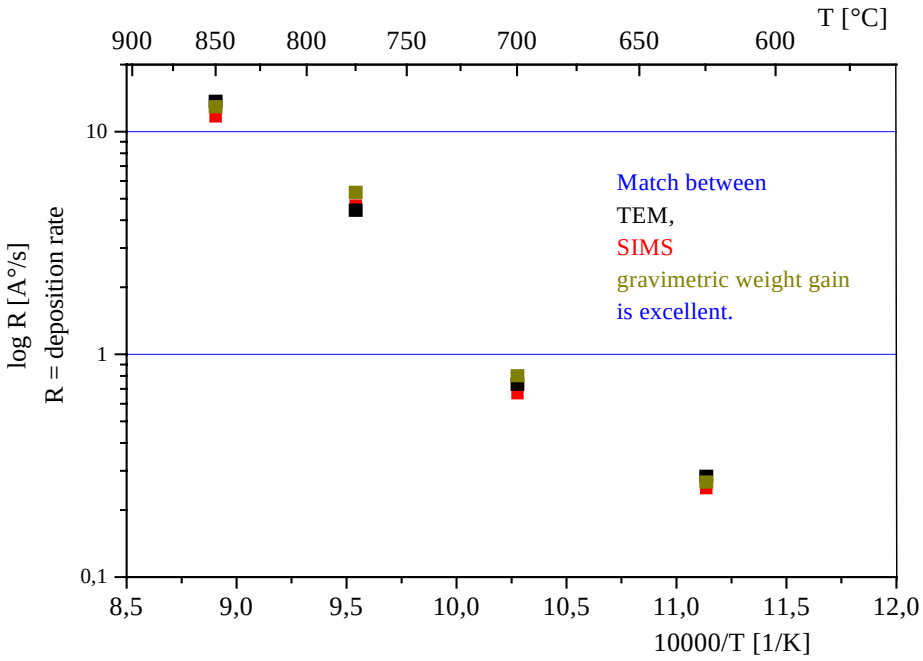

Fig. 4.1: Arrhenius plot gained from gravimetric weight gain compared to the more sophisticated methods TEM and SIMS. The boron doped Si layers were grown with LPCVD.

4.1.2. Mechanical Stylus profiling

This method works with a very small diamond needle that is pulled across the sample surface. This needle is moving vertically at each step in the topography of the wafer surface. The height of this move which is the step height can be scanned inductively and plotted as a function of the needle position.
The mechanical stylus profiler used in this work is a Veeco Dektak 6M with a theoretical resolution of 1 nm [3]. However, there is a high sensitivity to any kind of vibration that is enhancing the resolution.

The typical application in this work is to measure the topography of selectively epitaxially grown layers surrounded by silicon dioxide. Adding the oxide thickness to the step height, the layer thickness is gained even for a $Si_{1-x}Ge_x$-layer.
In general, any layer thickness can be determined by patterning the layer lithographically.
In this case an appropriate etching process that is selective to the underlying structure is required. E.g. polysilicon may be structured selective to silicon dioxide, or $Si_{1-x}Ge_x$ selective to silicon.

4.1.3 Four-Point-Probing (4-pp)

In the 4-pp a known current I is passed between two (outer) probes and the other two (inner) probes are used to measure the resulting voltage drop V. A detailed description of this method is found in [4,5]. In the common case for thin epitaxial layers, the sheet resistance of the layer is: $\rho_S = C * \frac{V}{I}$. Knowing the layer thickness d the resistivity is then easily determined: $\rho = \rho_S * d$.

The major limitation for resistivity measurement of thin epitaxial layers is that the probe current has to be confined within the layer. This may be done by a pn-junction which means that only p/N or n/P structures can be measured. In addition the probe force has to be very small to avoid pressing the tips through the pn-junction into the substrate even for layers of one micron thickness. Because of these reasons floating zone wafers with a resistivity of more than 1500 Ohmcm are used in this work for 4-pp measurements. In this case the substrate resistance is very high and parallel to the sheet resistance and can be neglected.

4.1.4 Optical Microscopy, Haze-inspection

Illuminating the surface of an as-grown epitaxial layer with a halogen lamp delivers first data of surface roughness. The white light is scattered diffusely by surface defects like islands (three-dimensional growth), precipitates (gas phase reactions), undulations (elasic relaxation of $Si_{1-x}Ge_x$ lattice strain, cross-hatch) and deposition on dielectric layers (selectivity control). If one can see a white, milky “haze”, the surface roughness is in the order of the wavelength. If the haze is blue then the surface roughness is smaller, but still undesired. An epitaxial layer of good quality always shows a specular surface without haze. This means that the visual haze-inspection provides a minute time-consuming way of getting a first impression of the layer.
This inspection may also be done by a dark-field microscope to investigate details.

4.2 Secondary-Ion-Mass-Spectroscopie (SIMS)

SIMS depth profiling is an analysis technique capable of determining the elemental concentrations of dopant and impurity atoms within a material as a function of depth. This method is accomplished by sputtering a small part of the sample with a monochromatic ion beam (Cs^+ or O_2^+) of typically 5-10 keV. The following collision cascade ionizes a small part of the milled material. It is possible to collect some of these ions and transfer them to a mass spectrometer (ion mass) for mass filtering. Then a secondary ion detector counts the intensity. Since the material is being continuously eroded it is possible to get chemical information as a function of depth. The ion beam technique requires an ultra-high-vacuum. SIMS is able to detect most elements, in particular all the elements regarded in this work: Si, Ge with their common dopants B, P, As, Sb and their common interface impurities O, C, N. The intensity signal of the particular impurity measured can be calibrated with the

signal of a reference sample with known concentration. The sputtering process results in a crater whose depth can be measured with a mechanical stylus profiler enabling depth profiling. Reference samples for dopants were silicon wafers with specified dopant concentrations from Siltronic AG. As reference samples for O, C implantation standards are common [1]. All the SIMS measurements were carried out on an Atomika 6500-tool with Cs^+ or O_2^+ as primary ions. The primary energy was mostly 6,0 keV.
Fig 4.1 shows the SIMS profile of an epitaxial layer grown on an RCA-cleaned substrate. The oxygen and carbon spike visible at the interface to the substrate is taken as an indicator for residual oxygen, carbon, respectively. A flat oxygen, carbon trace is taken as an indicator for a perfect interface.

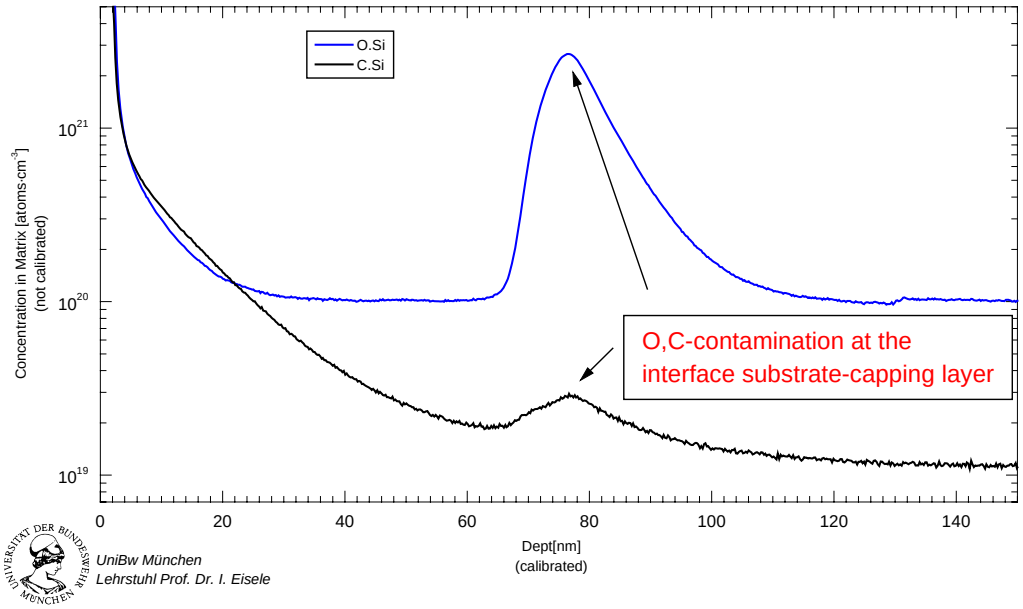

Fig. 4.1: SIMS depth-profile of a Si layer grown with LPCVD exhibiting O, C-impurities stemming from unsufficient substrate cleaning.

Besides contaminations doping profiles can be characterized by SIMS. Fig. 4.2 contains the SIMS-profile of a B doped Si layer stack. The layers have different B-concentrations. This “cascade” can be correlated with the diborane flow that was changed from 500 sccm to 200 sccm to 30 sccm to 0 sccm. The B signal is flat and only changing when the dopant gas flow is changed. This means that the entire layer deposition leads to homogenous doped layers from the substrate interface to the top. Calibrating the B signal with a reference sample as mentioned above, the total B-concentration may be derived.
It has to be mentioned that when a signal (e.g. for B) is dropping because the interface is reached (in Fig. 4.2 at ca. 400 nm), it’s not dropping very fast even if the underlying layer is not B-doped at all. The reason for this is that the beamed ions hit the B atoms and push them in the direction of the beam, in other words further into the substrate. This so called “knock-on” is especially strong for B because of the small atomic weight of this element.

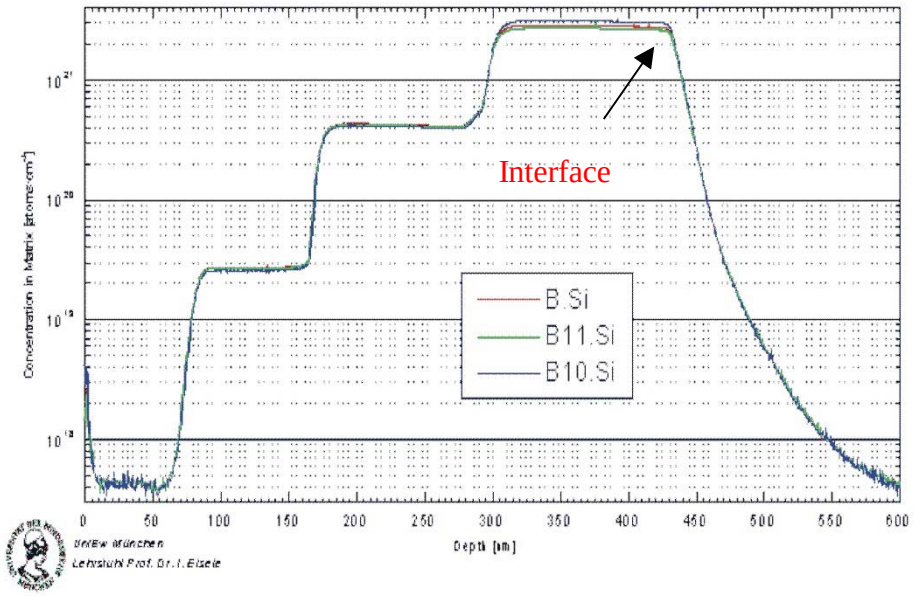

Fig. 4.2: SIMS depth-profile of a boron doped Si layer grown with LPCVD at a temperature of 775 °C.

The evaluation of dopant concentrations and layer thicknesses gets more complicated for doped $Si_{1-x}Ge_x$ –alloys. There are no reference samples with known dopant concentrations available for different $Si_{1-x}Ge_x$ –alloy compositions. Fig. 4.3 shows a SIMS depth-profile of a boron $Si_{1-x}Ge_x$ layer grown with the Applied Materials Centura LPCVD Epi system used in this work. The signals are flat over the thickness of the layer and abrupt at the interface. It may be derived that the layer is grown homogenously from the substrate interface to the top. More detailed descriptions of this method are found in [6,7].

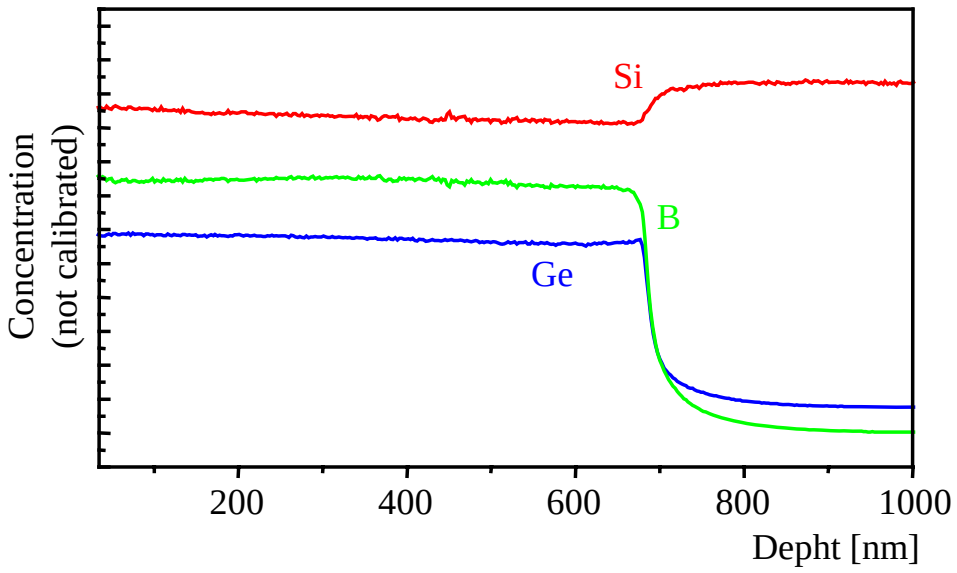

Fig. 4.3: SIMS depth-profile of a boron doped $Si_{1-x}Ge_x$ layer grown with LPCVD at a growth temperature of 775 °C.

4.3 Spectral Ellipsometry (SE)

Ellipsometry measures the change on the state of polarisation caused by reflection on the sample. If polarized light will be reflected on the boundary of two media, the state of polarisation of the reflected beam will change. This change is described by the complex Fresnel-reflection coefficients $\vec{r}_p$, $\vec{r}_s$.
Drude introduced the following terminology [8,9]:

$$\rho = \frac{\vec{r}_p}{\vec{r}_s} = \tan\Psi * \exp(i\Delta)$$

where $\vec{r}_p$, $\vec{r}_s$ are connected to the ellipsometric angles Ψ and Δ.
Tanψ is the ratio of the amplitudes and cosΔ is the phase difference between p- and s-wave induced by reflection.

Fig. 4.3.1 shows the schemata of a spectral ellipsometer [10]. The GESP-5 manufactured by Sopra GmbH used in this work uses a rotating polarizer and an analyzer thas is fixed during each measurement [11]. It may be noted that a geometry with a fixed polarizer and a rotating detector is also possible and used by other manufacturers. An image of the GESP-5 spectral ellipsometer used in this work is shown in Fig. 4.3.2.

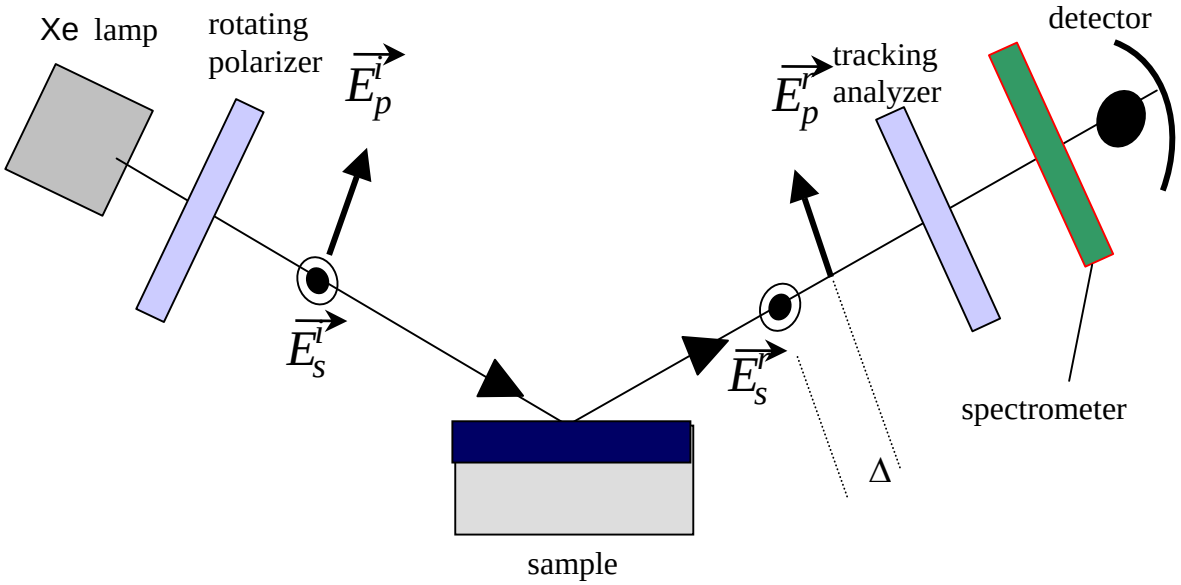

Fig. 4.3.1: Schemata of spectral ellipsometer with the rotating polarizer geometry used used in this work.

Fig. 4.3.2: Picture of the SOPRA GESP-5 spectral ellipsometer used in this work.

The determination of the physical parameters (layer thickness, alloy composition, interface roughness etc.) of the interesting sample out of the ellipsometric angles depends on three factors [12]:

- Accurate spectroscopic data, e.g. refractive index n and absorption coefficient k. Because the optical measurement is extremly surface sensitive, unwanted over-layer material stemming from the air like SiO_2 has to be recognized.

- An appropriate model for $\vec{r}_p$ and $\vec{r}_s$ represented in terms of the sample microstructure. These model contains refractive index n and absorption coefficient k of each layer. The Fresnel-reflection coefficients can than be calculated from Maxwell's equations via the dielectric function: $\varepsilon_1+\varepsilon_2 = (n+ik)^2$.

- The systematic determination of the values and confidence limits of the wavelength-independent parameters of the model with linear regression analysis. This provides mean square values and confidence limits on the physical values

themselves. The confidence limits provide information if the data are really determining parameter values. Therefore the use of too many parameters results in a drastic increase in confidence limits. So they provide a natural check against the tendency to add more and more parameters just to get a small mean square deviation.

The complex sytem of nonlinear differential equations that has to be solved provides only numerical solutions requiring a significant amount of computer power. This is the main reason why SE did not become attractive as a thin layer characterization tool until mid 1980's, despite the fact that the underlying theory's of Drude [8,9] and Maxwell are well known for more than a century.
This optical method is non-destructive, fast and cost-effective once the appropriate optical models are understood. These are the main reasons why SE is widely used as a line measurement tool in semiconductor manufacturing.
Detailed descriptions of the measurement technique are found in [11,12,15].

The most important applications in this work are:

1. The thickness measurement of dielectric layers, especially ultra thin silicon dioxide.

2. In MOS gate stacks the thickness measurement of a poly-electrode on an already measured silicon dioxide layer [11,15].

3. The capability for measuring alloy composition and layer thickness for structures such as $Si_{1-x}Ge_x$ on Si [13,14,16,18,20].

The measurement delivers two ellipsometric angles Ψ and Δ each wavelength. Each layer is characterized by the three parameters n refractive index, k absorption coefficient and thickness d. Hence the corresponding equation system contains more layer parameters than measured values:

$$M\left[\Psi(\lambda),\Delta(\lambda)\right] = L\left[(n_1(\lambda),k_1(\lambda),d_1),\ldots,(n_x(\lambda),k_x(\lambda),d_x),(n_{Substrate},k_{Substrate}))\right]$$

This means additional information whether on optical properties (n, k) or on layer thickness d are necessary. The substrate is always Si(100) throughout this work and the optical properties are well known from literature.

Application 1

There's only one layer and n, k of silicon dioxide, siliconnitride is well known. The problem symplifies to:

$$M\left[\Psi(\lambda),\Delta(\lambda)\right] = L\left[d\right]$$

The layer thickness d can be derived easily. However, for SiO_2 layers thinner than 2nm, the refraction index n may differ from the bulk value.

Application 2

The layer system is represented by an amorphous-/polysilicon layer with an underlying silicon dioxide layer already well known from application 1. The optical constants n, k for amorphous-/polysilicon are strongly depending on the deposition process giving the following problem:

$$M\left[\Psi(\lambda),\Delta(\lambda)\right] = L\left[(n_{a/p-Si}(\lambda), k_{A/P-Si}(\lambda), d_{A/P-Si}\right]$$

A possible solution is to measure the amorphous-/polysilicon layer thickness separately by another method like SEM, TEM (see chapter 4.4), GXR[1] or by patterning the layer lithographically. In the last case the appropriate etching process has to be selective to silicon dioxide. Then the layer thickness may be measured by mechanical stylus profiling (see chapter 4.1.2) and therefore the optical constants n(λ), k(λ) can be calculated from the ellipsometric angles. With known optical data n(λ), k(λ) for this specific amorphous-/polysilicon the next layer deposited with this process may be characterized easily.

Fig 4.3.3 shows n(λ) of Si in different states of crystallisation from 200-800 nm wavelength.

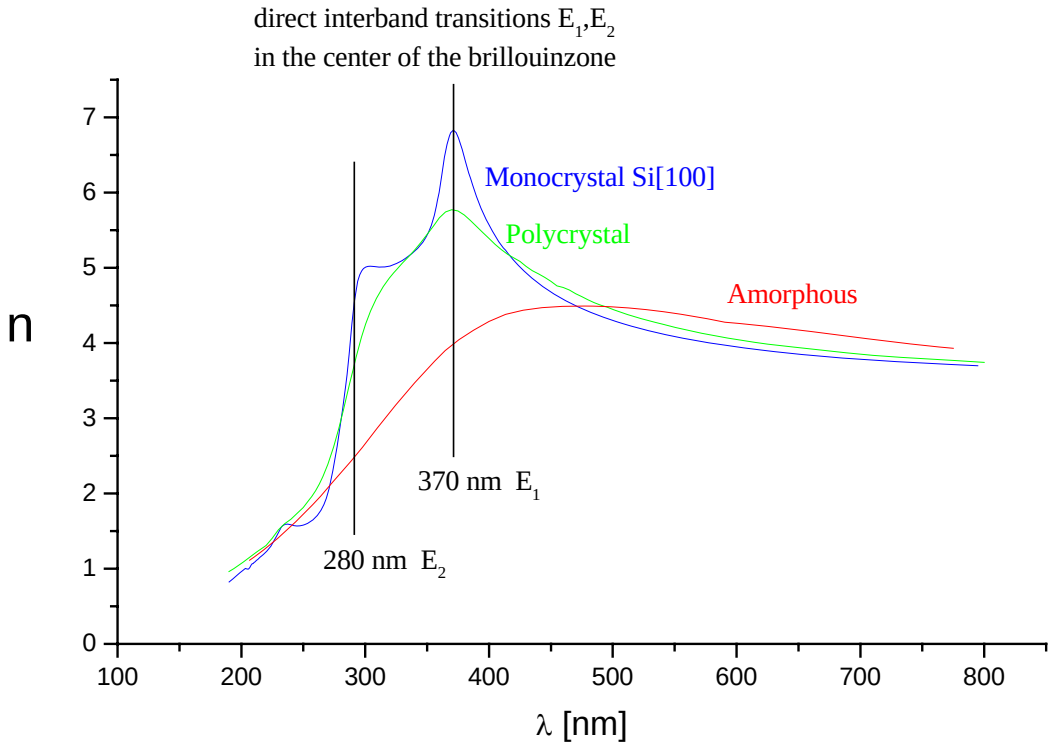

Fig. 4.3.3: Refractive index n of Si as a function of wavelength for different crystallization states. Blue: monocrystalline (epitaxial), green: polycrystalline, red: amorphous. After Sopra [11].

[1] Grazing Incidence X-Ray

For monocrystalline (epitaxial) Si the dispersion relation is dominated by two peaks at 280 and 370 nm, respectively. These are correlated to two direct interband transitions of the band structure of monocrystalline Si. They are normally called E1 (370 nm) and E2 (280nm) and are located in the center of the Brillouin zone. The dispersion for polycrystalline Si also shows peaks at the same wavelengths as monocrystalline Si. But their intensity is weaker depending on the structure (ratio crystalline phase/amorphous phase, grain size, surface roughness etc) of the film.
To evaluate the layer properties of a poly-Si film from spectral ellipsometric data is very complex and in most cases data from other measurement techniques have to be considered too [11,15]. The dispersion of the amorphous Si does not show any peaks corresponding to the lack of crystalline structure. An analysis of the measurent data for peaks corresponding to the E1, E2 transitions allows to decide about the crystallinity of the grown layer and to choose the appropriate dispersion relation. E.g. n(λ), k(λ) for amorphous Si if there are no peaks at all.

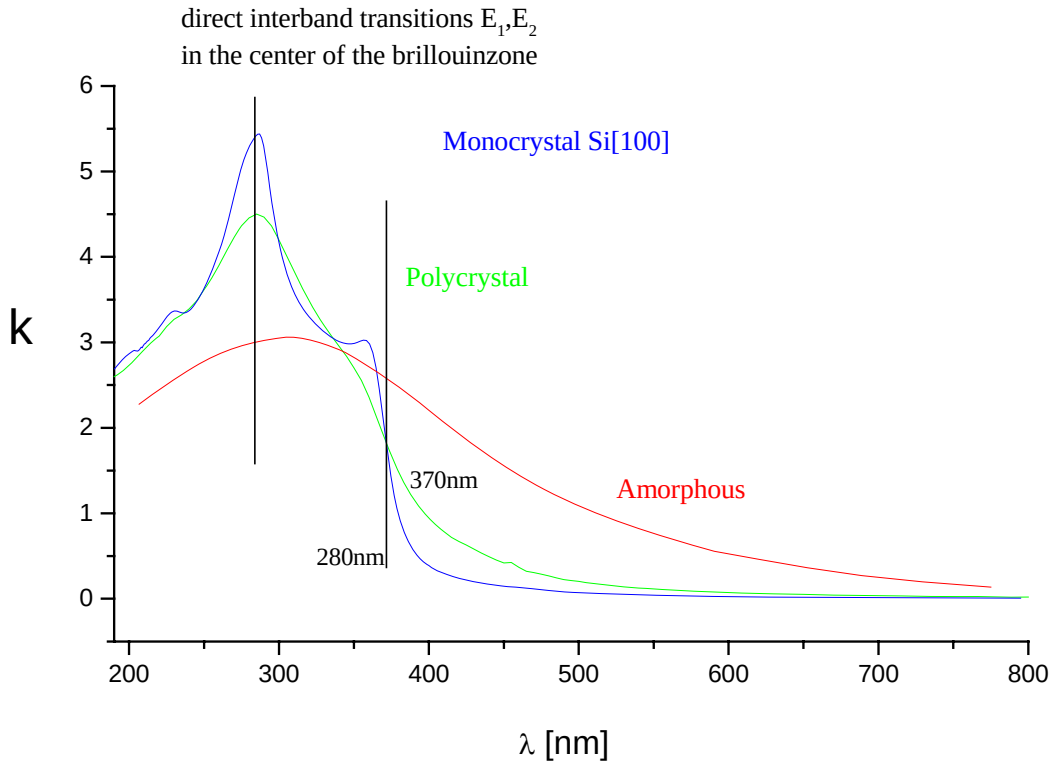

Fig. 4.3.4: Absorption coefficient k of Si as a function of wavelength for different crystallization states. Blue: monocrystalline (epitaxial), green: polycrystalline, red: amorphous. After Sopra [11].

A more sophisticated approach is the use of a dispersion model for n(λ), k(λ) that is fitted to the measured data. It is based on a Cauchy-approximation for the refraction index n together with three or four Lorentz-shaped peaks simulating the absorption k [11]. The

results were compared to the layer thicknesses gained from patterning the layers and measuring step heights with a mechanical stylus profiler. The agreement of the two methods was always within 2 nm.

Application 3

For measuring Ge content as well layer thickness for alloys such as $Si_{1-x}Ge_x$ on Si the situation is more complicated. n(λ), k(λ) are functions of Ge-content, strain and doping. Also native oxide and surface roughness have to be taken into account. For the first evaluations the dielectric functions derived by Pickering et al. are used as a reference [13,14]. In this work it is reported that the critical points of the dielectric functions are dependent on the Ge content as follows: E_1=3.393-1.335x+0.0365x^2, E_2=4.42-0.03x. Fig. 4.3.5 shows the refractive index n for different Ge concentrations.

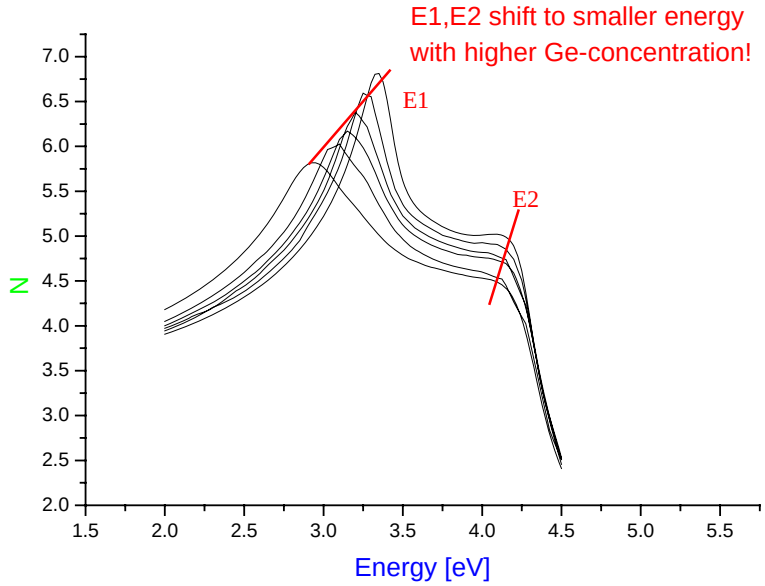

Fig. 4.3.5: Refractive index n of $Si_{1-x}Ge_x$ as a function of energy with different Ge content. After Pickering et al. [13,14].

Clearly the critical points shift to smaller energy with higher Ge content. From the measured ellipsometric angles the energy of the critical points can be derived and compared to the critical points in the reference dielectric functions. Then the two references with the critical points that best match the measured data are used for further fitting. This is done with an alloy-model used by Sopra GmbH [11] and first proposed by Aspnes [19]. The complete layer model includes substrate, alloy-model and native oxide. Ge concentration, $Si_{1-x}Ge_x$ and native oxide layer thickness are fit parameters. In principle, both alloy composition and layer thickness can be evaluated this way [20].
However, the reference dielectric functions are for intrinsic $Si_{1-x}Ge_x$ –layers and did not fit very good the heavily arsenic doped $Si_{1-x}Ge_x$ –layers examined in this work.

A possible solution is to measure the $Si_{1-x}Ge_x$–layer thickness separately by another method like SEM, TEM (see chapter 4.4), GXR or by patterning the layer lithographically. In the last case the appropriate etching process that is selective to silicon is used. Then the layer thickness may be measured by mechanical stylus profiling (see chapter 4.1.2) and the optical constants n(λ), k(λ) can be calculated from the ellipsometric angles. With known optical data n(λ), k(λ) for this specific $Si_{1-x}Ge_x$ –layer the Ge content may be evaluated much more easily with the alloy-model mentioned above. Repeating this procedure several times for different $Si_{1-x}Ge_x$ –alloys it is possible to generate an "alloy-library" for our specific $Si_{1-x}Ge_x$ –layers (see chapter 6.2).

4.4 Electron Microscopy

4.4.1 Scanning Electron Microscopy (SEM)

A focused beam of primary electrons is scanning across the sample. The electrons stem from field emission (very high resolution down to 1nm) or thermal emission of a cathode. Typical electron energies are 1-30 keV. The whole apparatus from cathode to sample is in vacuum to avoid diverging of the beam by collisions with gas molecules. The electrons are focused by electric and magnetic fields that are also used to scan the beam across the sample.

The impinging electrons are interacting with the electrons of the sample atoms, producing secondary electrons. These have a much smaller energy than the primary electrons and an escape depth of only some nanometers beneath the sample surface. This is the reason why their signal is used for building the image if the topography of the sample is interesting. They are drawn into the detector by an electric field and detected with a secondary-electron-multiplier and a photomultiplier. The final signal is modulating the brightness of the monitor synchronous to the position of the deflection current. Because all edges, walls and particles have a large surface, they produce a big amount of secondary electrons. Since electrons have a very small angle of aperture a very good depth resolution for topographic images is provided.

The images in this work are made by a Jeol JSM-6700 equipped with a field emitter providing a minimal possible resolution of 1nm. Fig. 4.4.1 shows a $Si_{0.8}Ge_{0.2}$ mesa with 200 nm thickness grown in the Applied Materials Centura Epi system. The process is selective with respect to silicon dioxide. The selectivity is confirmed because there is no deposition on the silicon dioxide detectable. The facets visible are stemming from the patterning process, because the resolution limit of the lithography equipment is 1 μm.

The electron beam transports a significant amount of electric charge to the sample. If there are isolating parts on the sample, e.g. a silicon wafer with a dielectric mask of silicon dioxide and/or nitride, the electrons cannot be transported away and build electrostatic charges on the sample surface. These are deflecting the electron beam making imaging very hard. The resolution drops significantly. The common approach to this problem is sputtering a thin film of conductive metal, e.g. Au or Pt on the surface. However, it has to

be mentioned, that material contrast like Si/SiO_2 or Si/SiGe is hard to detect below the metal film.

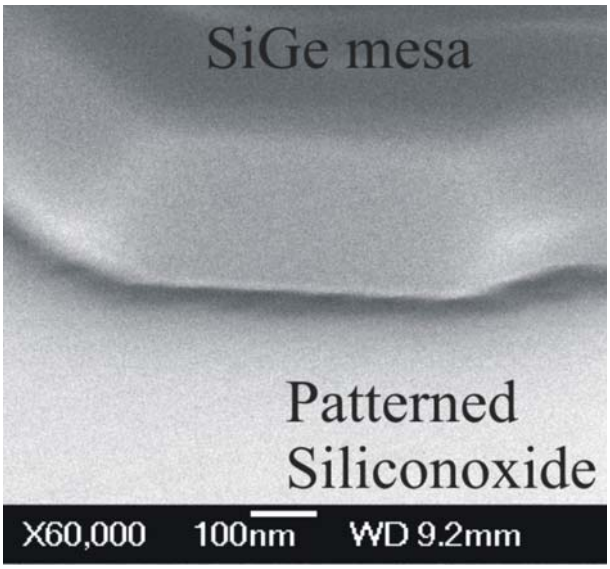

Fig. 4.4.1: SEM image of a selectively grown $Si_{0.8}Ge_{0.2}$ mesa with 200nm thickness.

4.4.2 Transmission Electron Microscopy (TEM)

A high energy electron beam is passed through a thinned sample (about 30 nm) and the diffraction pattern is detected. The wavelength of electrons with 200keV is 2.8 A°. So resolution on atomic scale is possible (high resolution TEM, HRTEM). The electrons are diffracted by the ordered atomic lattice of the crystal. The diffraction pattern behind the sample is symmetric according to the crystal lattice. Particularly, defects of the lattice like dislocations and precipitates can be detected indicating the quality of the grown crystal. Also the material contrast Si/SiGe and the interface SEG/oxide wall may be examined.
HRTEM gives the most detailed results on crystal quality but sample preparation and measurement is a considerable effort. Also it's a destructive technique.
The images in this work were made by Freescale Semiconductor Inc. Fig. 4.4.2 shows two high resolution TEM (HRTEM) images. Left hand side is a boron doped (8E19/cm3) layer which shows the ordered electron diffraction pattern of epitaxial silicon. No defects are visible, even the interface layer-substrate cannot be detected. Right hand side is a boron doped $Si_{75}Ge_{25}$–layer grown at 625 °C, with a resistivity of 0.6 mOhm cm. The ordered diffraction pattern of a crystal structure is visible. The contrast from the layer (dark) to the substrate (bright) stems from the germanium content (material contrast).

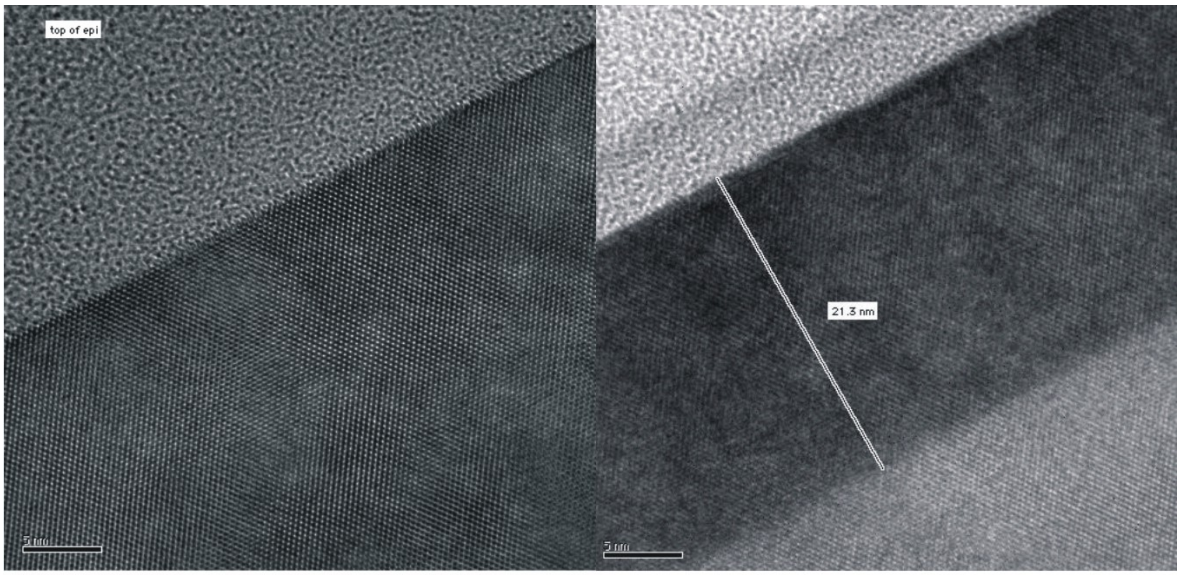

Fig. 4.4.2: TEM-images: left: Si:B 775 °C, see Fig. 4.1 (resistivity: 1.4 mOhm cm). Right: $Si_{75}Ge_{25}$:B 625 °C, see Fig. 2 (resistivity: 0.6 mOhm cm).

4.5 Characterization procedure for epitaxial layers on patterned substrates

The substrates were Si(100)-CZ-wafers with 100 mm diameter from Siltronic AG. The wafers were thermally oxidized (18nm) and patterned by a wet chemical etch with buffered HF according to the mask (100 mm ⊗ 100 mm) in fig. 4.5.1:

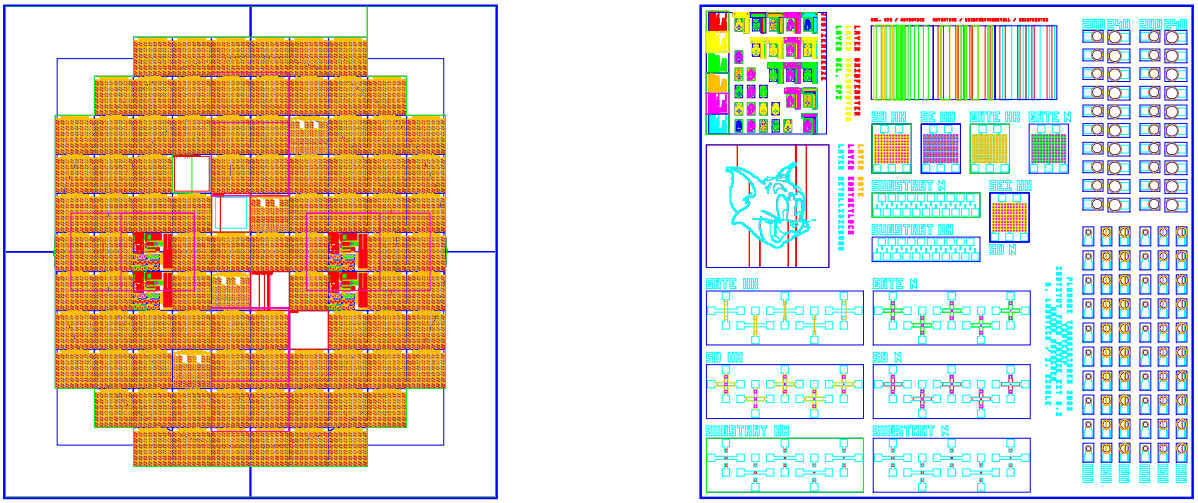

Fig.4.5.1: Test mask used for selective epitaxial growth.

The white squares are test windows. They are used for characterisation methods like SIMS, 4-pt-probe, spectral ellipsometry etc. The red squares are test chips plotted in detail on the right hand side. In the right lower corner of the test chip are circular shaped seed windows with a radius ranging from 100 μm^2 to 160 μm^2. These circular seed windows are used for all patterned wafers throughout this work, unless stated otherwise.
It is possible that the layer thicknesses as well as alloy compositions vary with the mask layout. This is the so called *loading effect.*

Evaluation of layer thicknesses:

The layers are deposited in seed windows surrounded by silicon dioxide. Fig. 4.5.2 shows a schematic cross section after deposition of a Si layer. The thickness of the epitaxial layer is given by: $d_{Epi} = d_{Poly} + d_{Ox} - d_{Stepheight}$. d_{Ox} is known from ellipsometric measurements. The step height $d_{Stepheight}$ can be measured with a mechanical stylus profiler or Atomic Force Microscopy. If there is no silicon nucleation visible on the oxide (selective deposition may be confirmed by optical microscopy, SEM, TEM)) then $d_{Poly} = 0$. If there is deposited silicon detectable on the oxide then d_{Poly} has to be evaluated by Spectral Ellipsometry (see chapter 4.3 and 8) and added to d_{Ox}.

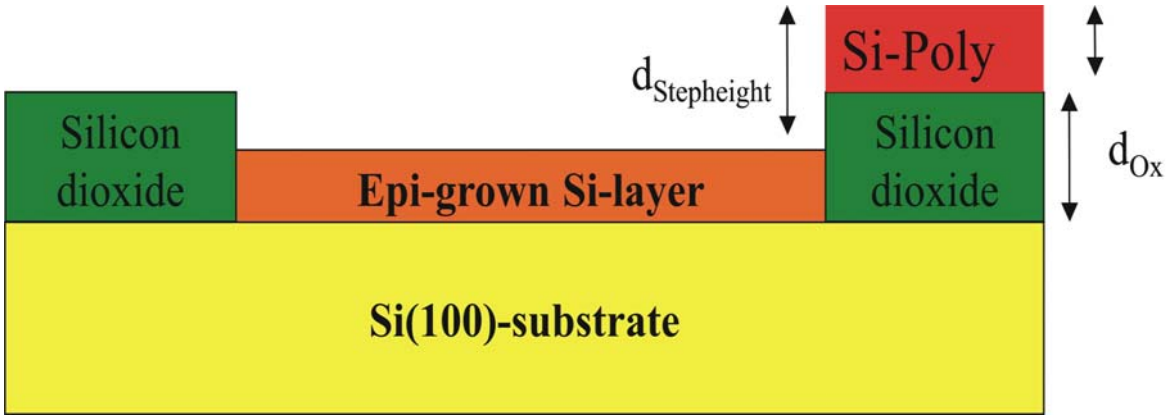

Fig.4.5.1: Schematic cross section of a seed window used for selective epitaxial growth.

To investigate homogeniety *(loading effect)* over the wafer, the thicknesses in the following windows were evaluated:

- Inner test window
- Outer test window
- 3 circles on the right side of each test chip, with 100, 160, 180 μm diameter respectively

5. Preepitaxial surface cleaning

For the growth of high-quality epitaxial layers atomically clean surfaces are essential. Contaminations on substrates prevent surface migration of adatoms and act as impurities and/or nucleation centers for defects. The most important are oxygen, carbon, boron and metal contaminants stemming from the air. Especially oxygen contamination leads to defect formation in the epi layer [1,2].
Chemical etching procedures used in concentional Si technology are necessary as the first step in substrate preparation. The two most common are called the RCA[1]-clean or standard clean (SC) and the HF-dip [2]. They will be shortly described in chapter 5.1. After insertion of the wafer into the reactor, oxide and carbon impurities will be removed by a heating step that is in Chemical Vapour Deposition normally supported by hydrogen ambient. Due to the continous trend to smaller device dimensions in silicon ULSI[2] dopant diffusion must be limited. This is especially true for boron-doping in p-MOSFET, because boron has a significantly higher diffusion coefficient than all n-type dopants. So processing with reduced thermal budget is necessary (see chapter 5.2). It was also suggested to remove oxygen, carbon by reductive species like silane [3,4,5] or germane [6]. Again reduced thermal budget is the motivation (see chapter 5.3).

5.1 Wet chemical Cleaning

The standard clean or RCA-clean consists of two steps [2,7]. First is a basic solution of $NH_4OH:H_2O_2:H_2O$ called SC-1, RCA-1 or Huang-A. The OH^--ions dissolve the natural oxide of the silicon wafer while the H_2O_2 reoxidates the bare silicon surface leading to a clean chemical silicon dioxide of 1 nm thickness. Because H_2O_2 oxidates all carbon impurities these will be removed from the wafer surface. Also the reaction underoxidates particles and dissolves them into the basic solution.
The second step consists of an acid solution of $HCL:H_2O_2:H_2O$ called SC-2, RCA-2 or Huang-B. It's main purpose is the removal of metal impurities. It does not attack the chemical oxide stemming from SC-1, so this remains as a protective layer on the silicon surface until insertion in the growth enviroment.
Hydrogen surface passivation is achieved using conventional diluted HF-etching of SiO_2 [8,9]. The HF-concentration in water is normally under 1% because otherwise surface roughness and carbon contamination are getting stronger. The chemical aggressive HF must be rinsed away before handling the wafer. The final rinse with DI-water is not perfect because it is known to remove a part of the hydrogen passivation leading to some recontamination of the wafer surface. It was also suggested to use isopropyl-alcohol (IPA) for the final rinse due to smaller surface roughness [10]. Drying is also easier than for DI-water due to the volatile nature of the alcoholes. The so-called "Marangoni-dry" consisting of IPA-steam/N_2 is established.

[1] Radio Corporation of America
[2] Ultra Large Scale Integration

5.2 Preepitaxial Hydrogen Bake and Thermal Desorption

As mentioned above, dopant diffusion must be limited especially for boron-doping in p-MOSFET. So processing with reduced thermal budget is necessary.
We investigated the minimum thermal budget to achieve contamination-free silicon surfaces for expitaxy. Process parameters varied are temperature (steady-state-boundary) and time (kinetic limitations). Results are compared to published results of [11-18] and the role of hydrogen in the removal of oxygen as well as carbon impurities is discussed.

The hydrogen from Linde AG is delivered with 5.0 N-purity and was passed through a point-of-use-purifier from Mykrolis which reduces oxgen and moisture levels down to 1ppm. Some experiments were performed without further purifying. The hydrogen flux during substrate cleaning was always set to 10 slm unless stated otherwise. After cleaning procedure a Si capping layer was deposited at 775 °C using dichlorosilane. To estimate the partial pressure of oxygen in the reactor enviroment the leakage was measured and partial pressure of oxygen $P(O_2)$ derived as stated in chapter 3.6.1.
Substrates used were Cz Si(100)-wafers with n-type-doping of 2 mΩ cm resistivity from Siltronic AG. The wafers were RCA cleaned and inserted into the reactor. Some samples were dipped in an HF/H_2O solution of 1/100 prior to insertion into the reactor.

Results & Discussion

Fig 5.1 contains the SIMS-profile of two epitaxial layers grown on RCA-cleaned substrates after 10 min and 20 min hydrogen bake at 850 °C. The oxygen spike visible at the interface of the sample baked for 10min is taken as an indicator for residual oxygen. A flat oxygen trace is taken as an indicator for an oxide-free interface.

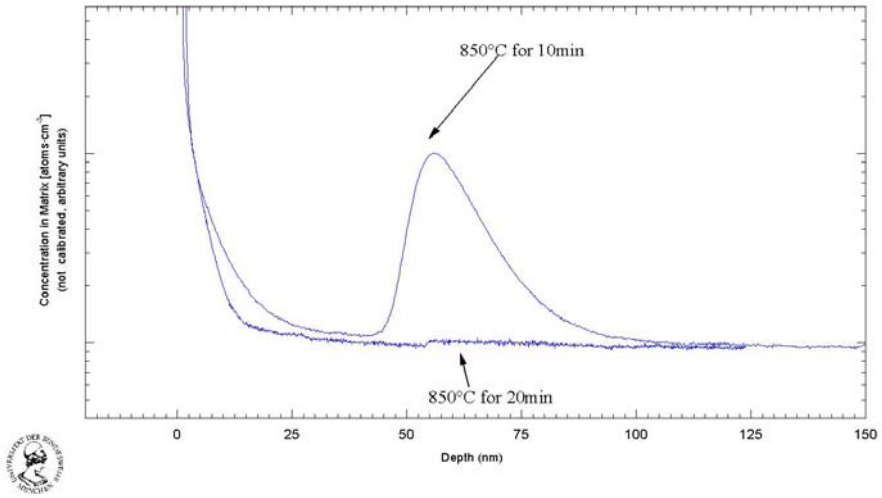

Fig.5.1: SIMS analysis of oxygen in epitaxial films deposited on samples which were prebaked 10 min, 20 min at 850 °C in a hydrogen athmosphere

At this point it may be mentioned that optical microscopy always showed hazy surfaces for samples which also showed an oxygen spike in SIMS. This can be correlated to a high defect density in the epitaxial layers. Samples without oxygen signals always showed specular surfaces indicating epitaxial layers with low defect density.
Fig 5.2 shows results compared to the steady-state boundary of F.W. Smith, G. Ghindini under UHV-conditions (SSVB) [12], J.J. Lander, J. Morrison [15] and T. Sedgwick at one atmosphere H_2 (SSAPB) [13,14]. The oxygen pressure for the AMAT Centura Epi system is derived according to the procedure stated in chapter 3.7.

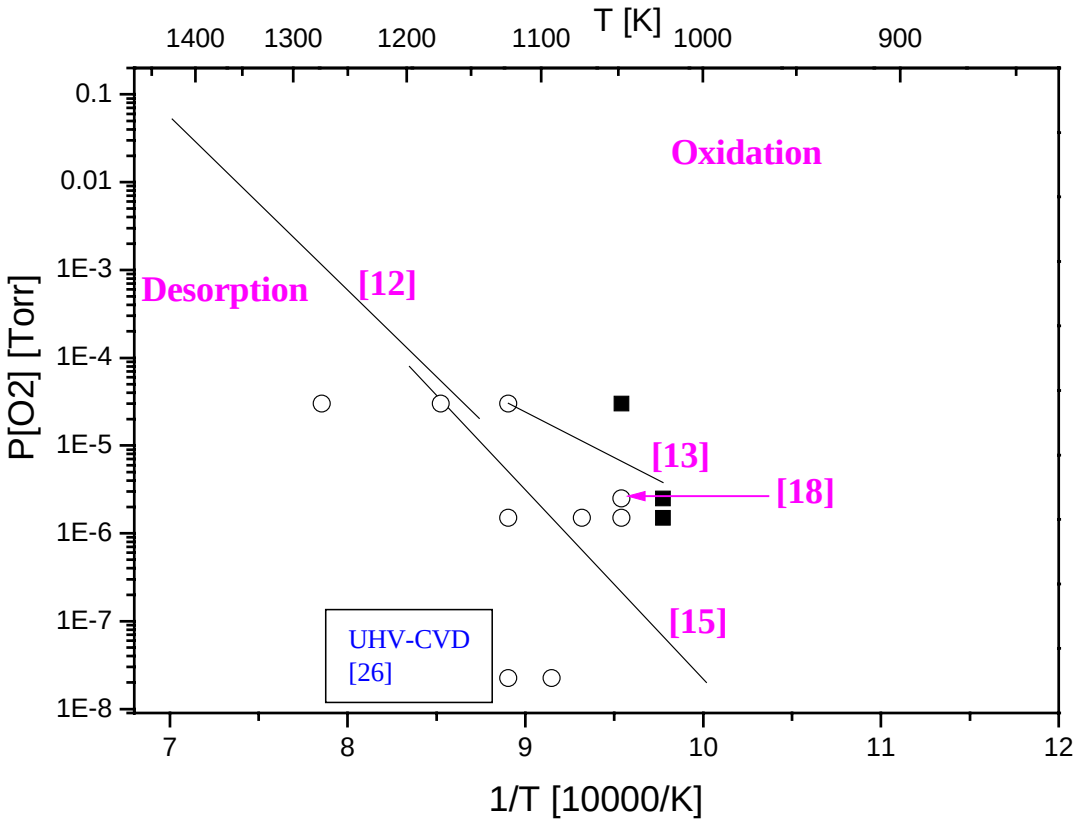

Fig.5.2: Boundary between region of oxide-free (open circles) and oxidized silicon surface (solid rectangles) as a function of temperature and oxygen concentration for a 10 Torr hydrogen gas ambient. The lines are the steady-state-boundaries of Smith, Ghindini [12], Lander, Morrison [15] for UHV-conditions and Agnello, Sedgwick [13] for APCVD in hydrogen. [18] is the work of Abbadie et al. on an AMAT Centura Epi System.

All results imply a less stringent boundary for desoxidation in hydrogen athmosphere than in UHV. Agnello and Sedgwick investigated oxidation/desoxidation for hydrogen athmospheric pressure in a CVD-reactor [13]. They also found a less stringent boundary for desoxidation.

They discussed the following possible causes:

- Oxide transport in the boundary layer due to diffusion in the carrier gas (hydrogen) may lead to a smaller oxygen partial pressure on the silicon surface for 760 Torr hydrogen pressure. However, the diffusion coefficient is inversely proportional to the process pressure. This means for 10 Torr of hydrogen the diffusion is a factor 76 stronger than for Agnello's APCVD experiments.

- Hydrogen ambient leads to an incubation time for the oxidation of (100)-silicon surfaces [14]. This means a slower velocity of the oxidation reaction. Because the desorption reaction is not altered the steady-state boundary for achieving oxide free surfaces may be shifted to lower temperatures and/or higher oxygen partial pressures.

However, hydrogen may play a role in the reaction kinetics of oxide removal. In another experiment a thermally oxidized wafer with an oxide thickness of around 7.3 nm as measured by spectral ellipsometry was annealed for 100 minutes under 10 Torr hydrogen athmosphere. The temperature was set to 900 °C. The oxide thickness was also measured after the annealing process and found to be 6.4 nm. Regarding a measurement uncertainty of 1 nm, the maximum possible thickness reduction is not more than 3 nm in 100minutes. The 5 min cleaning step at 900 °C removes 1 nm of silicon dioxide within 5 minutes.
This implies that hydrogen-etching of the 1 nm thick silicon dioxide may be ruled out as the main reaction of a 5 min cleaning step at 900 °C.

Another approach to this question is performing annealing experiments in inert gas enviroment. Noble gases are predestinated for this purpose because of the very low reactivity in the temperature range of 900 °C - 1100 °C.
Ludsteck et al. [19] published silicon dioxide growth experiments in an argon/oxygen mixture of 1 atmosphere pressure. The reactor was a commercially avaible RTP[1]-System manufactured by Mattson Thermal Products GmbH. Three different reactions were considered as follows:

(1) $Si + O_2$ (diff) = SiO_2 (activation energy: 2.9 eV); this is equal to the well known Deal-Grove-regime [20] and causes SiO_2 growth.

(2) Si(diff) + O_2 = SiO_2 (activation energy: 4.0 eV); the diffusion of silicon atoms from the interface to the surface may also lead to SiO_2 growth, particularly if the oxygen partial pressure is very low.

(3) At high temperature and very low oxygen partial pressure the diffusion of silicon atoms may also lead to oxide desorption: Si(diff) + SiO_2 = 2SiO. SiO has a much higher steam pressure than Si or SiO_2 and will dissappear from the wafer surface.

[1] Rapid Thermal Processing

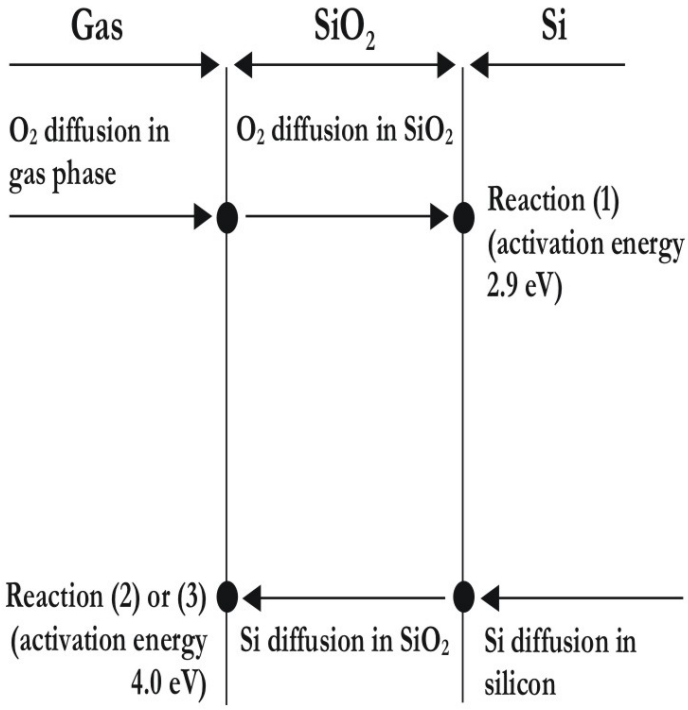

Fig.5.3: Model with three possible reactions for growth and desoxidation of a very thin oxide.

The third process is the widely accepted reaction for thermal desorption discussed by [12], but it is important to note that Smith, Ghindini did not discuss silicon atom diffusion through silicon dioxide. In case of oxide films with 1-3 nm thickness covering the whole substrate surface the necessary silicon for reaction (3) has to come from the bulk by diffusion. Because diffusion is always a process enhanced by temperature and time the model may also deliver a possible explanation for the above mentioned time limit for removing a chemical oxide. The exact mechanism of thermal desorption was investigated by several other authors [21]. Tromp et al. [21] reported the removal of SiO_2 from the Si(100)-surface by the formation and lateral growth of holes in the SiO_2, while the surrounding SiO_2 retains its initial thickness. Surface diffusion of Si inside the holes supplies Si for reaction with SiO_2 at the Si/SiO_2-interface, so that volatile SiO may be formed ("island etching"). This inhomogenous Si consumption leads to surface roughening. An important consequence of this may be enhanced defect generation due to lattice misfit relaxation in $Si/Si_{1x}Ge_x$-hetero- structures (see chapter 6.2). Tromp's results also imply that defects play a significant role in thermal decomposition of SiO_2. Raider [22] relates the initial inhomogenous stage of thermal SiO_2 desorption to carbon impurities.

The above results obtained from cleaning in noble gas enviroment may be compared to the results obtained from cleaning in hydrogen ambient. Fig. 5.4 contains both results and the steady-state boundaries of Smith, Ghindini [12], Lander, Morrison [15] and Agnello,

Sedgwick [13]. Sedgwick also discussed cleaning under argon atmosphere. His result is also depicted in the figure 5.4. Good agreement can be seen between all results. This implies that within the investigated process parameters (T,P) the well known reaction path $Si + SiO_2 = 2SiO$ may be fundamental for silicon substrate cleaning under hydrogen, argon and UHV ambient.

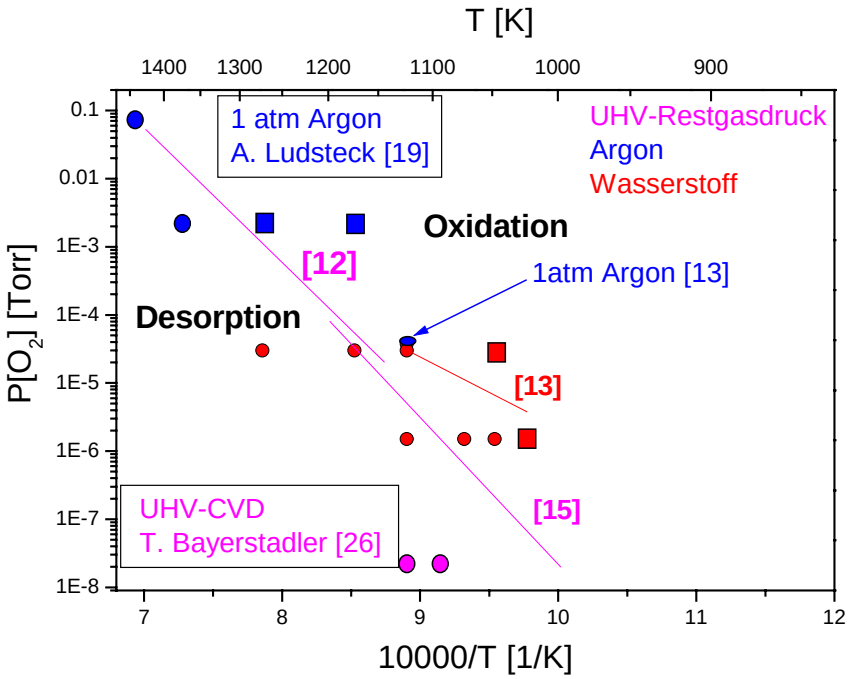

Fig. 5.4: Boundary between region of oxide-free (circles) and oxidized silicon surface (rectangles) as a function of temperature and oxygen concentration for a 10 Torr hydrogen gas ambient.

Carbon contamination

In all above mentioned SIMS-profiles the carbon-related signal behaved in the same manner as the oxygen-related signal, this means, with every oxygen-peak a carbon-peak could be detected. This rises the question whether C is removed by thermal desorption, or by chemical reactions with hydrogen as process gas.

Fig. 5.5 shows the O, C-profile of a silicon layer grown after a 5 min 900 °C bake measured by SIMS. Gas fluxes were turned off during prebake and the chamber was pumped down to a base pressure of 10 mTorr.

A strong carbon contamination is visible while no oxygen related signal can be detected. This result implies that hydrogen plays a crucial role in removing carbon contaminations from substrate surfaces prior to epitaxy. The ability of hydrogen to react with carbon

compounds to hydrocarbons which leave the silicon surface is already mentioned by [23,24].

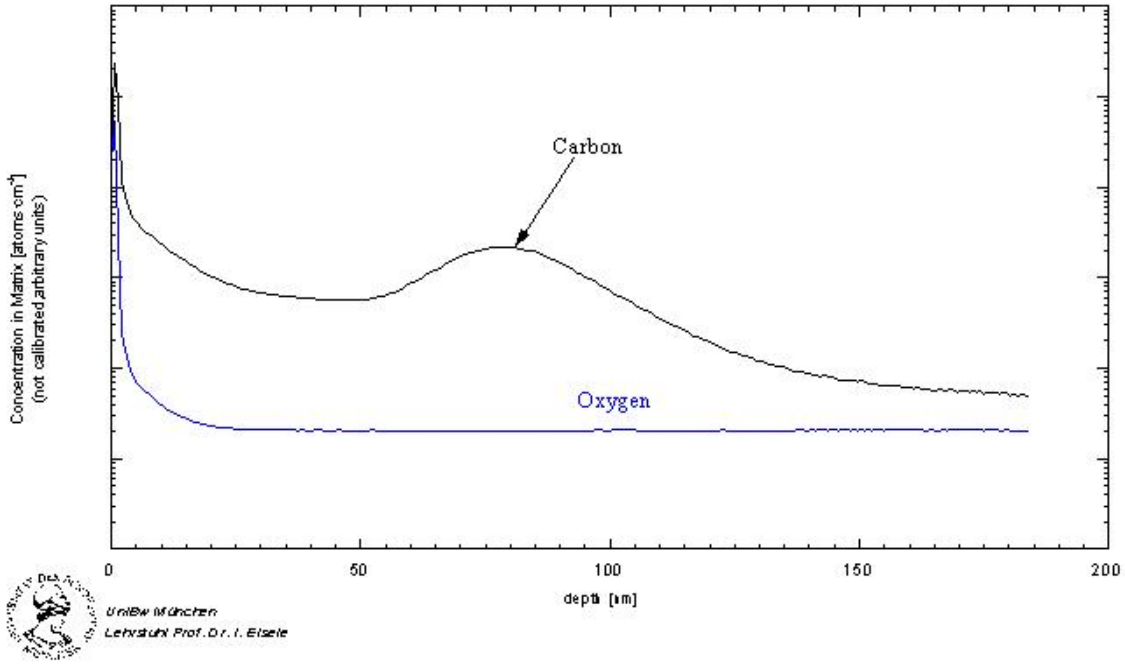

Fig. 5.5: SIMS analysis of oxygen, carbon in an epitaxial film deposited on a sample which was RCA-cleaned and prebaked in 10 mTorr reactor pressure.

A final experiment on a silicon substrate was performed in 3 steps:

1. annealing at 10 mTorr for 300 s (thermal desorption exactly like above).
2. Immediately after that another prebake at 900 °C for 5 min with 10 Torr hydrogen atmosphere (hydrogen bake).
3. Depositing an epitaxial silicon capping layer.

SIMS analysis showed no oxygen signal but a strong carbon spike at the interface. From the above discussion we know that after step 1 and 3 a carbon spike is detected at the interface. If steps 2, 3 are performed no carbon contamination can be detected. These results imply that the hydrogen bake of step 2 cannot remove all carbon impurities if step 1 was performed before.
A possible explanation is delivered by Stimpel et al. [25]. The author investigated that SiC is generated if carbon impurities on a silicon (100) surface are annealed over 700 °C. These SiC compounds are known remain stable in the temperature range from 700 - 1200 °C. In other words during step 1 SiC is generated on the surface. Step 2 cannot remove these SiC compounds because they are to stable.

Conclusion

In summary the minimum thermal budget to achieve contamination-free silicon surfaces prior to expitaxy could be estimated in a commercial LPCVD-system. For silicon dioxide removal <= 900 °C temperature and oxygen pressure are the most relevant factors what is also the case for cleaning under UHV conditions. From the above results one may conclude that within these process parameters (T,P(O_2)) the well known reaction path Si + SiO_2 = 2SiO may be fundamental for silicon substrate cleaning under hydrogen, argon and UHV ambient. So etching of the 1 nm thick silicon dioxide by hydrogen can be ruled out as the main reaction of a 5 min cleaning step at 900 °C. For the removal of very thin chemical oxides the diffusion of silicon atoms through the silicon dioxide cannot be neglected. The presence of hydrogen in the growth enviroment leads to a shift in the steady-state-boundary for achieving oxide free silicon (100) surfaces to less stringent requirements. Hydrogen is also responsible for a complete removal of carbon impurities.

5.3 Desoxidizing Precursors

As reference the standard thermal desorption under 10 Torr H_2 at 900 °C for 5 min mentioned in chapter 5.2 is used. Additionally several publications on SiH_4-assisted bake [3,26] and GeH_4-assisted bake [6] are used for comparison.
We repeat from chapter 5.2:

- Hydrogen bake at T<=900 °C is equal to a thermal desorption under real inert-gas or UHV conditions.

- For removal of carbon hydrogen must be present in the process ambient.

- Any time delay between cleaning and epitaxial growth must be avoided to avoid re-contamination (for the LP-CVD regime of Centura this also means that the process gases must be as clean as possible and that the growth temperature should be equal to the cleaning temperature). However, recontamination is rendered by hydrogen atmosphere during an incubation time as was investigated by Sedgwick et al. [27]. This incubation time is a function of oxygen partial pressure and substrate temperature.

- The lower the oxygen partial pressure from process gas impurities, the lower the minimal temperature required for thermal desorption (see chapter 5.2).

It is also important to note:

- Process gases silane (SiH_4), disilane (Si_2H_6), or germane (GeH_4) are best sources for SiO_2 removing species. Due to the thermal induced cracking of these molecules at the sample surface the etchants hydrogen, silicon, and germanium can be set free

for an silicon or germanium assisted SiO_2 removal as well as a hydrogen assisted carbon removal under LPCVD conditions.

- The more stringent the low-temperature cleaning requirements are, the smaller the thermal dissociation energy of the used cleaning gas has to be. (Si_2H_6 and GeH_4 have significantly smaller thermal dissociation energies compared to SiH_4.)

5.3.1 Silane (SiH_4)

A SiH_4 assisted low-temperature thermal desorption under inert-gas (UHV / H_2) conditions for LPCVD growth is definitively possible down to cleaning temperatures of 700 °C if SiH_4 partial pressure is not higher than 10^{-3} mbar [26].
Murota et al.[3] demonstrated SiH_4-assisted substrate cleaning followed by defect-free epitaxial growth in an ultrapure CVD-system. This is equipped with gas purifiers and load-lock like the AMAT Centura Epi System but has a much smaller leakage (several orders of magnitude) leading to a respectively lower oxygen background level. This is probably the main reason why Murota could achieve fully selective silicon-epi without clorinated precursors. The process parameters reported for the cleaning step are 650 °C - 750 °C temperature and a silane partial pressure of around 10^{-3} mbar. This is comparable to the also succesful cleaning step in UHV-CVD reported by [26].
However, this process is not self-limiting, the end of impurity reducing and the beginning of epi-growth cannot be distinguished.

A silane-assisted desorption step in AMAT-Centura has to fulfill the following requirements:

- Meeting the partial oxygen pressure boundary for thermal desorption.
- Full selectivity to oxide, because otherwise undesired poly-growth will occur instead of reducing the oxide.
- Full selectivity to oxide means very stringent requirements to reactor impurities like moisture and oxygen [3,13,14,24,27] and a low silane partial pressure <= 10^{-3} mbar [3,26]. This is probably the main reason why Murota could achieve fully selective silicon-epi without clorinated precursors [3].

From the above discussion it is clear that oxygen partial pressure plays a key role for the minimum temperature that allows substrate cleaning prior to low-defect epitaxy.

- The oxygen partial pressure renders oxide desorption and enhances reoxidation for temperatures <= 750 °C in the AMAT Centura Epi System. Hence cleaning temperature for thermal desorption cannot be lowered below 750 °C.

- The impurity background pressure in the AMAT Centura Epi System is very high compared to UHV-CVD reactors [26] and/or the ultraclean reactor system used by Murota et al.[3]. This may be one reason why a silane based selective process and hence a silane-assisted cleaning step cannot be defined until now.

- This also renders selective epitaxial growth with disilane.

Another reason rendering the development of a silane-based cleaning process is the MFC-configuration of the AMAT Centura Epi System not allowing silane partial pressures < $5*10^{-2}$ Torr. This may be overcome by replacing the MFC with a smaller one.

5.3.2 Germane (GeH_4)

The main differences between a GeH_4–assisted precleaning step and a SiH_4-assisted are:

- Meeting the boundary for thermal desorption may be easier than for silane because germanium oxides from oxygen impurities are not stable at process temperatures >500 °C.

- Selectivity to SiO_2 is already achieved.

- GeH_4 reduces SiO_2 which is reported in literature [6,28].

- No growth of germanium on the bare silicon surface; this may be difficult because of the high reactivity of GeH_4 on Si(100)-surfaces [29].

The following recipe was used for a first experiment:

- Wet-chemical standard clean (RCA) forming a chemical oxide (thickness 1 nm), introducing into reactor.
- Heating up the sample to 700 °C under inert-gas (P_{total} = 5 Torr, 6/0.5 slm H_2) for 60 s.
- Switching on a GeH_4 flow of 5 sccm GeH_4/H_2 for 120 s.
- Depositing a cap layer of silicon to protect the interface until SIMS-measurements are performed.

Layers were always hazy und showed O,C,N-related signals in SIMS-measurements indicating insufficient cleaning. This may be the reason for the unsufficient interface cleaning. To investigate this in more detail preclean experiments with a temperature of 750 °C were performed. For evaluating the preclean quality a cap layer was grown after the following standard recipe:

- Total chamber pressure: 10 Torr, total growth temperature 750 °C.
- 16/1slm H_2, 100 sccm DCS, 100 sccm B_2H_6.
- Deposition time was 600 s.

With the standard hydrogen bake at 900 °C, 10 Torr for 300 s this cap layer may be used as a reference with the following properties: 120 nm film thickness, 140 Ohm/square sheet resistance. Surfaces are mirror-like indicating low defect densities.
For comparison of the same process performed on GeH_4 haze and sheet resistances of the grown layers were evaluated. Tab 5.1 shows the corresponding sheet resistances [Ohm/square] and haze for several different germane assisted cleaning processes:

	10 Torr,12/0 slm H_2	5 Torr,12/0 slm H_2	10 Torr,6/0.5 slm H_2	5 Torr,6/0.5 slm H_2
Haze	yes	yes	yes	strong haze
Sheet.Res.	155	155	155	175

Tab. 5.1: Haze and sheet resistance [Ohm/square] for a defined Si:B cap layer grown on a silicon substrate precleaned with GeH_4-assistance at 750 °C

All samples show haze indicating defect generation. In addition sheet resistances are slightly higher than for the standard precleaned reference.

There are several reasons possible for defects stemming from the interface:

- Insufficient removal of oxide and carbon.

- Growth of germanium islands on the bare silicon surface. This may be due to the higher cleaning temperature of 750 °C.

- Breakdown of GeH_4 selectivity to the oxide. If this happens before the oxide is totally reduced, remaining oxide islands may be overgrown by germanium. This may also be caused by the higher leakage rate because oxygen and moisture always render selectivity.

Further SIMS-measurements are needed to clarify this point.

6. P-type doping

In the last years, there was considerable interest in the selective growth of $Si_{1-x}Ge_x$-structures with p-type doping for source/drain-extensions in CMOS technology [1,2]. The aggressive downscaling of CMOS puts stringent requirements on doping shallowness and abruptness of source/drain-junctions. Increasing use of strain engineering for enhanced hole/electron mobilities in CMOS requires reduced thermal budget for the metastable $Si_{1-x}Ge_x$-structures to avoid lattice relaxation induced defect generation. The existing implanted profiles require a high-temperature thermal anneal. This thermal budget is also closely connected with boron outdiffusion. Selective epitaxy provides a method to deposit Si/ $Si_{1-x}Ge_x$ source/drain-junctions with heavy doping and low thermal budget. In most studies B_2H_6 served as dopant precursor [1-6]. Several authors reported the influence of the mask layout on deposition (loading effects) [6-9].
The major target of the present work was the development of a selective LPCVD[1] epitaxy process for the fabrication of highly-doped source / drain extensions for CMOS transistor technology. The specifications are as follows:

1. Process temperature <= 750 °C, resistivity <1 mΩ cm, thickness 15-20 nm.
2. Cross-wafer uniformity < 20%.
3. Selectivity versus SiO_2, measured by optical microscopy and TEM.
4. Germanium concentration between 20-30%.

6.1 Selective growth of highly boron-doped silicon

The research was started with the development of a selective dichlorosilane based CVD process. The process parameter space for all samples was:

- Ex-situ wet-chemical standard cleaning (RCA).
- In-situ thermal desorption for t = 300 s at T_S = 900 °C (10 Torr total chamber pressure) in H_2.
- Process pressure: 10 Torr, process temperature: 625-850 °C.
- 16/1 slm H_2, 100 sccm DCS.
- Flow of B_2H_6 from 0 - 500 sccm. The concentration is 500 ppm in hydrogen.

Fig. 6.1.1 shows the corresponding areal deposition rates for a B_2H_6 flow of 200 sccm. Clearly the growth regime shows an Arrhenius type behaviour and is therefore kinetically limited. The activation energy is found to be 44 kcal/mol for DCS/ B_2H_6-related silicon growth. The deposition rate for DCS related silicon epitaxy is connected to hydrogen desorption from the growing surface as rate-limiting step. Sinniah [10] reported an activation energy of 47 kcal/mol for hydrogen desorption from a Si(100)-surface. This may imply that the DCS/ B_2H_6-system follows the same rate-limiting step.

[1] Low Pressure Chemical Vapour Deposition

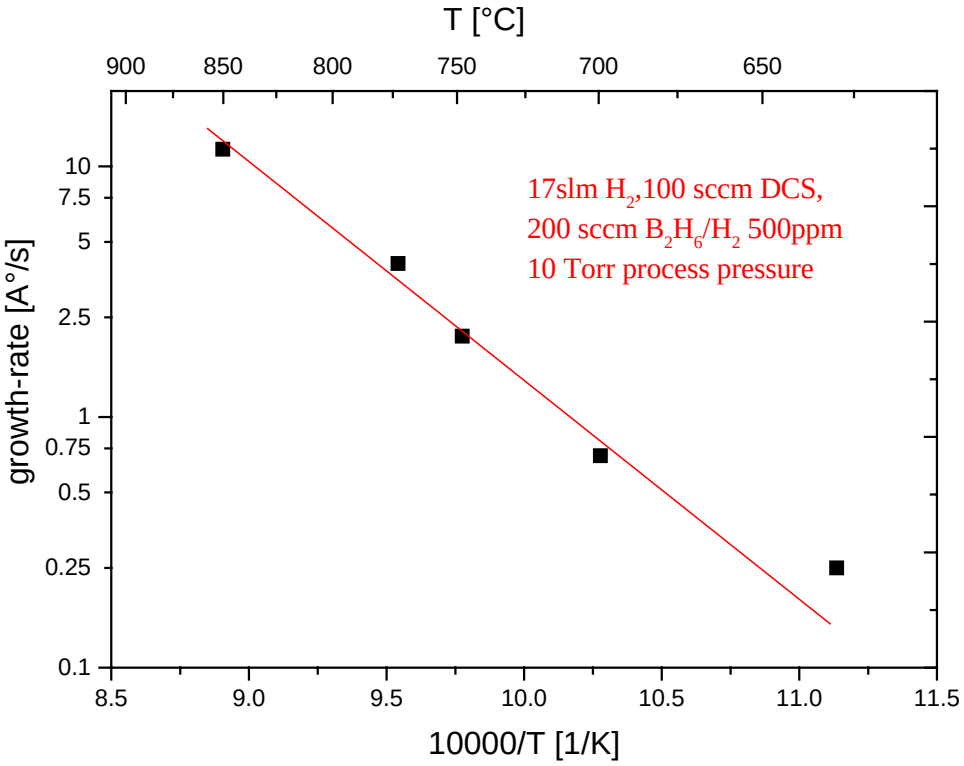

Fig. 6.1.1: Growth rate vs. growth temperature for a DCS/ B_2H_6 process.

Doping profiles and resistivity

Fig. 6.1.2 shows the SIMS-profile for the epitaxial silicon layer grown at 775 °C shown above:

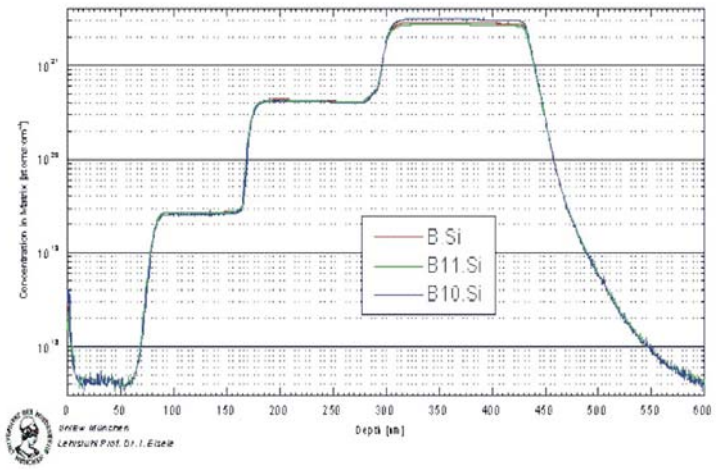

Fig. 6.1.2: SIMS-profile of boron-doped Si-Epi-layer, grown with DCS and B_2H_6.

Boron incorporation decreases from $3*10^{21}/cm^3$ down to the resolution limit if diborane flux is switched from 500-200-30-0 sccm. It can be seen that the transitions are sharp with

< 10 nm/decade. Nevertheless all surfaces are specular indicating no defect generation due to the very high doping-levels.
Fig. 6.1.3. shows SIMS-profiles for epitaxial silicon layers grown at 750 °C with 10 Torr process pressure (ss Fig. 6.1.1). Deposition time was 600 s. From measuring the SIMS-craters with a mechanical stylus profiler a growth rate of 0.21 nm/s could be evaluated. This seems to be constant for different diborane-fluxes within the process parameters investigated.

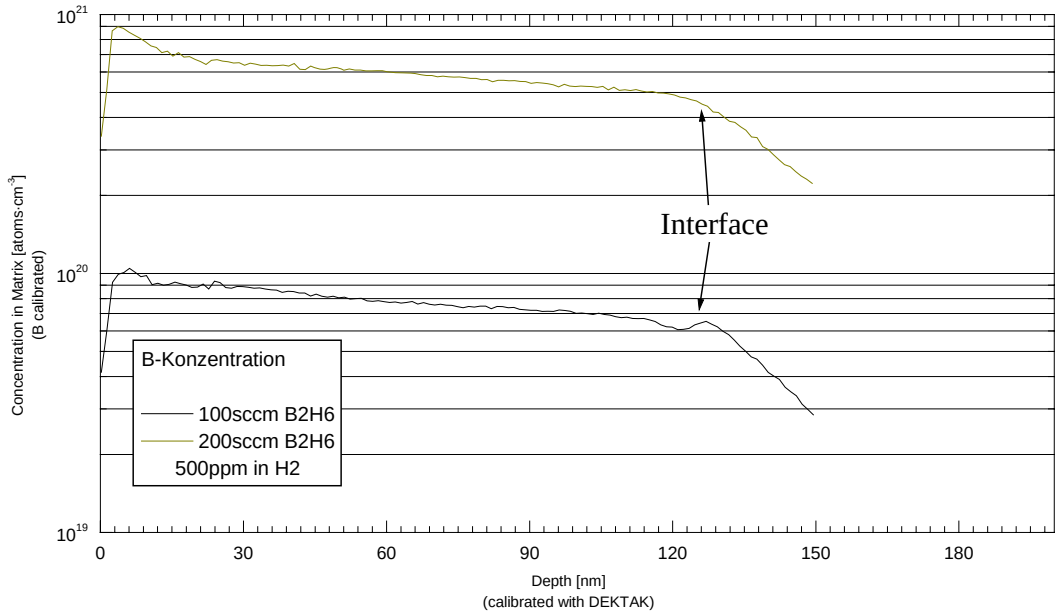

Fig. 6.1.3: SIMS-profiles of boron-doped Si-Epi-layers grown at 750 °C with DCS and B_2H_6.

However boron-incorporation rises up to $6*10^{20}/cm^3$ if diborane-flux is switched from 100 sccm to 200 sccm. Nevertheless surfaces are specular indicating no strong defect-generation due to the very high doping-level.
From 4-pt-probe measurements the specific resistivities were derived as 1,80 and 0,80 mΩ cm, respectively.
The latter resistivity value is the lowest published for epitaxial grown boron-doped silicon to the best of the author's knowledge.

Selectivity

To investigate selectivity and loading effects we used wafers with patterned oxide as described in chapter 4. The same processes as depicted in Fig. 6.1.1 were performed. No nucleation on the oxide mask could be detected showing full selectivity of the processes up to a layer thickness of 50 nm. Fig. 6.1.4 shows the TEM cross section of heavily boron

doped Si grown at a temperature of 775 °C (see Fig. 6.1.1). No silicon growth can be detected on the silicon dioxide. The undercut of the oxide wall during hydrogen prebake for selective epitaxy is related to the hydrogen pressure at high temperatures [11]. It was proposed that adsorbed hydrogen provides Si intermediates by the following reactions:

(1) $SiO_2(s) + 4H(ads) \Leftrightarrow 2H_2O(g) + Si(ads)$
(2) $Si(ads) + SiO_2(s) \Leftrightarrow 2SiO(g)$

From Fig. 6.1.4 it can be seen that the undercut is totally filled with epitaxial silicon. No voids can be seen at all, which is a stringent requirement for CMOS-technologie. Thicknesses were evaluated for different window sizes from 1 cm^2 down to 20*20 μm^2 as described in chapter 4.5. Within the precision of the stylus profiler no variation of layer thickness over the wafers could be detected. It also should be mentioned that there is no difference between areal and selective layer thicknesses within the resolution of the measurements.

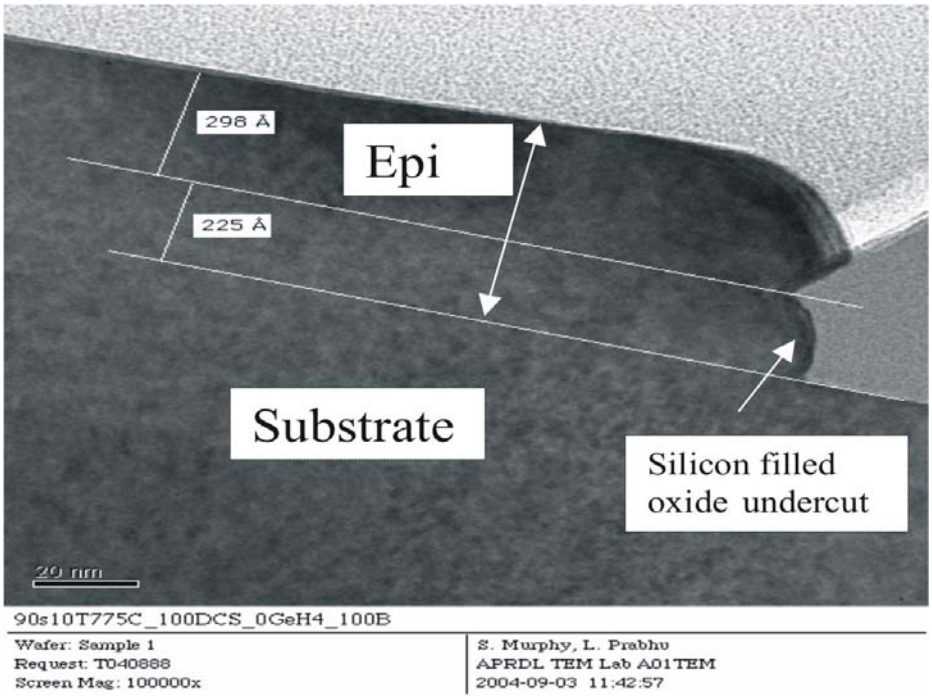

Fig. 6.1.4: TEM-image of a selectively grown Si:B layer. The growth temperature was 775 °C. DCS and B_2H_6 were used as precursors.

Conclusion

This process fulfills all requirements of an industrial production sequence. Selective growth of crystalline and highly-doped source / drain-extensions (resistivity <1 mOhm cm) with a thickness between 15 nm and 20 nm. Even the thickness of 50 nm for selective

deposition of pMOS sources/drains is reached. The deposition rates are sufficient to achieve reasonable throughput.

6.2. Selective growth of intrinsic $Si_{1-x}Ge_x$-layers

In the introduction of this chapter it was mentioned that processes for deposition of $Si_{1-x}Ge_x$-layers are desireable. A Ge concentration between 20-30% was targeted. The process parameter space under investigation was defined as follows:

- Ex-situ wet-chemical standard cleaning (RCA).
- In-situ thermal desorption for t = 5 min at T_S = 900 °C (10 Torr total chamber pressure) in H_2.
- Process pressure: 10 Torr, growth temperature 700 °C.
- 2-7 sccm GeH_4 flow, 16/1 slm H_2, 50 sccm DCS.

Fig. 6.2.1 shows the SEM image of a $Si_{0.8}Ge_{0.2}$ mesa grown at 700 °C. The magnification is 60.000 and confirms a thickness of more than 200 nm. No deposition can be detected on the SiO_2, showing a deposition process fully selective with respect to silicon dioxide. The facets visible are caused by the used lithografy which only has a resolution of 1 μm.

Fig. 6.2.1: SEM image of a selectively grown $Si_{0.8}Ge_{0.2}$ mesa of 200 nm thickness. The growth temperature was 700 °C. DCS and GeH_4 were used. No deposition can be detected on the silicon dioxide mask.

Growth rates and alloy compositions

Spectral ellipsometry provides a fast, nondestructive and accurate measurement technique already used as in-line production control. From the measurement data layer thickness and

composition may be fitted with an appropriate optical model (see chapter 4.3). Additional Sopra GXR (grazing-incidence x-ray) measurements and AFM, SEM measurements were performed for very accurate thickness estimation.With these methods we estimated growth rate and alloy composition as depicted in Fig. 6.2.3, Fig. 6.2.4.

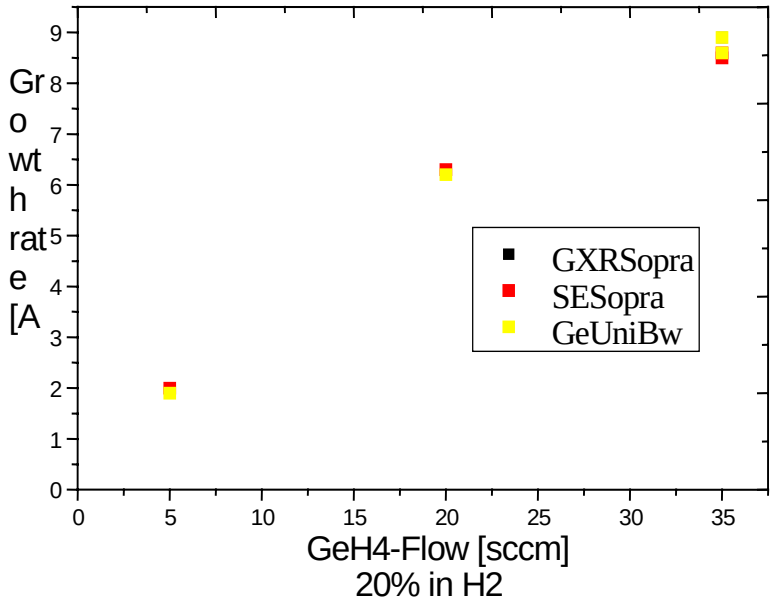

Fig. 6.2.3: Growth rate of the $Si_{1-x}Ge_x$ layers selectively grown by LPCVD with varying GeH_4-fluxes at 700 °C on a Silicon substrate patterned with a SiO_2 mask.

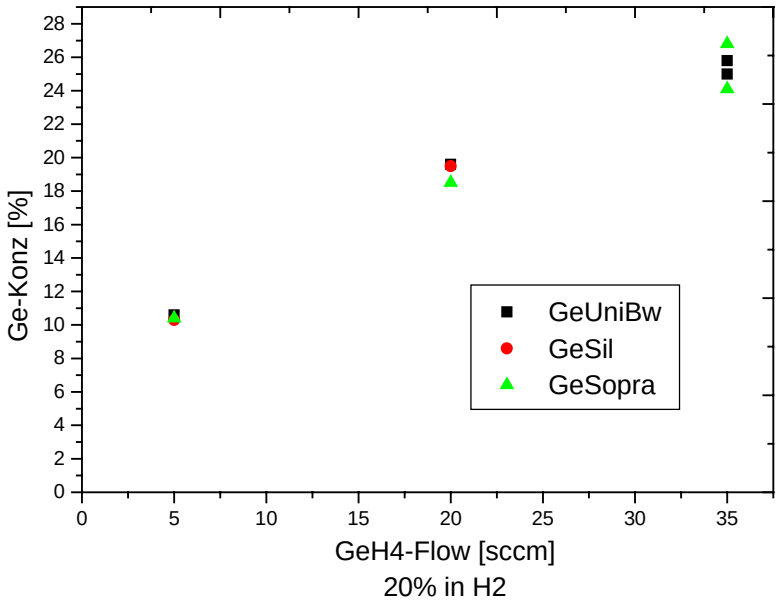

Fig. 6.2.4: Composition of the $Si_{1-x}Ge_x$-layers selectively grown by LPCVD with varying GeH_4-fluxes at 700 °C on a Silicon substrate patterned with a SiO_2 mask.

The deposition rate behaves linear with GeH_4-flux which in literature is explained by GeH_4-catalysis of the Dichlorosilane process [12]. It may be noted that despite the lower temperature (700 °C) the rates still meet Freescales throughput requirements.

The alloy composition bows down from linearity for small GeH_4-flows, which is also expected from literature [1]. Optical microscopy confirmed specular surfaces and selectivity with respect to silicon dioxide.

Surface morphology and crystal quality

Due to the large lattice misfit of 4% between Si and Ge crystals there is a significant amount of strain energy built up during growth of $Si_{1-x}Ge_x$-alloys. Depending on Ge concentration and layer thickness this energy is relaxed through generation of misfit dislocations. These dislocation network generates surface undulations on top of the corresponding $Si_{1-x}Ge_x$-layer. The resulting morphology, known as "cross-hatch" (see Fig. 6.2.5) was investigated with AFM[1]-measurements. These "cross-hatching" is known to have a bad influence on MOSFET's fabricated on Si/ $Si_{1-x}Ge_x$-heterostructures [14]. Also, additional layers grown over the $Si_{1-x}Ge_x$-layer are known to get a rough surface. This is an especially important problem in the fabrication of vertical transistors that are based on $Si/Si_{1-x}Ge_x$ epitaxial layer stacks. For these reasons, epitaxial surfaces should be as flat as possible.

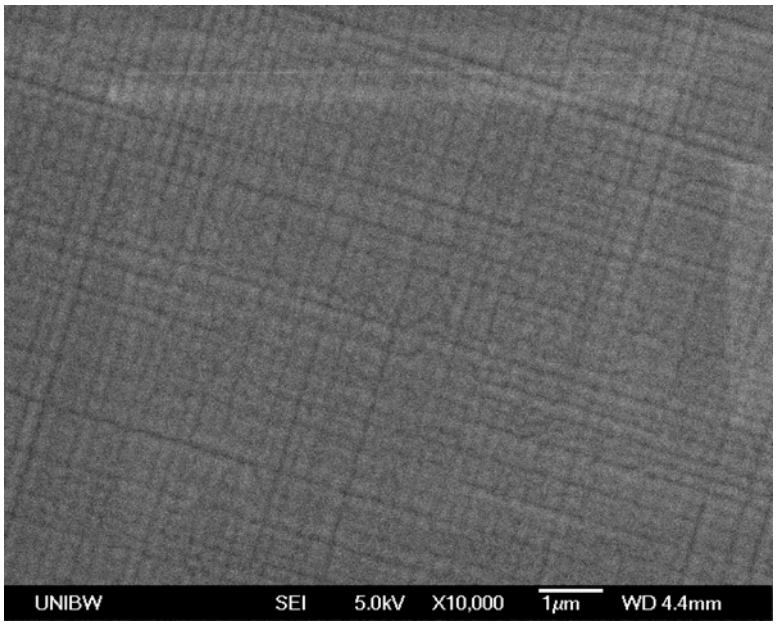

Fig. 6.2.6: SEM-Image of a 250 nm SEG-$Si_{0.65}Ge_{35}$ -layer, showing the typical "cross-hatch".

The surface topography and root-mean-square-(RMS)-roughness was investigated with 500*500 nm scans performed on a Burleigh Aris-3300 contact-AFM. The resolution limit is 1 nm.

[1] Atomic Force Microscope

Ge-concentration	10 %	15 %	20 %	26 %
RMS-roughness	< 1 nm	< 1 nm	3,99 nm	5,75 nm

Tab. 6.2.1: RMS-roughness over Ge-concentration for intrinsic $Si_{1-x}Ge_x$-alloys grown selectively on patterned wafers. The layer thickness was 20 nm.

Tab. 6.2.1 gives the RMS-rougness of the above mentioned intrinsic $Si_{1-x}Ge_x$-layers. For 10%, 15% Ge-content RMS-roughness is below the resolution limit of 1nm. For germanium contents above 20% the RMS-roughness is strongly increasing. Fig. 6.2.6 shows the AFM-Images of the above SEG-$Si_{1-x}Ge_x$-layers, left 20% germanium, right 26% germanium. The microstructures visible especially on the right side are known by literature as so called undulations (see above). This is a sign of beginning lattice relaxation.

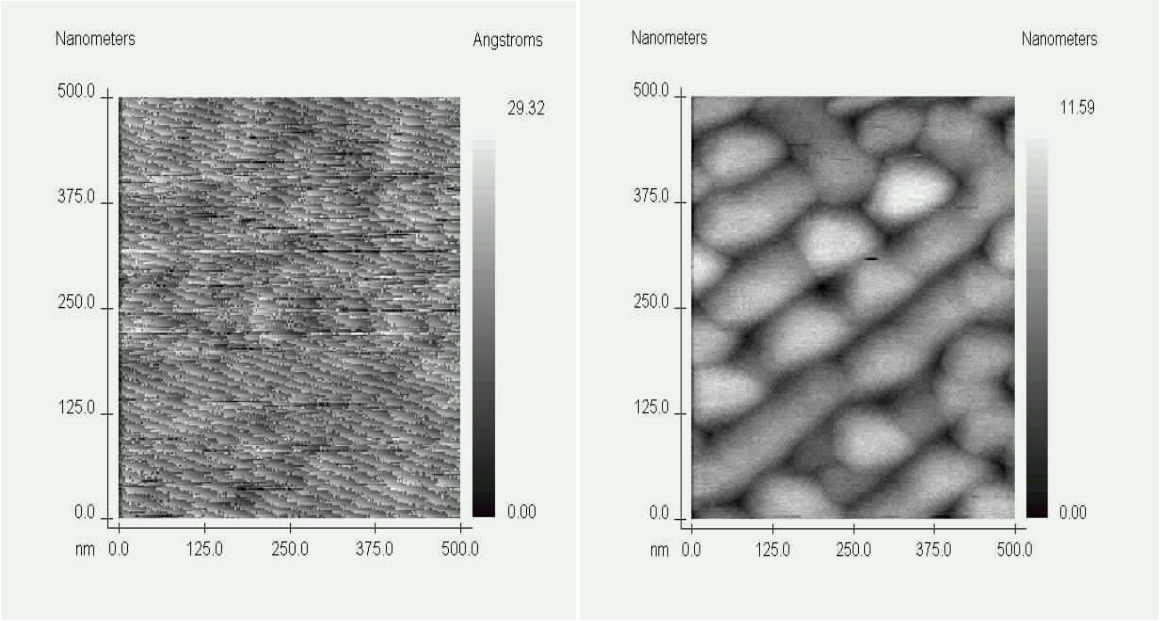

Fig. 6.2.6: AFM-Images of 20nm SEG-$Si_{1-x}Ge_x$ -layers, left 20% germanium, right 26% germanium

Fig. 6.2.7 shows the corrsponding SEM-images with a magnitude of 200000 (1 cm = 50 nm).

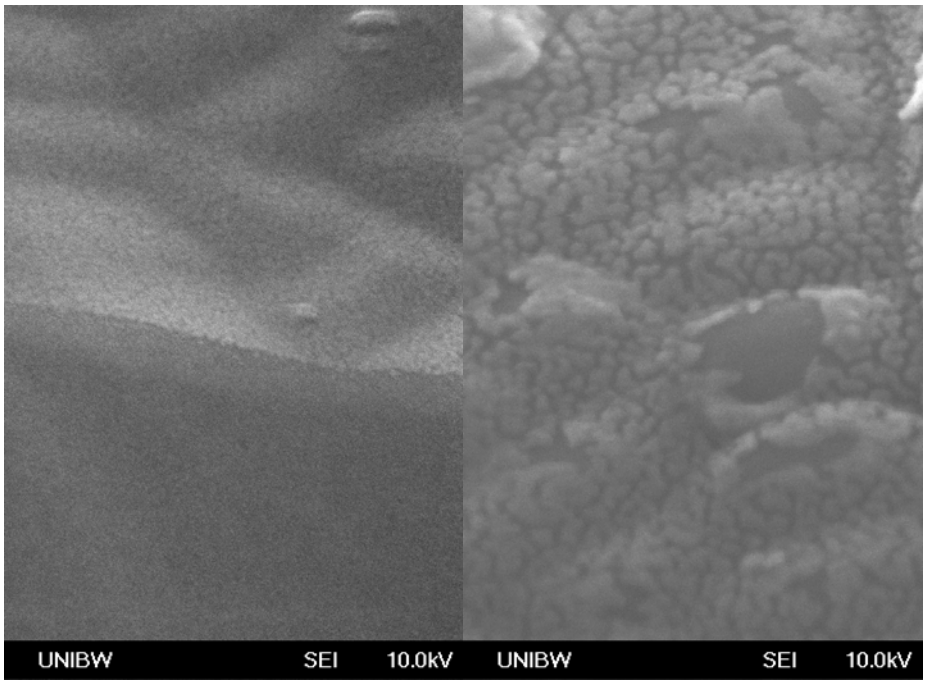

Fig. 6.2.7: SEM-Images of 20nm SEG-$Si_{1-x}Ge_x$ -layers, left 20% germanium, right 26% germanium.

As can be clearly seen the surface undulations have a size of approximately 100 nm. The small particles on top are an artefact stemming from platinum sputtering which is a standard sample preparation for SEM-measurements. The undulations are much bigger for the sample with 26% germanium (right hand side) than for 20% germanium (left hand side).
From these investigations the following conclusions can be drawn:

- Deposition rate and germanium-content are rising almost linear with GeH_4-flow and meet the requirements of industrial applications.

- Surface roughness is getting stronger with germanium-content, this phenomena is connected to the higher misfit dislocation density caused by lattice relaxation.

- Selectivity with respect to silicon dioxide is good (optical microscopy and SEM).

From literature it is well known that pseudomorphic $Si_{1-x}Ge_x$-layer are metastable [15]. Thickness and Ge concentration determine the temperature at which the layer can be deposited without starting lattice-mismatch relaxation [16,17]. Thus lowering growth temperature below 700 °C is necessary to reduce roughness for $Si_{1-x}Ge_x$-epitaxy. However, it should be mentioned that lattice relaxation may also be activated by the thermal budget of following processes.

To further examine crystal quality vertical pin-diodes were fabricated by growing i-$Si_{1-x}Ge_x$-layers on heavily n-doped Si substrates. The procedure is described in chapter 2.4. Fig. 6.2.8 exhibits the reverse current of a pin-diode (normalized to the area of the pin-diode) with an 80 nm thick intrinsic $Si_{0.9}Ge_{0.1}$-layer.

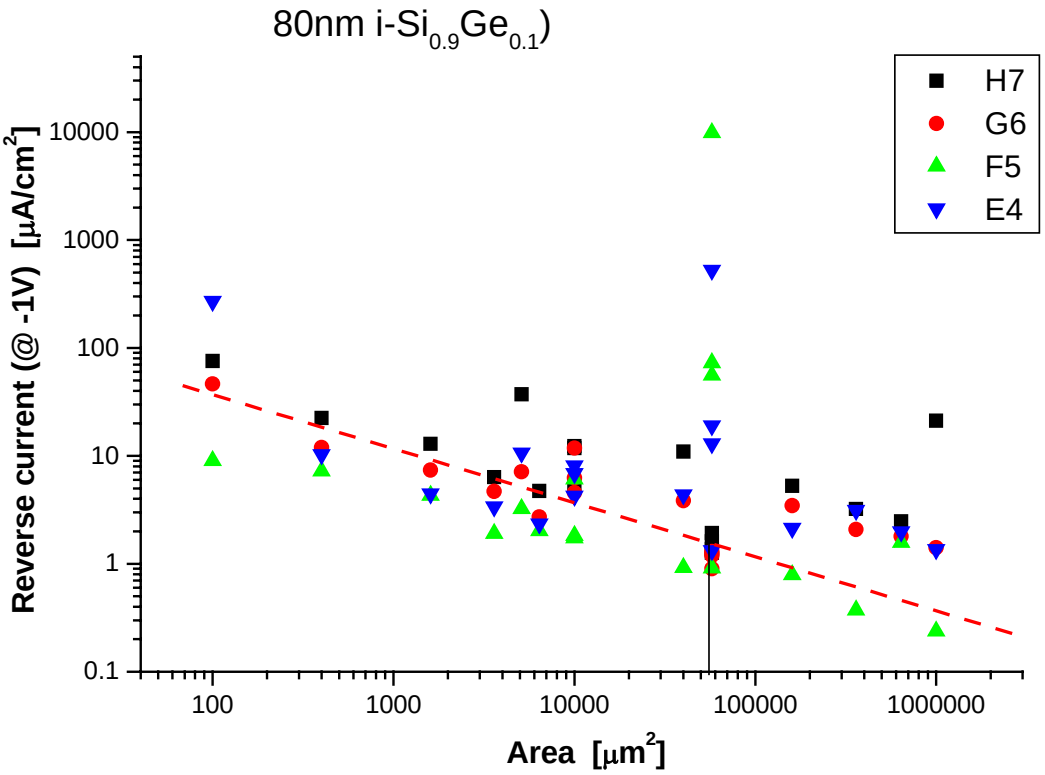

Fig. 6.2.8: Normalized reverse current of pin-diodes with i-$Si_{1-x}Ge_x$-layer as a function of mesa area size.

H7, G8, F5 and E4 refer to different chips on the tested wafer. The dependence of the normalized reverse current on mesa area exhibits a slope of -0.5 up to a mesa area of 1 mm^2. A slope of -0.5 means that the leakage current is dominated by the passivation around the pin-mesas. No sign of extended defects is visible even up to an area of mm^2. Contribution of extended defects is only visible for few of the tested pin-diodes.
In general, this demonstrates an excellent crystal quality.

6.3. Selective growth of heavily boron-doped $Si_{1-x}Ge_x$-S/D-extensions

Fig. 6.3.1 and 6.3.2 show the TEM-images of a $Si_{1-x}Ge$:B layer selectively grown by LP-CVD on a silicon substrate patterned with a SiO_2 mask. Process parameters are: 10 Torr, 775 °C, 16/1 slm H_2, 50 sccm DCS, 10 sccm GeH_4/H_2 20%, 50 sccm B_2H_6/H_2 500 ppm. The deposition time was 90 s giving a layer thickness of 107 nm.

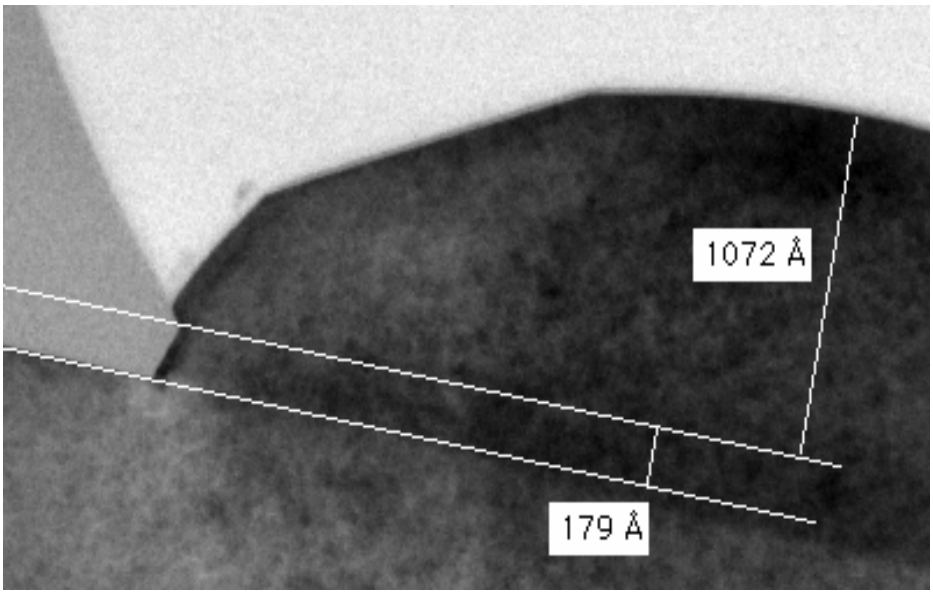

Fig. 6.3.1: TEM-image of a $Si_{1-x}Ge_x$:B layer selectively grown by LPCVD on a silicon substrate patterned with a SiO_2 mask. Process temperature was 775 °C and a DCS/GeH_4/B_2H_6-chemistry was used.

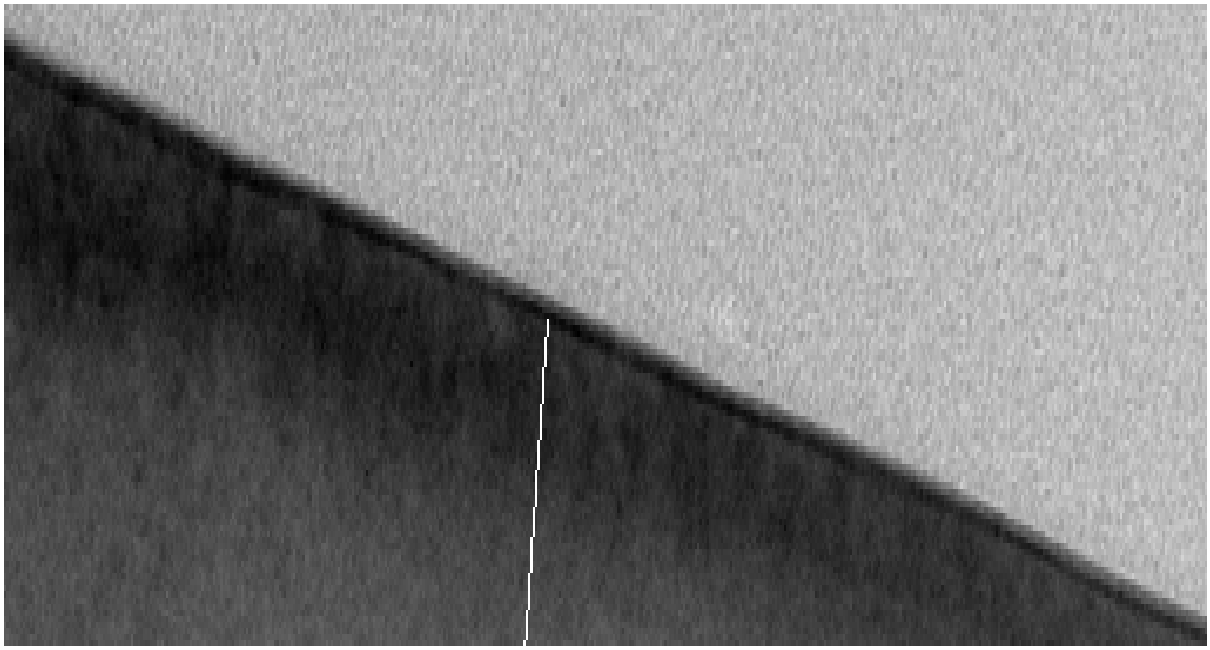

Fig. 6.3.2: TEM-image showing undulations (same layer as above).

Growth rates and alloy compositions

Fig. 6.3.3 contains the areal growth rates of B_2H_6 doped epitaxial layers. All growth rates show Arrhenius type behaviour. The activation energy is found to be 44 kcal/mol for DCS-B_2H_6-related silicon growth. The deposition rate for DCS related silicon epitaxy is connected to hydrogen desorption from the growing surface as rate-limiting step. Sinniah [10] reported an activation energy of 47 kcal/mol for hydrogen desorption from a Si(100)-surface. This may imply that the DCS/ B_2H_6-system follows the same rate-limiting step. It should be noted here that the same argumentation is true for the i-Si growth from DCS (see chapter 6.1). Adding 4 sccm GeH_4 to the DCS-process results in a much higher deposition rate (see Fig. 6.3.3). The activation energy is found to be 24 kcal/mol. The germanium content evaluated by spectral ellipsometry rises with decreasing deposition temperature as depicted in Fig. 6.3.3. Here it may be noted that similar trends were reported for the DCS-GeH_4-PH_3-system [1,5] and the DCS-GeH_4-AsH_3 –system [13].

With the above results on intrinsic $Si_{1-x}Ge_x$-layers we decided to choose the process with 4 sccm GeH_4-flow (leading to 20% Ge-content at 700 °C) as starting point for very-low-temperature boron-doping investigations. Growth temperatures were 700, 625 and 550 °C. To avoid defect generation by excessive Boron-doping the corresponding Diborane fluxes were set to 200, 100 and 50 sccm.

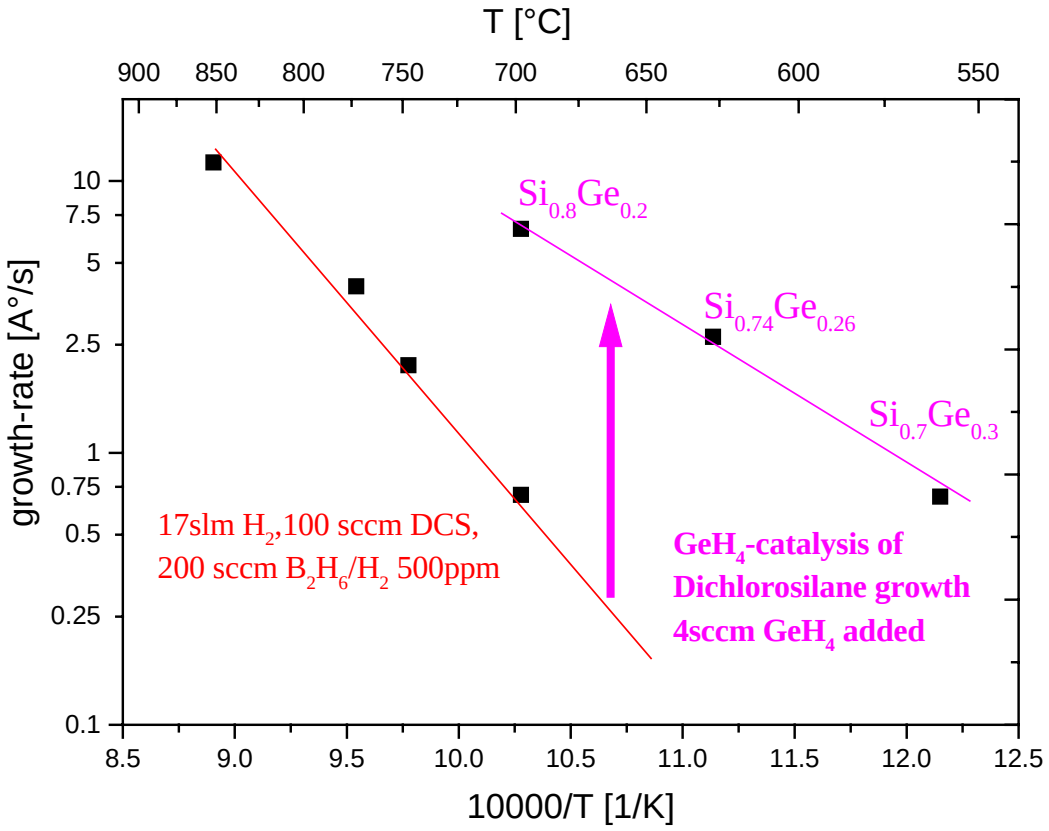

Fig. 6.3.3: Growth rates for diborane doped Si and $Si_{1-x}Ge_x$-layers as a function of inverse temperature. Data with and without GeH_4 are presented.

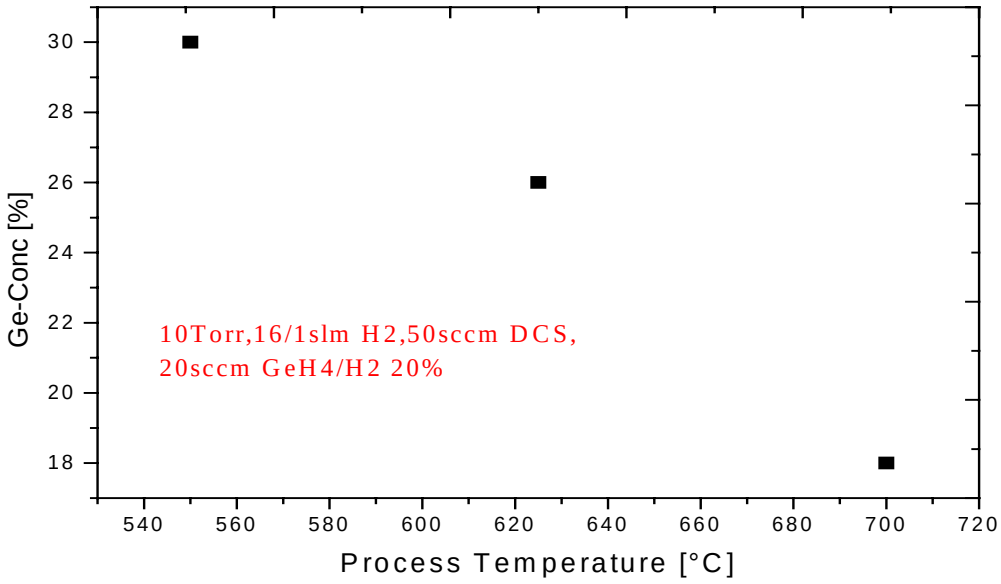

Fig. 6.3.4: Ge-concentration of heavily Boron-doped $Si_{1-x}Ge_x$-layers

Fig. 6.3.3 shows a strong thermally activated behaviour of the deposition rate. It may be noted that the process temperatures 700 °C and 625 °C still meet Freescales throughput requirements.
The alloy composition (Fig. 6.3.4) increases strongly with lower growth temperature which is expected from literature [2,3]. The reason is the higher reactivity of the germane process gas as compared to dichlorosilane.

Selectivity

Optical microscopy confirmed specular surfaces of the epitaxial layers. To investigate selectivity and loading effects we used patterned wafers as described in chapter 4. No deposition on the oxide mask could be detected showing full selectivity of the processes. Thicknesses were evaluated for the different window sizes described in chapter 4. Within the precision of the mechanical stylus profiler no variation of layer thickness over the wafers could be detected.

Surface morphology and crystal quality

To investigate surface quality we performed AFM-measurements on a Burleigh Aris-3300 contact-AFM. Fig. 6.3.5 presents 500*500 nm scans for the 3 boron-doped SiGe-layers according to Fig. 6.3.3. Clearly visible, the undulations are decreasing for process temperatures <700 °C. This evidences smaller lattice relaxation at lower temperatures.

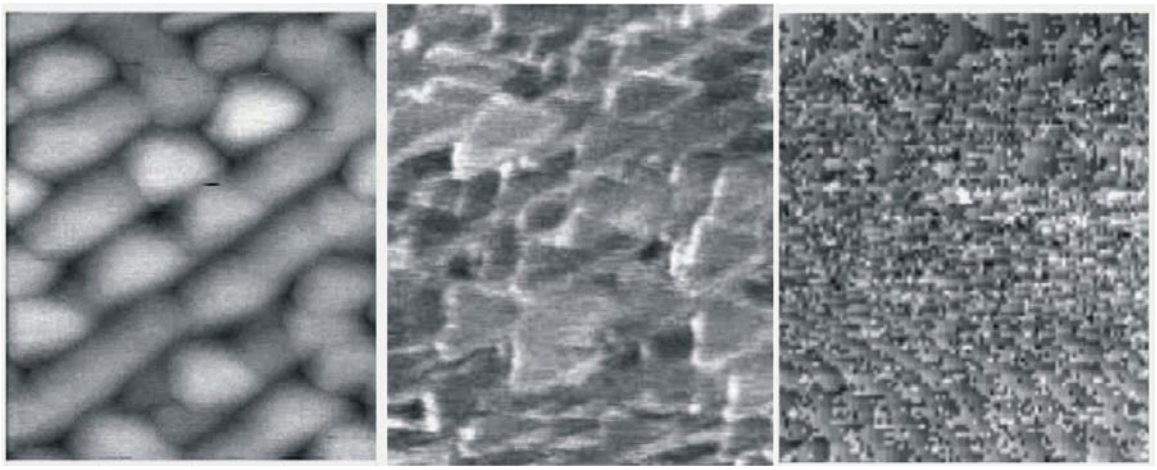

Fig. 6.3.5: AFM-Images 500*500 nm of 20 nm thick boron-doped SEG-$Si_{1-x}Ge_x$-layers, resistivity <1 mΩ cm, left 700 °C 26% Ge, middle 625 °C 26% Ge, right 550 °C 30% Ge.

The root-mean-square (RMS) roughness was also investigated. According to table 6.3.1 the RMS values drop strongly with decreasing deposition temperature. This is even true for the higher Ge-content of the sample grown at 550 °C.

Process temperature [°C]	700	625	550
Ge-concentration [%]	26%	26%	30%
RMS-roughness [nm]	5,75 nm	<1 nm	<1 nm

Tab. 6.3.1: RMS-roughness and Ge-concentration for heavily boron-doped SiGe-layers as a function of growth temperature.

Fig. 6.3.6 shows TEM cross sections of heavily boron doped Si (left) and heavily boron doped SiGe (right). The process temperatures were 775 °C and 625 °C, respectively (see Fig. 6.3.3). Despite of the high doping concentration no defects can be observed.

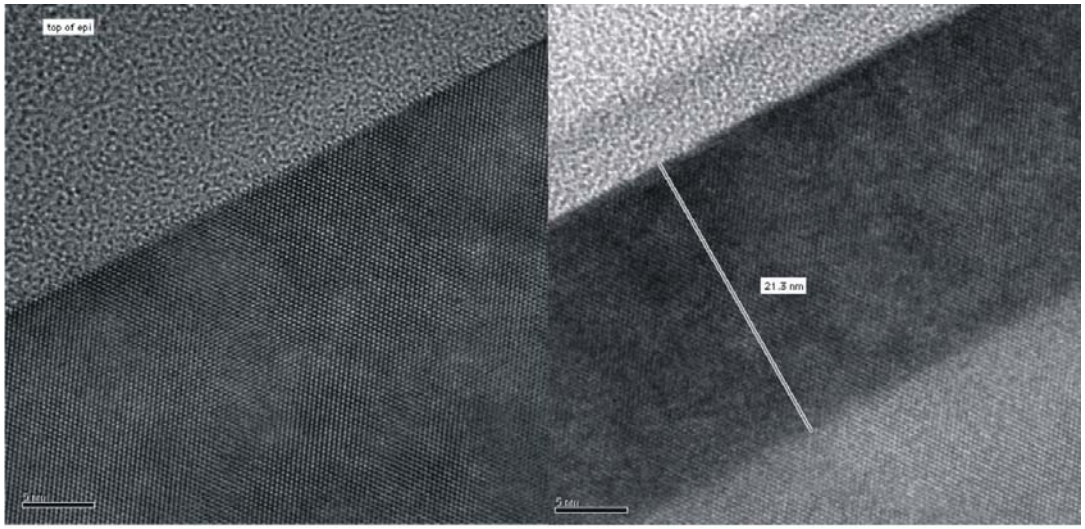

Fig. 6.3.6: TEM-images: left: Si:B 775 °C, see Fig. 2 (resistivity: 1.4 mΩ cm, see Fig. 8). Right SiGe:B 625 °C, see Fig. 2 (resistivity: 0.6 mΩ cm, see Fig. 8).

Resistivity and doping behaviour

For resistivity measurements 4-point probing on fullsheet and inside seed windows of patterned wafers was performed. No differences have been observed within the resolution limit of the prober. Here it should be noted that it is not straightforward to extract dopant concentration for SiGe layers from SIMS-measurements because calibration standards for varying SiGe-alloys are not available (see chapter 4.3). Because of these reasons we only mention the resistivities of the layers derived from four-point-probing and layer thickness measurements. Fig. 6.3.7 contains the resistivity vs. germanium mole fraction for different process parameters. Independent of parameter variations the resistivity drops with rising Ge-content up to 18%. This is consistent with the results of Noh, Murota [4] for a silane-germane-diborane chemistry and may be independent of precursor choice. As an explanation lattice strain compensation by germane-boron co-doping is proposed [5]. The resistivity values belong to the lowest ever published for epi-grown boron-doped $Si_{1-x}Ge_x$ to the best of the author's knowledge.

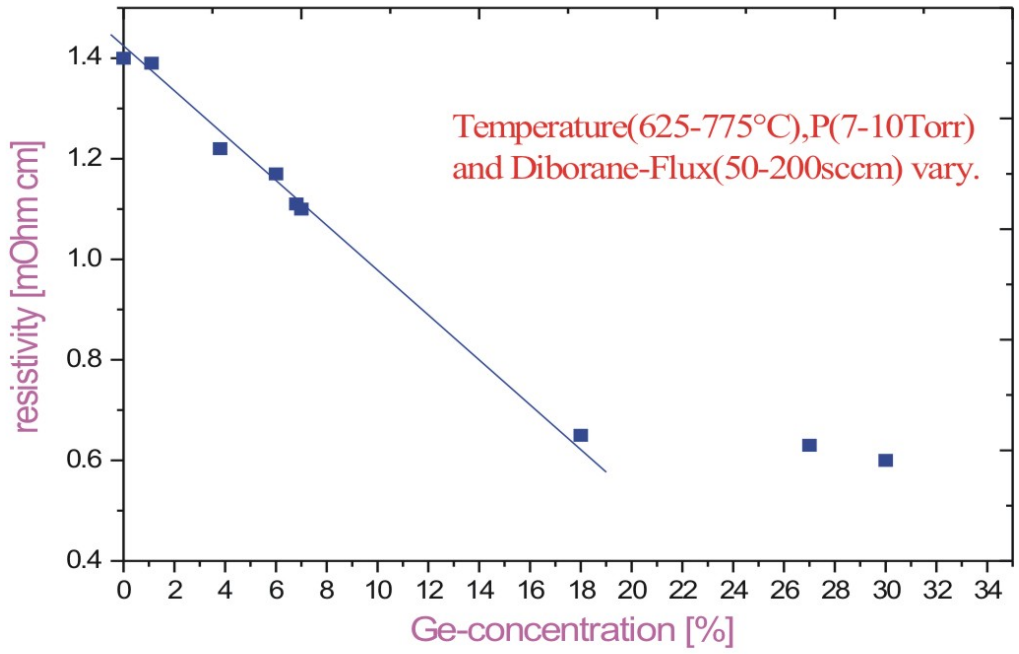

Fig. 6.3.7: Resistivity as a function of germanium mole fraction x for heavily boron doped $Si_{1-x}Ge_x$ layers (variation of temperature, pressure P and dopant gas fluxes)

It should be noted that boron-incorporation also rises with smaller growth temperature. To avoid defect-generation by extreme boron-incorporation ($<10^{21}/cm^3$) in low-temperature processing diborane-fluxes are lowered (100 sccm for 625 °C, 50 sccm for 550 °C) to achieve maximum dopant-activation.

To investigate selectivity and loading effects we used patterned wafers as described in chapter 4. No deposition on the oxide mask could be detected showing full selectivity of the processes. Thicknesses were evaluated for the different window sizes described in chapter 4. Within the precision of the mechanical stylus profiler no variation of layer thickness over the wafers could be detected.

The results can be summarized as follows:

- The growth rate rises almost linear with GeH_4-flux up to 30% alloy composition.
- Germanium incorporation rises almost linear with GeH_4-flux. The lattice strain compensation due to higher germanium mole fraction leads to a higher dopant activation up to 20% Ge.
- Dropping the process temperature to 625-550 °C leads to very smooth surfaces, even for very high boron-doping levels; this is attributed to the temperature-activated lattice relaxation.
- At 625 °C process temperature we achieved 42 nm layer thickness without deposition on the oxide. This may even by enough for depositing source/drain with boron-doped SiGe of less than 1 mΩ cm resistivity.
- No loading effects could be observed within the precision of the mechanical stylus profiler.
- The selective deposited layer thickness was always over 50 nm.

Conclusion

The boron doping behaviour in silicon epitaxial layers for different process temperatures was investigated. A dichlorosilane chemistry without additional HCl has been used. Selectivity with respect to silicon dioxide was achieved for Si:B and SiGe:B. The selectively deposited layer thickness was always above 50 nm. The process is suitable for selectively epi-grown source/drain-(extensions) in future CMOS-devices. For Si:B and SiGe:B homogeneity over the patterned wafer could be achieved within the accuracy of the thickness measurements. The addition of germane to the growth enviroment improves deposition rate, especially at temperatures smaller than 700 °C. With TEM investigations and the fabrication of pin-diodes very low defect levels could be confirmed. Dropping the process temperature to 625 - 550 °C leads to very smooth surfaces, even for very high boron-doping levels; this is attributed to the temperature-activated lattice relaxation. Up to 18% Ge the resistivity drops with rising Ge-content. This is consistent with the results for a silane-germane-diborane chemistry and may be independent of precursor choice. The

resistivity achieved (0.8 mΩ cm for Si:B and 0.6 mΩ cm for SiGe:B) meets the ITRS[1] [18] requirements of the coming technology nodes.
Therefore this process fulfils the requirements of an industrial production sequence.

[1] International Technology Roadmap for Semiconductors

7. N-type doping

In the past, there was considerable interest in the selective growth of n-type doped SiGe-structures with low pressure chemical vapour deposition (LPCVD). In most studies PH_3 served as dopant gas [1,2]. Other researchers [3,4] investigated phosphine (PH_3) and arsine (AsH_3) doping in atmospheric pressure chemical vapour deposition (APCVD). It is well known that n-type doping from group-V-hydrides is difficult because of strong reduction of the growth rate, while doping efficiency is insufficient in most cases [1,5,6,7].
The exact doping mechanism is still unclear. R. Reif [7] suggested that the electronic nature of the surface impacts adsorption behaviour. Yu et al.[8] found that a semiconductor surface is generally p-type due to a large density of dangling bonds. By heavy adsorption of phosphorus the Fermi level shifts rapidly towards the conduction band. Boron doping caused the Fermi level to shift towards the valence band. Changes in surface adsorption may be expressed as changes in Fermi level and surface band bending. Murota [9] proposed that the number of active adsorption sites is related to the Fermi level which is given from arsenic concentration in the semiconductor bulk and the growth temperature. Bloem et al. [10,11] considered the transition from an intrinsic semiconductor to an extrinsic semiconductor to explain doping incorporation.
However, data on homogeneity over the patterned wafer, growth rate and doping efficiency, are still lacking for PH_3 and AsH_3.

7.1. Areal growth & doping

Fig. 7.1 shows the areal growth rates of arsenic doped epitaxial layers. The dopant gas flow was always 25 sccm of AsH_3/H_2 1%.
The activation energy for DCS-related silicon growth is found to be 52 kcal/mol. The deposition rate for DCS is connected to hydrogen desorption from the growing surface as rate-limiting step. Sinniah [12] found an activation energy of 47 kcal/mol for hydrogen desorption from a Si(100)-surface. For a process pressure of 640 Torr the activation energy is found to be reduced to 31 kcal/mol.
Silane-related growth shows a contrary behaviour. The activation energy is rising with pressure from 24 kcal/mol at 10 Torr up to 43 kcal/mol at 80 Torr. This observation indicates that the hydrogen desorption limited regime is reached only for higher process pressures. Higher partial pressures of silane also lead to gas phase reactions producing an enhanced amount of highly reactive silicon containing species, e.g. SiH_2, SiH_3 [13]. These enhance the deposition rate.
Adding 4 sccm GeH_4 to the DCS-process at 10 Torr, 700 °C results in a much higher deposition rate (see Fig.7.2). A similar trend was reported for the DCS/GeH_4/PH_3-system [1,5].

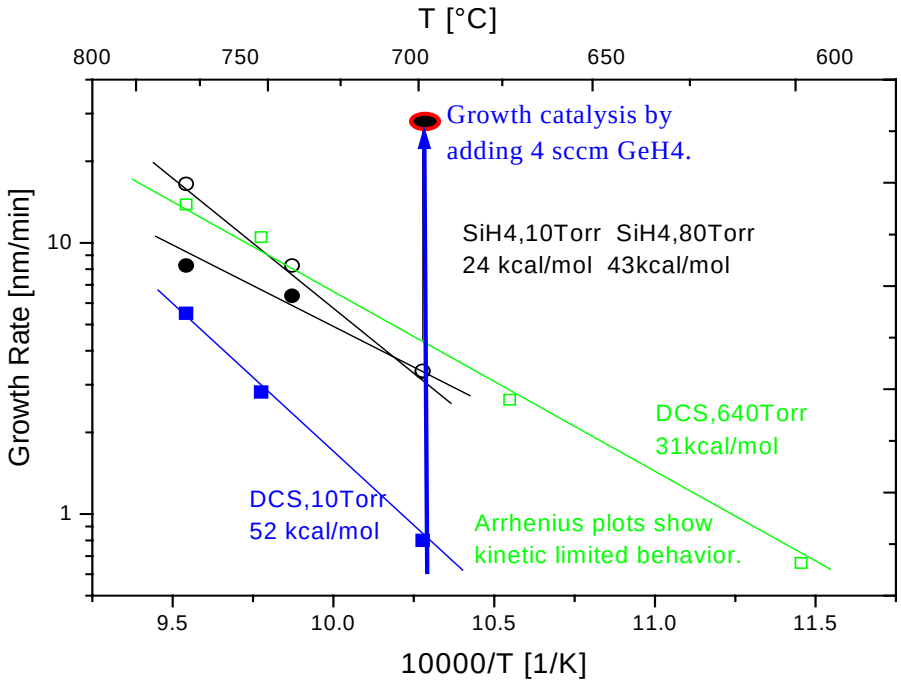

Fig.7.1: Growth rate for arsine doped Si and SiGe-layers, 100 sccm DCS, 10 Torr (full squares) 100 sccm DCS, 640 Torr (open squares) 100 sccm SiH_4, 10 Torr (full circles) 100 sccm SiH_4, 80 Torr (open circles) (17 slm H_2, AsH_3/H_2 1%).

Areal doping behaviour

Fig. 7.2 depicts the temperature dependence of the SIMS evaluated arsenic concentrations in the epitaxial layers for silane and DCS related growth.

Dichlorosilane (DCS) related arsenic doping

For 640 Torr the incorporated arsenic dopant concentration shows a temperature dependence ranging from $10^{19}/cm^3$ (775 °C) up to $2*10^{21}/cm^3$ (600 °C), see Fig. 7.2. The temperature dependence has the form [As] = $a\exp(b/T)$, with b = $2.77*10^4$ [1/K]. A similar dependence is found in the data of Agnello, Sedgwick [3,4] for 760 Torr total process pressure. In the range from 750-600 °C Agnello found b = $3.37*10^4$ [1/K]. It is interesting to note that $2.77*10^4/3.37*10^4$ = 640 Torr/760 Torr within accuracy of the measurements. From this point of view one may conclude that the maximum arsenic concentration is closely linked to the total process pressure.
For LPCVD at 10 Torr the arsenic dopant concentration was always below the SIMS detection limit ($10^{17}/cm^3$), i.e. there was no arsenic detectable.
Adding 4 sccm GeH_4 at 10 Torr results in a strong signal of arsenic in SIMS. Here it should be noted that it is not straightforward to extract dopant concentration for $Si_{1-x}Ge_x$ from SIMS-measurements because calibration standards for varying $Si_{1-x}Ge_x$-alloys are not

available. Also curves linking ion concentration to resistivity are only found for bulk silicon crystals [14].
Because of these reasons we only mention that the resistivity of the layer derived from four-point-probing and layer thickness measurements was 5 mΩ cm. Therefore the DCS/GeH_4/AsH_3-system follows a similar trend as reported for the DCS/GeH_4/PH_3-system [1,5].

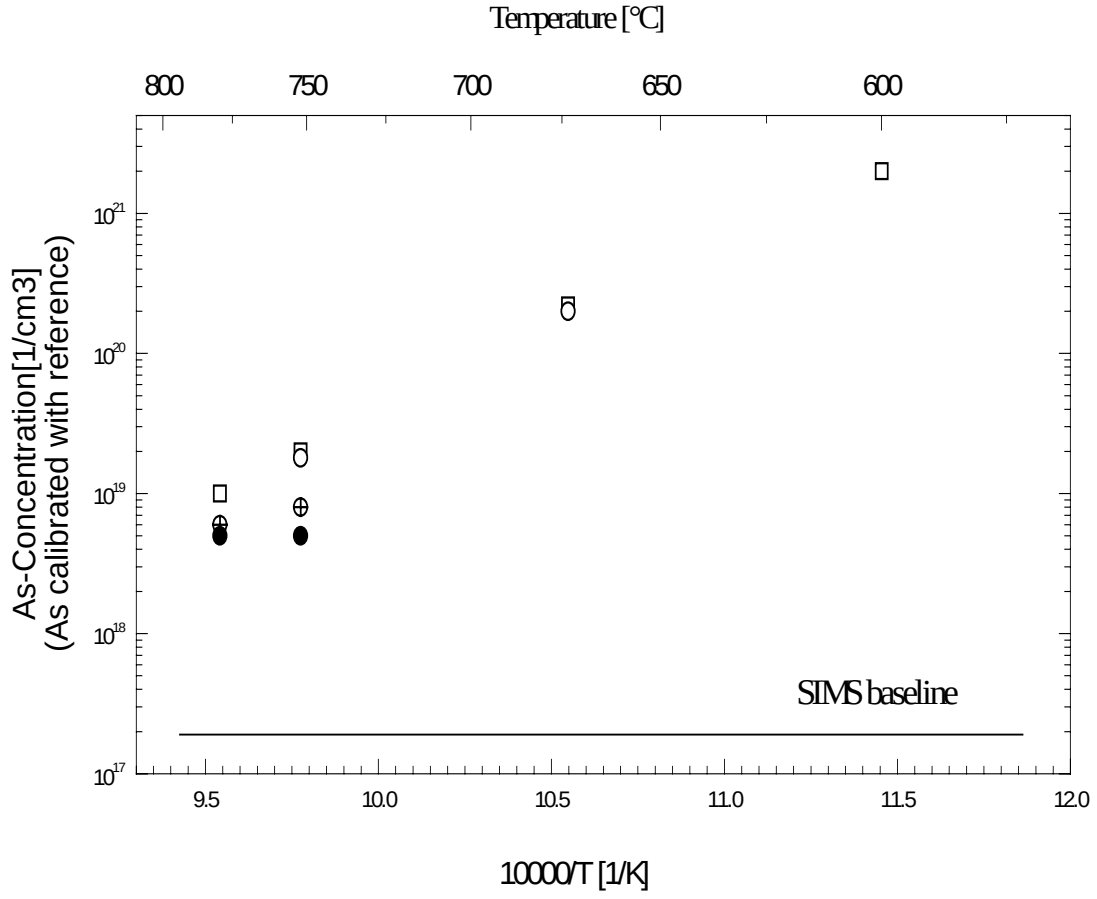

Fig.7.2: SIMS measured arsenic concentrations in epitaxial films deposited at different process pressures and temperatures. DCS, 10 Torr (baseline), DCS, 640 Torr (open squares), SiH_4, 10 Torr (full circles), SiH_4, 80 Torr (circles,+ center), SiH_4, 640 Torr (open circles) (17slm H_2, 25 sccm AsH_3/H_2 1%).

Silane related arsenic doping

In the range of 775-675 °C deposition temperature, the doping efficiency is rising with process pressure. For 10 Torr there is no temperature-dependence observed, while for the higher pressure of 640 Torr the As-concentration shows nearly the same temperature dependence as for DCS. The reason for this behaviour may be due to the stronger gas phase reactions resulting in more reactive silicon species, e.g. SiH_2, SiH_3 (see chapter 3.5.1) [13]. These are known to enhance n-type dopant incorporation. That the behaviour of silane and DCS shows the same tendency implies that a similar reaction path is valid for DCS. This will be discussed further in chapter 7.2.

Doping transitions

Fig. 7.3 shows the SIMS As-depth-profiling of epitaxial layers for different process temperatures and chemistries. For DCS the transition lenghts to reach a steady-state are in the order of some 10 nm. Adding 4 sccm GeH_4 at 700 °C to the DCS-system drasically reduces the doping transition length. For silane the transition lenght exceeds 50 nm.
R. Reif [7] suggested that the electronic nature of the surface impacts the adsorption behaviour. On an electron-deficient (p-type) surface stemming from boron-doping the number of dangling bonds may be larger than for an intrinsic surface enhancing adsorption. On an electron-rich (n-type) surface stemming from arsenic-doping further adsorption may be rendered.

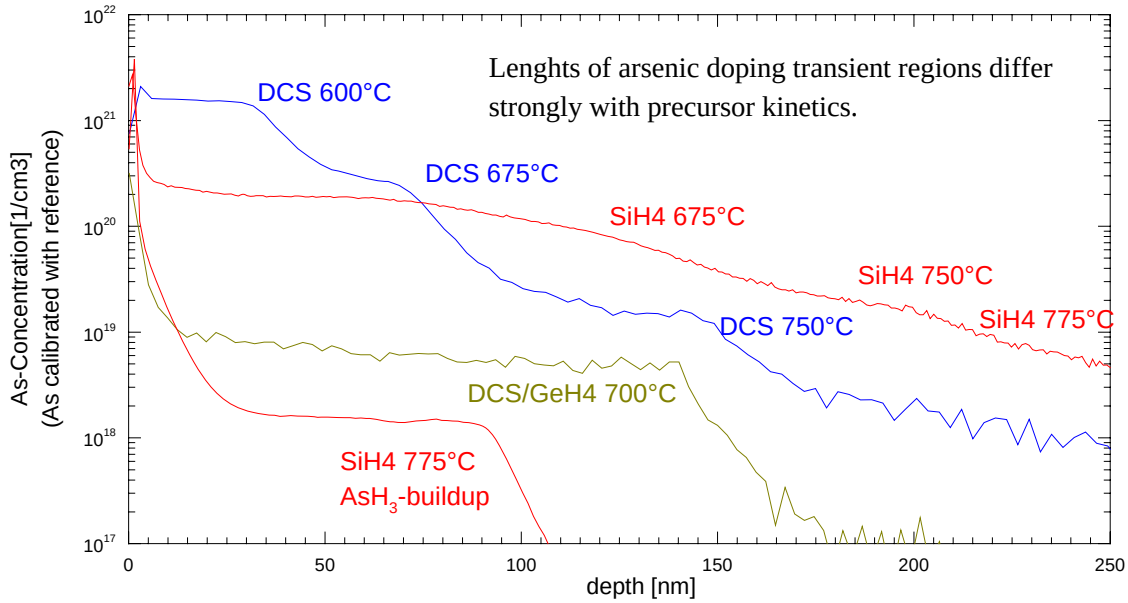

Fig.7.3: SIMS As-depth-profiling in epitaxial films deposited by varying precursor chemistries. The gas flows were 100 sccm SiH_4, 100 sccm DCS, 100 sccm DCS/4 sccm GeH_4, respectively.

A more formal approach to this problem recognizes that the driving force for adsorption is represented by a difference in chemical potential between the gas-source-molecule and the resultant surface adsorbate. The chemical potential of the semiconductor surface may be related to the Fermi level within the semiconductor and the corresponding band bending at the surface. Changes in surface adsorption are then expressed as changes in surface band bending.
Yu et al. [8] found that a semiconductor surface is generally p-type due to a large density of dangling bonds at a surface and the Fermi level for Si(100) surfaces is pinned about 0.46 eV above the valence band edge. By heavy adsorption of phosphorus the Fermi level shifts rapidly towards the conduction band by 0.45 eV. Boron doping caused the Fermi level to shift towards the valence band edge nearly 0.4 eV. These measurements were performed at

room temperature and found to correspond to surface structures as well. This changes could have strong effects with respect to surface adsorption and hence doping behaviour.
Murota [9] proposed that the number of active adsorption sites is related to the Fermi level which is given from As concentration in the semiconductor bulk and the growth temperature.
To further examine this behaviour we performed another arsenic doping experiment on 2 samples which were prepared as follows: 1) a heavily p-type (boron) doped substrate providing an electron-deficient (p-type) surface, 2) an AsH_3 built-up process (30 s of 25 sccm AsH_3 at 775 °C) on a heavily p-type (boron) doped (10 mΩ cm) substrate giving an electron-rich (n-type) surface.

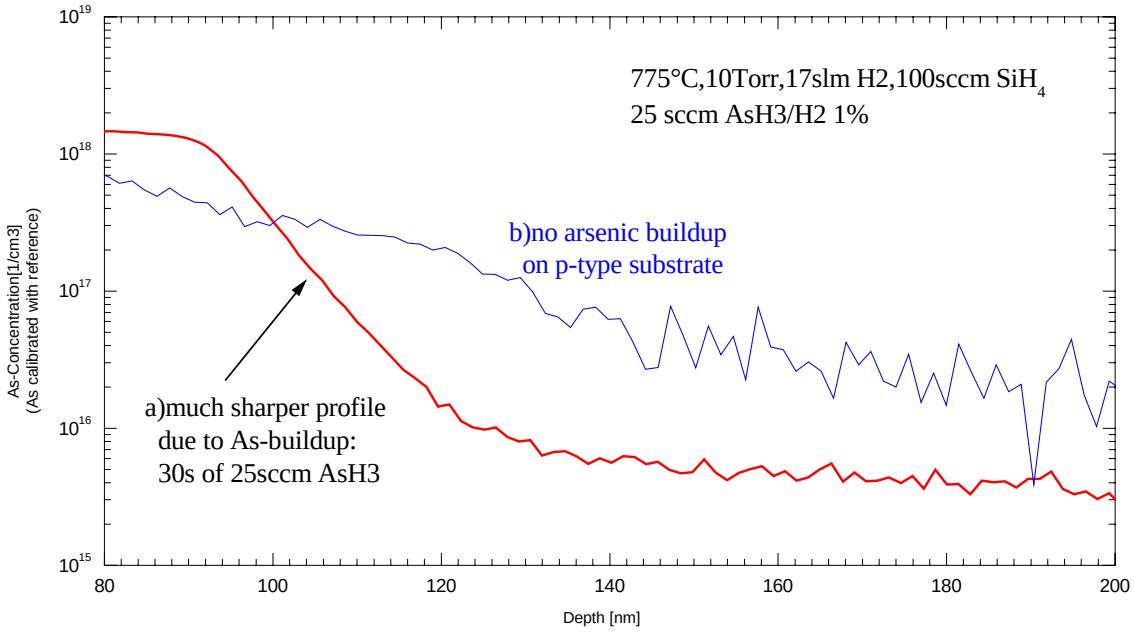

Fig.7.4: As-doping transition in epitaxial films (SIMS measurement) starting with a) As-built-up leading to an n-type surface, b) p-type surface because of boron-doped substrate.

Fig. 7.4 shows the As-depth-profiling in the epitaxial films grown on 1), 2) with a SiH_4/AsH_3-chemistry at 10 Torr. Clearly the preepitaxial arsenic built-up leads to a much stronger rise in As-concentration as compared to the case of the bare p-type substrate.

The following model is proposed:

With arsenic incorporated, the Fermi level begins to shift slowly towards the conduction band. This may cause enhanced incorporation of arsenic leading to an even stronger shift of the Fermi level and so on. When the Fermi level reaches the region directly underneath the conduction band edge arsenic incorporation saturates. The temperature-dependency of Fermi level and conduction band edge is linked to the doping saturation behaviour for large

arsine partial pressures. This may also be the reason why the As-concentrations are independent of silicon precursor for high arsine partial pressures (640 Torr).

7.2 Epitaxial growth of As doped Si and $Si_{1-x}Ge_x$ on patterned substrates

The above mentioned processes were also performed on substrates patterned with thermal oxide. The wafers were patterned as described in chapter 4.5. The selectivity was investigated by optical microscopy and SEM.
For the silane and the silane/arsine-system every sample exhibited deposition on the silicon dioxide mask.
No deposition on the silicon dioxide could be detected for the DCS and the DCS/GeH_4-system at 10 Torr process pressure. No thickness inhomogenities over the patterned wafer could be detected within the accuracy of the mechanical stylus profiler. This was already demonstrated in chapter 6.1 and 6.2.
Due to the fact that areal As doping of pure Si does not exhibit sufficient growth rates and doping efficiency (see chapter 7.1), the more promising As doped $Si_{1-x}Ge_x$-structures were investigated. It was also outlined that much higher doping incorporation is observed for higher process pressures up to 640 Torr. This implies that higher pressures also may be useful for the DCS/GeH_4/AsH_3-system. On the other hand, total process pressure must not be too high to avoid breakdown of selectivity (see chapter 3.6.2). Hence deposition at 10 Torr and 20 Torr pressure was performed with same gas flows. In others words all precursor partial pressures are also doubled. The arsenic doped $Si_{1-x}Ge_x$-layers showed full selectivity with respect to silicon dioxide as could be confirmed by optical microscopy and SEM. Mesa thicknesses were evaluated for different window sizes from 1 cm^2 area down to circular shaped windows of 160 to 100 μm diameter as described in chapter 4.5. In Tab. 7.1 representative layer thicknesses are listed. Very strong inhomogenities are detected. The growth rates rise strongly with decreasing window size. It should be noted that for 10 Torr total pressure the mesa thicknesses in the small circles are about 3 times bigger than in the big test windows. For 20 Torr process pressure this difference is smaller then 2 times. Also depicted is the mesa thickness enhancement factor λ from 10 Torr to 20 Torr. One would expect observing higher deposition rates for higher precursor partial pressures, but a difference of 4-7 times in mesa thickness cannot be explained only by the doubled precursor partial pressures.
To further investigate the loading effect SEM-images were performed. Fig. 7.5 shows the cross section of a $Si_{1-x}Ge_x$ mesa grown with DCS/GeH_4/AsH_3. The process pressure was 20 Torr. No deposition can be detected on the silicon dioxide. It is interesting to observe the enhanced mesa thickness at the edge. According to other researchers this indicates the occurrence of a chemical loading effect [15]. This means that additional precursor species are diffusing lateral from the silicon dioxide mask towards the seed window leading to higher growth rates at the edges.

	Window 1 cm^2 area	Circle 180 μm dia.	Circle 160 μm dia.	Circle 100 μm dia.
10 Torr	23 nm	60 nm	60 nm	60 nm
20 Torr	150 nm	250 nm	250 nm	250 nm
λ	6.52	4.17	4.17	4.17

Tab.7.1: Mesa thicknesses selectively grown in different seed windows for AsH_3 doped $Si_{1-x}Ge_x$.

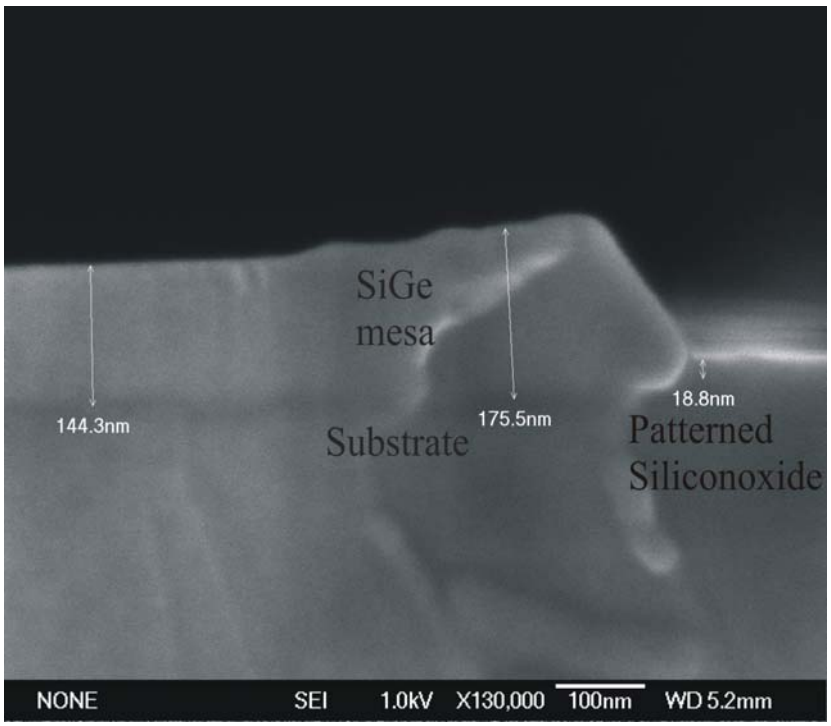

Fig.7.5: SEM-image cross section of As-doped $Si_{1-x}Ge_x$-mesa grown selectively to silicon dioxide. The enhanced mesa thickness at the edge indicates the occurrence of a chemical loading effect.

Because i-Si and i-$Si_{1-x}Ge_x$ deposited from DCS don't exhibit thickness inhomogeneities, it is clear that the observed loading effect must be strongly connected with the addition of AsH_3 to the deposition process. However, the reaction pathes of the three precursors DCS, GeH_4 and AsH_3 may influence each other resulting in a complex chemistry.

In a final experiment As doped Si was grown selectively from DCS and AsH_3 on the same silicon dioxide mask used above. Gas flows were the same as in chapter 7.1 and the total process pressure was set to 10 Torr. Mesa thicknesses were evaluated for different window

sizes from 1 cm^2 area down to circular shaped windows of 160 to 100 μm diameter as above. The sample exhibited strong inhomogeneities with the mesa thicknesses in the small circles about 3 times bigger than in the big test windows. From that observation it can be concluded that the cause for the loading effect lies mainly in the DCS/ AsH_3-system for the investigated process parameters. The influence of GeH_4 as the dominant reason may be ruled out.
In chapter 3.5.5.2 it was mentioned that the addition of PH_3 or AsH_3 to a SiH_4 deposition process shifts the growth regime from surface controlled to mass transport controlled and causes significant loading effects this way:
Adding arsine (AsH_3) to the process gas leads to a significant drop of growth rate. A stable monolayer of As is built rendering SiH_4 from further adsorbing. In this case only the more reactive species like SiH_2, SiH_3 contribute to the growth (see chapter 3.5.1) because they have a much higher sticking coefficient on P poisoned Si(100)-surfaces. The reactions involving production of SiH_3, SiH_2 are not the rate limiting steps in the deposition of intrinsic silicon from SiH_4, but they are if AsH_3 is added. This behaviour shifts the reaction path from a surface reaction dominated by the decomposition of SiH_4 to a reaction dominated by a gas phase reaction of SiH_4 to SiH_3 and SiH_2. Hence the deposition of As-doped Si from SiH_4 and $SiCl_2H_2$ is mass transport controlled. Deposition in the mass transport controlled regime is known to cause significant (chemical) loading effects (see chapter 3.6.3).

Conclusion

We investigated the arsenic doping behaviour in silicon epitaxial growth for different process temperatures and precursor chemistries.
For LPCVD at 10 Torr the arsenic dopant concentration was always very low ($10^{17}/cm^3$). For 640 Torr the arsenic dopant incorporation shows a temperature dependence ranging from $10^{19}/cm^3$ (775 °C) up to $2*10^{21}/cm^3$ (600 °C). Adding 4 sccm GeH_4 at 700 °C drastically reduces the resistivity (5 mΩ cm) while keeping a much higher deposition rate (see Fig. 7.1). Therefore the arsine-doping follows a similar trend as reported for phosphine [1,5].
The doping transition lenghts ranged from about 20 nm (DCS/GeH_4) up to more than 50 nm for silane. They are drasically reduced by an arsine build-up process. The doping behaviour can be explained in terms of the electronic behaviour of the surface.
Selectivity with respect to siliconoxide was achieved for DCS at low pressures (10, 20 Torr). For i-Si and i-$Si_{1-x}Ge_x$ homogeneity over the patterned wafer could be achieved within accuracy of the thickness measurements. Selective growth with arsine doped Si and $Si_{1-x}Ge_x$ layers has also been achieved. However, considerably loading effects have been observed as soon as arsine has been added. The growth rates rise strongly with smaller window size. As the reason the shift from surface controlled growth regime to mass transport dominated growth regime is discussed. The reactions involving production of the very reactive radicals SiH_3, SiH_2 are rate limiting in doping from arsine.

The addition of germane to the growth enviroment tackles the major problems of n-type doping with the group-V-hydrides, e.g. low deposition rate and doping efficiency.
In LPCVD selectivity can be achieved with clorinated silicon precursors. More investigations are necessary to deal with the loading effect problem.

8. Very low-temperature silicon CVD

The aggressive down scaling of CMOS puts stringent requirements on doping shallowness and abruptness of source/drain-junctions. Increasing use of strain engineering for enhanced hole/electron mobilities in CMOS requires reduced thermal budget for the metastable $Si_{1-x}Ge_x$-structures to avoid lattice relaxation induced defect generation. The thermal budget is also closely connected with boron outdiffusion. There is also considerable interest in the selective growth of highly p-type and n-type doped SiGe-structures with low pressure chemical vapour deposition (LPCVD) (see also chapter 7).
Another requirement is the deposition of highly doped Si films on already fabricated structures (e.g. vertical SiGe-diodes or poly-electrodes) that require reduced thermal budget processes. The vertical stacks of SiGe-tunnel diodes or transistors require highly conducting Si top electrodes that must be deposited without degrading the sharpness of the underlying structures.

8.1 Growth of highly B-doped silicon with disilane (Si_2H_6)

We investigated the following process parameters:

- Deposition temperature: 600 °C,
- Process gas flows: 6/2 slm H_2, 1000 sccm Si_2H_6 (5% in H_2), 0 sccm - 500 sccm B_2H_6/H_2 500 ppm
- Total process pressure 10 Torr

In Fig. 8.1.1 the SIMS depth-profile of an epitaxially grown B-doped Si layer is depicted:

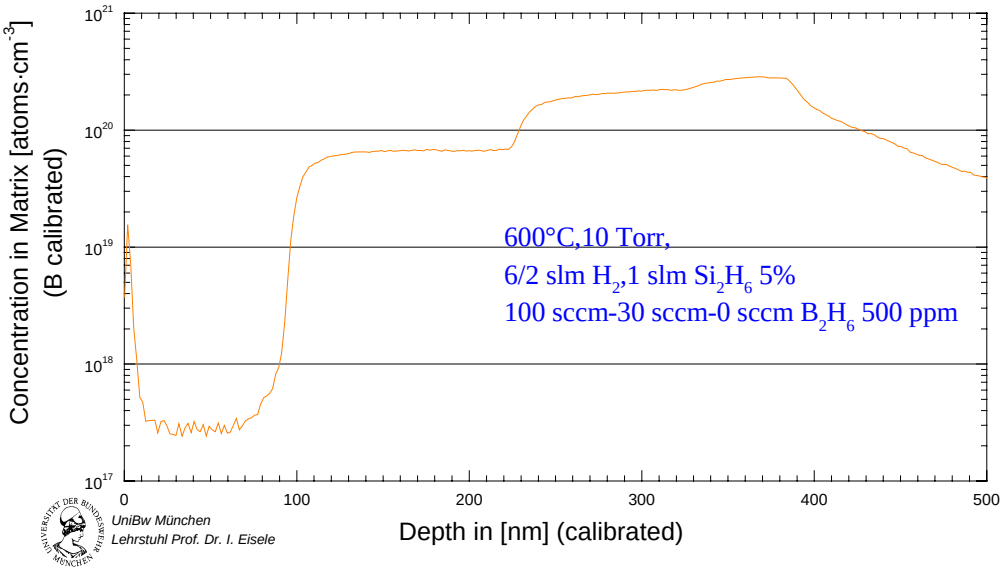

Fig. 8.1.1: SIMS-profile of a B-cascade in an epitaxial layer grown at 600 °C from Si_2H_6 and B_2H_6.

The B-profiles are shallow and abrupt and can be correlated easily to the B_2H_6–flows: 100 sccm of B_2H_6 lead to a B–concentration of (2-3)*10^{20}/cm^3, 30 sccm to 8*10^{19}/cm^3, 0 sccm to the baseline of our SIMS set-up. The corresponding deposition rates are 6.7 A°/s, 5.6 A°/s, 0.37 A°/s, respectively.

Fig. 8.1.2 shows the SIMS-profile of a B doped epitaxial layer grown at 600 °C from Si_2H_6 and B_2H_6. The measured signal corresponds to a constant doping with a concentration of 8*10^{20}/cm^3.

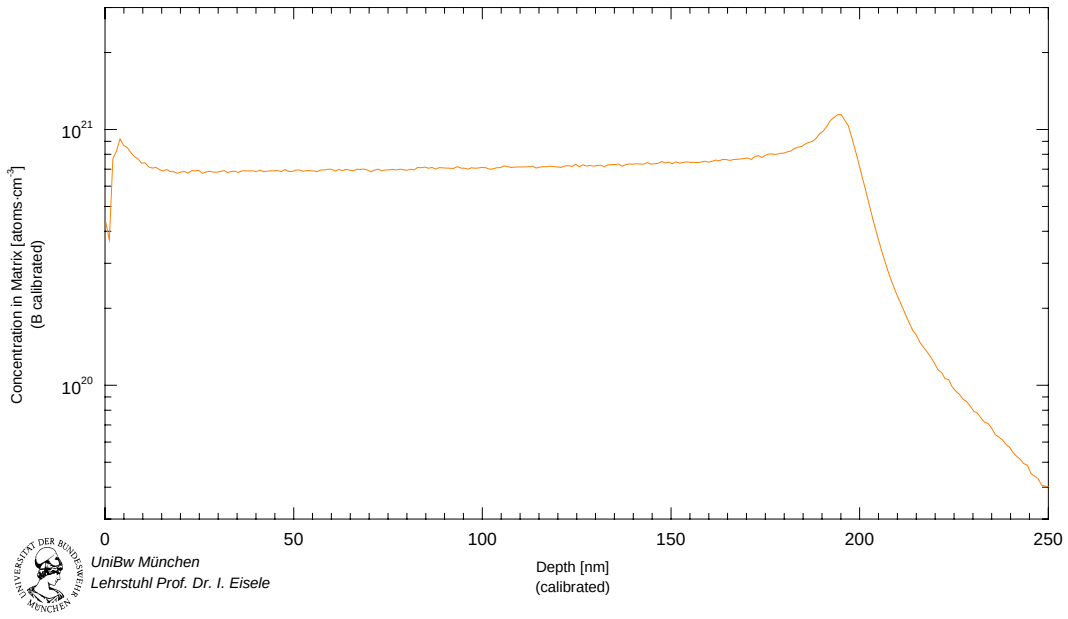

Fig. 8.1.2: SIMS-profile of a B doped epitaxial layer grown at 600 °C from Si_2H_6 and B_2H_6.

For resistivity measurements 4-point probing was performed. With known layer thickness a resistivity of 0.7 mΩ cm was achieved. Regarding the relation between B-concentration and resistivity, the so called “Irvin-curves” [1], an active B-concentration of (3-4)*10^{20}/cm^3 could be achieved. This value and the active B-concentrations of the dichlorosilane based processes discussed in chapter 7.1 are compared to solid-solubility-limits from ref. [2] in Fig. 8.1.3. The values are clearly in excess of equilibrium solid solubility. This implies that B incorporation is kinetically controlled in this process regime. The deposition temperature may be too low to reach thermodynamically equilbrium. In contrast to that the doping limits for ion implantation are derived from thermodynamically solid-solubility considerations. The reason for this is the high-temperature step after ion implantation that brings the silicon crystal and dopant into thermal equilibrium. An important consequence of this observation is that the “frozen” crystal stemming from low-temperature in-situ doped epitaxy may have an active dopant concentration much higher than achievable with convential ion implantation.

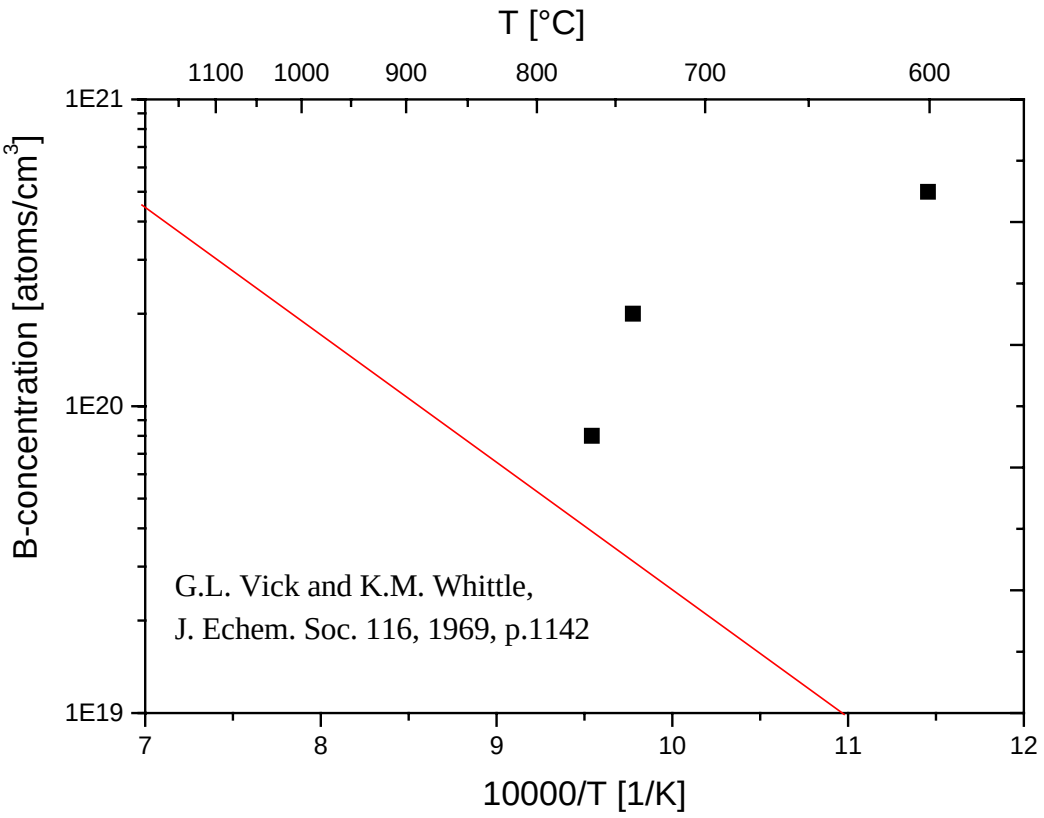

Fig. 8.1.3: Active B-concentration over growth temperature. The red line is the solid-solubility limit from ref. [2].

These results can be summarized as follows:

- B incorporation in the range > $5*10^{20}/cm^3$ is possible. Very high dopant activation down to a resistivity of 0.7 mΩ cm can be achieved. This values are the lowest resistivities published for epitaxially grown B-doped silicon to the best of the author's knowledge.

- Low-temperature B-doped epitaxy is able to outnumber the thermodynamic solid-solubility limit for B.

- The disilane-diborane-system provides reasonable deposition rates even for the low-temperature of 600 °C. Sufficient homogeneity over the wafers, no loading effects could be observed.

- Specular surfaces indicate reasonable crystal quality.

- No selectivity with respect to silicon dioxide could be observed yet.

8.2 Growth of highly As-doped silicon with disilane (Si_2H_6)

We investigated the following process parameters:

- Deposition temperature: 520 °C to 640 °C.
- Process gas parameters: 6/2 slm H_2, 1000 sccm Si_2H_6 (5% in H_2), 500 sccm AsH_3/H_2 1000 ppm or 10000 ppm as shown.
- Total process pressure 10 Torr.

Substrates were thermally oxidized and patterned as described in chapter 4.5. All samples showed silicon deposition on the silicon dioxide mask. The thicknesses were measured by spectral ellipsometry using the procedure described in chapter 4.3 and are depicted in Fig. 8.2.1. No variation of layer thickness over the patterned wafer could be observed. In the seed windows all layers showed specular surfaces indicating epitaxial crystal quality. For thickness determination mechanical stylus profiling on several structures on the mask was performed following the procedure described in chapter 4.5. No loading effect (variation of layer thickness due to window size and mask geometrie) could be observed. Fig. 8.2.1 shows the growth rates for the above process parameters.

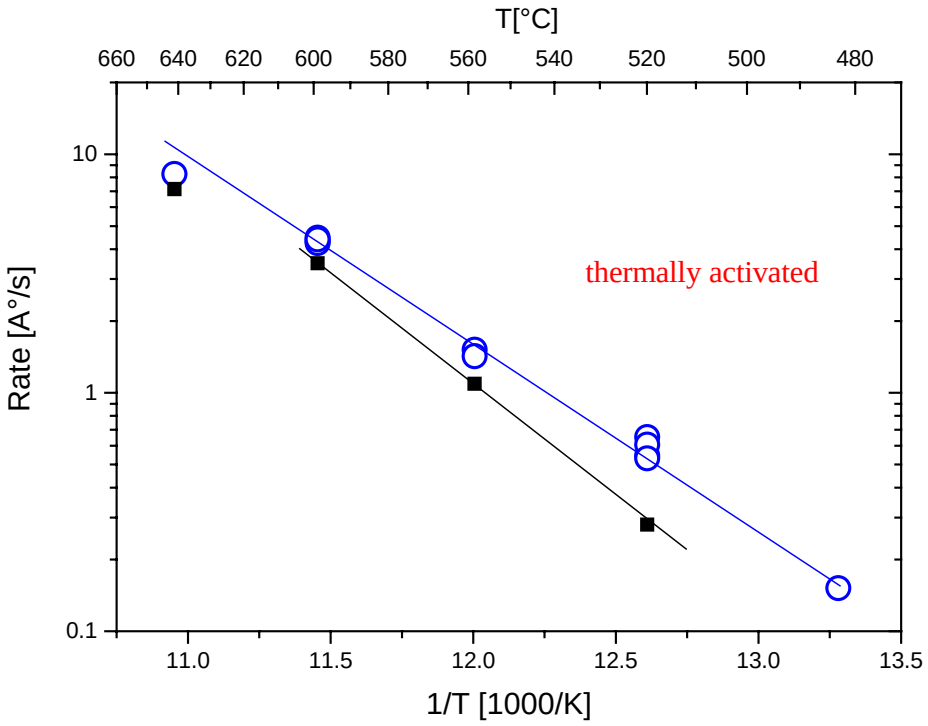

Fig. 8.2.1: Deposition rates for arsenic doped silicon as a function of inverse temperature. Open circles: amorphous/poly, full squares: epitaxial.

An Arrhenius type kinetic activated behaviour is observed for deposition on the silicon dioxide and for epitaxial deposition in the seed windows. The activation energies are 36 kcal/mol, 43 kcal/mol, respectively.

Nakazawa investigated the deposition of amorphous Si films grown with Si_2H_6 and reports an activation energy of 33 kcal/mol [3]. Sinniah et al. reported an activation energy of 47 kcal/mol for hydrogen absorption from the Si(100)-surface [4]. This indicates that the rate limiting step of the epitaxial growth regime in the seed windows is closely connected to hydrogen desorption.

The arsenic doping efficiency for the epitaxial layers was evaluated with SIMS-measurements. Fig. 8.2.2 contains the As-concentrations of the above mentioned epitaxial layers. Concentrations show a strong increase with dropping growth rate. On the other hand switching from 500 sccm AsH_3/H_2 1000 ppm to 500 sccm AsH_3/H_2 10000 ppm also results in a strong increase of arsenic incorporation. It is interesting to note that for constant partial pressures of the process gases the As-concentration is exponentially dependent on temperature.

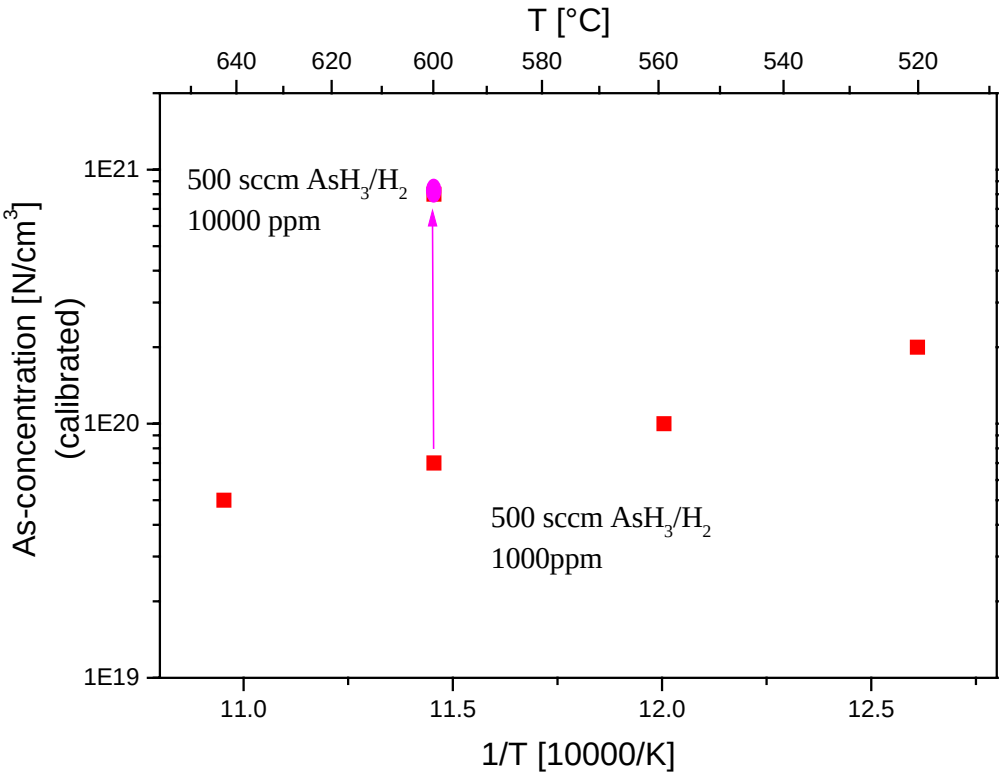

Fig. 8.2.2: As-concentrations for epitaxial siliconas a function of inverse temperature.

So far Si_2H_6 related AsH_3 doping shows much higher deposition rates, very high doping efficiency and specular surfaces compared to dichlorosilane or SiH_4 related AsH_3 doping (see chapter 7). The SIMS-profile of an As doped Si layer grown from Si_2H_6 and AsH_3 is depicted in Fig. 8.2.3. As can be clearly seen, the As-related signal is constant with a concentration of (5-6)*10^{20}/cm^3. For resistivity measurements 4-point probing was performed. With known layer thickness (gravimetric weight gain) a resistivity of 0.7 mΩ

cm was achieved. Regarding the relation between As-concentration and resistivity [1], an active As-concentration of around $2*10^{20}/cm^3$ could be achieved. This is the best value reported in literature to the best of the author's knowledge.

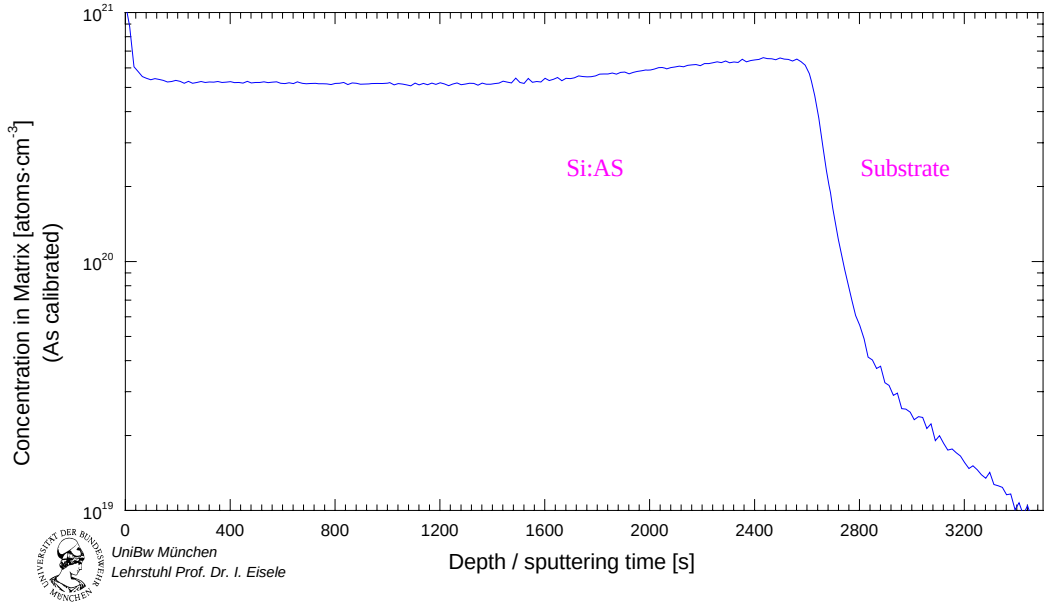

Fig. 8.2.3: SIMS-profile of As-doped epitaxial silicon layer.

Specific resistivities were evaluated by 4-point-probing . Regarding the relation between As-concentration and resistivity, the so called "Irvin-curves" [1], the active As-concentrations were evaluated as shown in Tab. 8.2.1:

T[°C]	600	600	560	520
As-conc. [n/cm_3]	$(5\text{-}6)*10^{20}$	$7*10^{19}$	10^{20}	$2*10^{20}$
Active As [n/cm_3]	$2*10^{20}$	$7*10^{19}$	10^{20}	Ca. $1.5*10^{20}$
Resistivity[mΩ cm]	0.7	1.1	0.9	0.8

Tab. 8.2.1: Resistivities compared to active and incorporated As-concentrations for epitaxial silicon.

These values are compared to solid-solubility-limits from ref. [5] in Fig. 8.2.4. The values are clearly in excess of equilibrium solid solubility. This implies that As incorporation is kinetically controlled in this process regime. The deposition temperature may be too low to reach thermodynamic equilbrium. In contrast, the doping limits for ion implantation are derived from thermodynamically solid-solubility considerations. The reason for this is the

high-temperature step after ion implantation that brings the silicon crystal and dopant into thermal equilibrium. An important consequence of this observation is that the "frozen" crystal stemming from low-temperature in-situ doped epitaxy may have an active dopant concentration much higher than achievable with convential ion implantation.

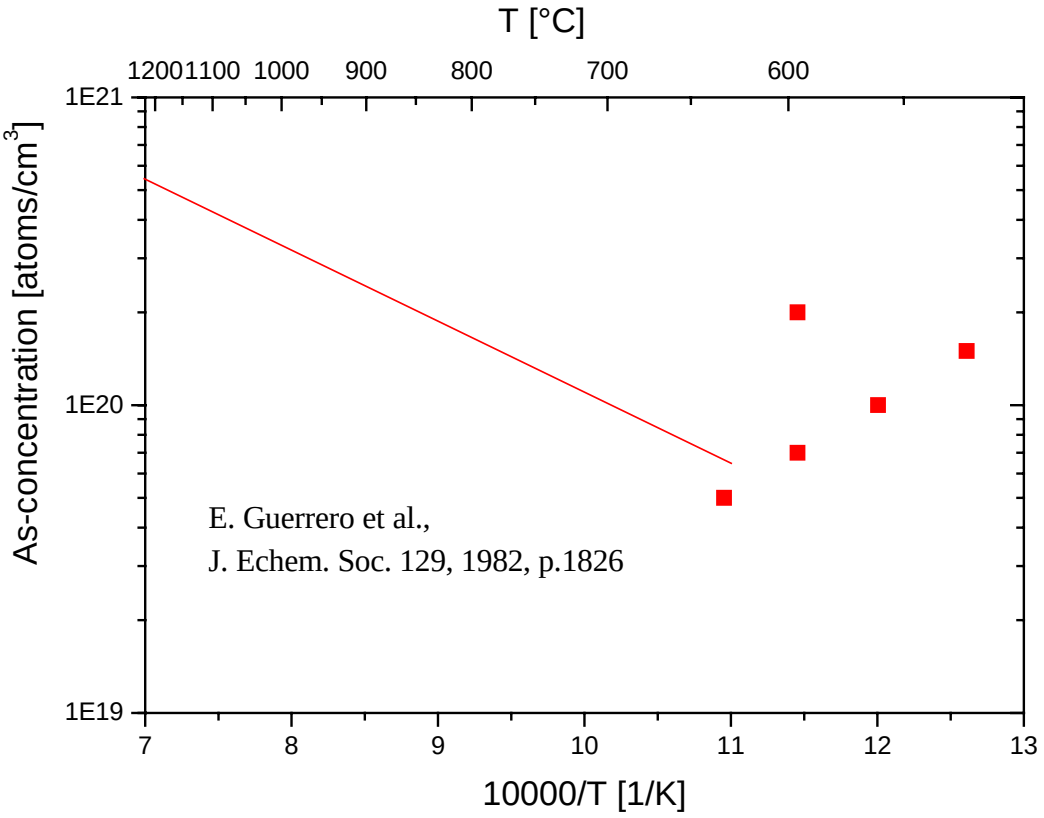

Fig. 8.2.4: Active As-concentration versus inverse growth temperature. The red line is the solid-solubility limit from ref. [5].

In chapter 3.5.5 the following mechanism for doping from As was outlined: A stable monolayer of As is built rendering SiH_4 from further adsorbing. In this case only the more reactive species like SiH_2, SiH_3 contribute to the growth (see chapter 3.5.1) because they have a much higher sticking coefficient on As poisoned Si(100)-surfaces. In addition no loading effects (inhomogeneities of layer thickness across the substrate) could be observed. These also seem to be strongly connected to SiH_2, SiH_3 radicals. The disilane molecule readily decomposes into the very reactive radicals SiH_3 and SiH_2 (see chapter 3.5.2). This seems to be the reason for the superior As doping behaviour and homogeneity of layer thickness of disilane related Si growth in contrast to silane and DCS (see chapter 7).

These results can be summarized as follows:

- As incorporation in the range > $10^{20}/cm^3$ is possible. Very high dopant activation down to a resistivity of 0.7 mΩ cm can be achieved. This values are the lowest resistivities published for epitaxially grown As-doped silicon to the best of the author's knowledge. The decomposition pathway of the disilane molecule into the very reactive radicals SiH_3 and SiH_2 seems to be the reason for this superior As doping behaviour.

- Low-temperature As-doped epitaxy is able to outnumber the thermodynamic solid-solubility limit for As.

- The disilane-arsine-system provides reasonable deposition rates even for low-temperatures <= 600 °C. Sufficient homogeneity over the wafers.

- No loading effects could be observed.

- Specular surfaces indicate reasonable crystal quality.

- No selectivity with respect to silicon dioxide could be observed yet.

However, a selective process with superior doping and throughput properties compared to the DCS-based processes would be very desireable for the fabrication of source/drain-extensions for NMOS. The results lead us to the following suggestion to achieve selectivity: addition of selectivity enhancing HCl, 70 sccm at 640 °C.

Surprisingly, the deposited layer exhibited no difference compared to the chlorine-fee process. This may perhaps be explained by the fact that HCl-etching of Si is a strong temperature activated process. From that point of view it is a useful suggestion to switch to higher process temperatures. More investigations are necessary to exploit the above mentioned promising results.

9. Conclusions & Outlook

The aim of this work was the development of low temperature processes in doped SEG[1]. The aggressive downscaling of CMOS- and DRAM-structures puts strict requirements on doping shallowness and abruptness of source/drain-junctions. Because diffusion of dopants (especially boron) is strongly temperature activated, the temperature for doping (and subsequent processes) has to be lowered considerably to fulfill the IRTS[2]-requirements for the coming technology nodes. This is not possible for the high-temperature anneal required after conventional ion implantation, but in-situ doped SEG is a promising technology.
Another reason for the demand of low temperature processes is the increasing use of pseudomorphically grown metastable $Si_{1-x}Ge_x$ for strain engineering to enhance hole /electron mobilities in the channel of MOSFET's. These require reduced thermal budget to avoid lattice relaxation induced defect generation. Lowering growth temperature below 700 °C is necessary in a lot of cases. This is also urgent in the fabrication of vertical devices that are based on $Si/Si_{1-x}Ge_x$ epitaxial layer stacks.
Another important consequence of downscaling CMOS is the necessity for alternative gate dielectrics, so called high-k materials. The thermal stability of the material has to withstand the thermal budget of all following processes. A high-temperature annealing step after ion implantation will drastically limit the possible choice of the material.
In this work it has been shown that selective epitaxy in CVD provides a way to deposit $Si/Si_{1-x}Ge_x$ source/drain-junctions with high and abrupt doping levels and low thermal budget.

The minimum thermal budget to achieve contamination-free silicon surfaces prior to expitaxy could be estimated in a commercial LPCVD-system to 120 s at 775 °C. For silicon dioxide removal the oxygen pressure is the key factor which is also the case for cleaning under UHV conditions. The reaction path $Si + SiO_2 = 2SiO$ seems to be fundamental for silicon substrate cleaning under hydrogen, argon and UHV ambient. Etching of silicon dioxide by hydrogen can be ruled out as the main reaction at temperatures ≤ 900 °C. The presence of hydrogen in the growth enviroment leads to a shift in the steady-state boundary for achieving oxide free silicon (100) surfaces under less stringent requirements. Hydrogen is also responsible for a complete removal of carbon impurities. Silicon surface cleaning assisted by silane or germane did not suceed because of the residual oxygen partial pressure. To achieve contamination-free silicon surfaces, the leakage has to be lowered significantly in future LPCVD-systems.
An industrial CMOS compatible selective epitaxial process for the fabrication of source/drain-extensions fulfilling the IRTS requirements of the coming technology nodes has been demonstrated. We investigated the boron doping behaviour in silicon epitaxial layers for different process temperatures. A dichlorosilane chemistry without additional HCl has been used. Selectivity with respect to silicon dioxide was achieved for Si:B and

[1] Selective Epitaxial Growth.
[2] International Technology Roadmap for Semiconductors

$Si_{1-x}Ge_x$:B. For Si:B and $Si_{1-x}Ge_x$:B sufficient homogeneity over the patterned wafer could be achieved. The addition of germane to the growth enviroment improves deposition rate, especially at temperatures below 700 °C. With TEM investigations very low defect levels could be confirmed. Dropping the process temperature to 625 - 550 °C leads to very smooth surfaces, even for very high boron-doping levels; this is attributed to the absence of temperature-activated lattice relaxation. Up to 18% Ge the resistivity drops with rising Ge-content. This is consistent with the results for a silane-germane-diborane chemistry and may be independent of precursor choice. The resistivity achieved (0.8 mΩ cm for Si:B and 0.6 mΩ cm for $Si_{1-x}Ge_x$:B) meets the ITRS requirements of the coming technology nodes. It is desirable to try additional HCl for achieving selectivity to silicon nitride in future. In a further process sequence halo, extensions and source/drain of PMOS may be deposited by subsequent selective epitaxial growth. The increasing use of SOI-(silicon-on-insulator)-wafers induces the demand to adapt the process to buried oxide of different thicknesses.

For investigation of the n-type doping behaviour the silicon precursors silane, dichlorosilane are compared in terms of doping efficiency, deposition rate and selectivity with respect to silicon dioxide. For LPCVD at 10 Torr the arsenic dopant concentration was always very low ($10^{17}/cm^3$). For 640 Torr the arsenic dopant incorporation shows a temperature dependence ranging from $10^{19}/cm^3$ (775 °C) up to $2*10^{21}/cm^3$ (600 °C). The doping transition lenghts ranged from about 20 nm (DCS/GeH_4) up to more than 50 nm for silane. They are drasically reduced by an arsine build-up process. This doping behaviour can be explained in terms of the electronic behaviour of the surface. Selectivity with respect to silicon dioxide was achieved for DCS, but not for silane. For i-Si and i- $Si_{1-x}Ge_x$ sufficient homogeneity over the patterned wafer could be observed. Selective growth with arsine doped Si and SiGe layers has also been achieved, but considerable loading effects were observed. The growth rates rise strongly with smaller window size. Since the growth regime is switching from surface controlled to mass transport controlled for doping with group-V-hydrides, another precursors with another chemistry, e.g. disilane or another dopant gas may be the appropriate choice. Adding germane drastically reduces the resistivity to 5 mΩ cm while keeping a much higher deposition rate. To further lower the resistivity the use of phosphine as an alternative doping source is desirable.

The silicon deposition from disilane-diborane and disilane-arsine provides reasonable deposition rates even for low-temperatures ≤ 600 °C. Sufficient homogeneity over the wafers could be observed. Doping with diborane and arsine showed excellent dopant activation down to a resistivity of 0.7 mΩ cm. The doping efficiency is compared to the thermodynamic solid solubility limit and discussed in terms of metastable structures. This values are the lowest resistivities published for epitaxially grown B- and As-doped silicon to the best of the author's knowledge. Low-temperature B- and also As-doped epitaxy is able to outnumber the thermodynamic solid solubility limit for B, As, respectively. Specular surfaces indicate reasonable crystal quality. The reason for this superior n-type doping behaviour is that the disilane molecule readily decomposes into the very reactive radicals SiH_3 and SiH_2. No selectivity with respect to silicon dioxide could be observed. Howewer, a selective process with superior doping and throughput properties compared to

the DCS-based processes would be very desireable for the fabrication of source/drain-extensions for NMOS. A first experiment with the addition of selectivity enhancing HCl exhibited no difference compared to the clorine-fee process. This may perhaps be explained by the fact that HCl-etching of Si is a strongly temperature activated process. From that point of view future investigations will focus on process temperatures ≥ 680 °C.

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