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ARTICLE

Piezoresistive Platinum Diselenide Pressure Sensors with Reliable High Sensitivity and Their Integration into Complementary Metal-Oxide-Semiconductor Circuits

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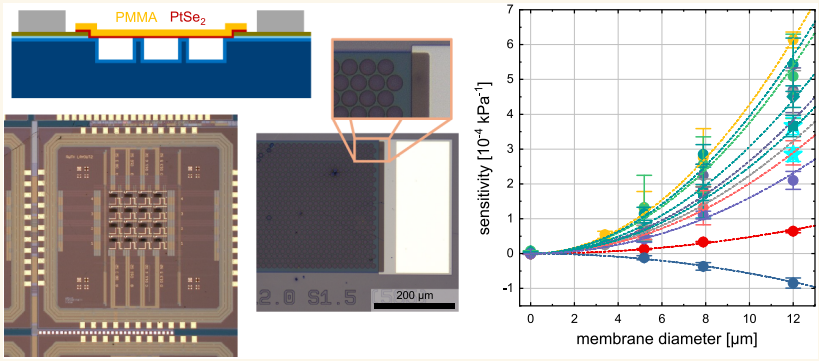

ABSTRACT: Membrane-based sensors are an important market for microelectromechanical systems (MEMS). Two-dimensional (2D) materials, with their low mass, are excellent candidates for suspended membranes to provide high sensitivity, small footprint sensors. The present work demonstrates pressure sensors employing large-scale-synthesized 2D platinum diselenide ($PtSe_2$) films as piezoresistive membranes supported only by a thin polymer layer. We investigate three different synthesis methods with contrasting growth parameters and establish a reliable high yield fabrication process for suspended $PtSe_2$/PMMA membranes across sealed cavities. The pressure sensors reproducibly display sensitivities above 6×10^{-4} kPa^{-1}. We show that the sensitivity clearly depends on the membrane diameter and the piezoresistive gauge factor of the $PtSe_2$ film. Reducing the total device size by decreasing the number of membranes within a device leads to a significant increase in the area-normalized sensitivity. This allows the manufacturing of pressure sensors with high sensitivity but a much smaller device footprint than the current state-of-the-art MEMS technology. We further integrate $PtSe_2$ pressure sensors with CMOS technology, improving the technological readiness of $PtSe_2$-based MEMS and NEMS devices.

KEYWORDS: *platinum diselenide, pressure sensor, 2D materials, MEMS, CMOS*

Research in micro- and nanoelectromechanical systems (MEMS and NEMS) has increasingly included two-dimensional (2D) materials. Their crystalline, layered nature promises decisive advantages, especially in the area of sensing.[1−3] One outstanding property of several 2D materials is their piezoresistivity, which can be more fully exploited due to the atomic material thinness. Piezoresistive sensors utilizing 2D materials have been demonstrated in the form of graphene-

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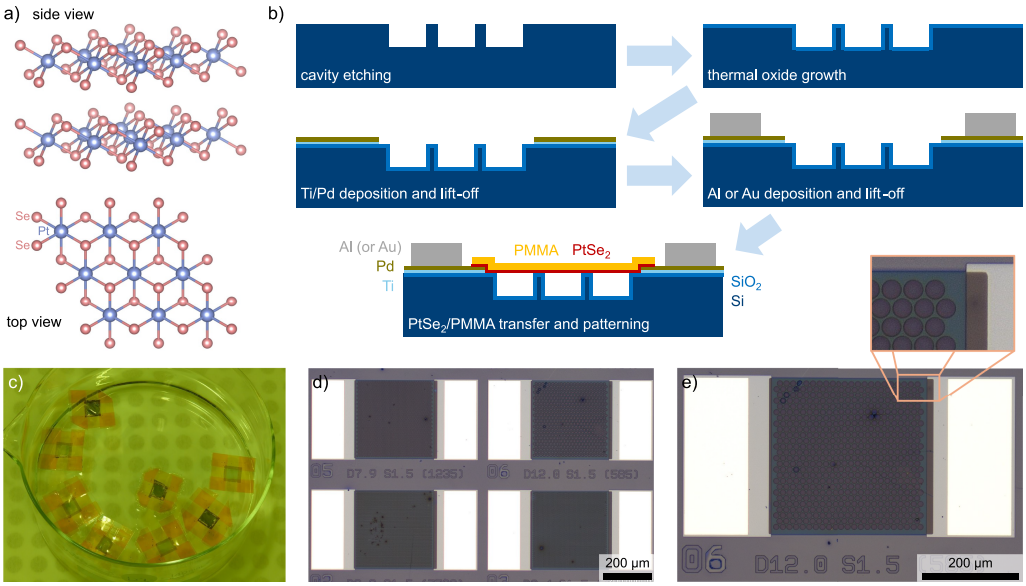

Figure 1. (a) Atomic structure of $PtSe_2$ (side view of two monolayers and top view of a single monolayer). Crystal data from the Materials Project,[51,52] graphical representation created using VESTA.[53] (b) Cross-sectional schematics of the process flow for the fabrication of $PtSe_2$/PMMA pressure sensors. (c) Photograph of several $PtSe_2$/PMMA films inside their transfer frames after delamination from the growth substrate. (d-e) Optical microscopy images of $PtSe_2$/PMMA membrane devices on chip #182.2 with various membrane diameters. Images of 17 different chips are shown in Figure S2.

Table 1. Overview of the Fabricated and Analyzed Pressure Sensor Chips[a]

source	synthesis method	chip name	approx $PtSe_2$ thickness	GF	contact metal stack
University of the Bundeswehr Munich	thermally assisted conversion (TAC)	#133.2	12.2 nm	−6.2	Ti/Pd + Au
		#151.2	23.5 nm	+4.2	Ti/Pd + Au
		#180.3	6.1 nm	−33.2	Ti/Pd + Al
		#182.2	4.2 nm	−46.8	Ti/Pd + Au
		#183.4	3.3 nm	−55.6	Ti/Pd + Au
		#184.3	4.2 nm	−47.9	Ti/Pd + Au
		#190.2	14.9 nm	−32.4	Ti/Pd + Au
		#216.3 *	3.5 nm	−30.6	Ti/Pd + Au
		#220.1			Ti/Pd + Al
		#220.3			Ti/Pd + Au
		#220.4			Ti/Pd + Au
		#221.1 **			Ti/Au
		#221.2 **			Ti/Au
		#249.1	20 nm	−29.6	Ti/Pd + Au
Thales R&T	molecular beam epitaxy (MBE)	#192.3	8.5 nm	unknown	Ti/Pd + Al
		#192.4			Ti/Pd + Au
		#195.8	7 nm	−38.2	Ti/Pd + Au
		#195.9			Ti/Pd + Au
University of the Bundeswehr Munich	metal−organic chemical vapor deposition (MOCVD)	#266.4	5 nm	−36.0	Ti/Pd + Au
		#268.6	3.5−5 nm	−31.3	Ti/Pd + Au

[a]Chip #216.3 (marked with *) featured a modified device design with reduced membrane area. Chips #221.1 and #221.2 (marked with **) were CMOS ASIC substrates featuring a different device design from all other chips.

based pressure sensors[4−14] and accelerometers,[15] as well as pressure[16] and mass sensors[17] made from one of the best-studied 2D materials, molybdenum disulfide (MoS_2). Noble-metal dichalcogenides (NMDCs), a subgroup of transition-metal dichalcogenides (TMDCs) in which the metal is a noble metal such as platinum (Pt) or palladium (Pd), have also recently gained attention. The piezoresistive properties of platinum diselenide ($PtSe_2$, shown with its atomic structure in Figure 1a) have been studied,[18,19] and $PtSe_2$-based piezoresistive pressure sensors have been demonstrated.[20,21] Although the resonance[22,23] and capacitance[24−28] of 2D membranes have also been used as pressure sensor mechanisms, the piezoresistivity of 2D materials is a simple transduction mechanism for sensors with high sensitivity. A piezoresistive pressure sensor based on the NMDC palladium diselenide ($PdSe_2$) has been shown to reach a sensitivity of 3.9 × 10^{-4} kPa^{-1}; however, a silicon nitride (SiN_x) membrane of very large dimensions was used as a mechanical support.[29] Utilizing the 2D material itself as a membrane instead would

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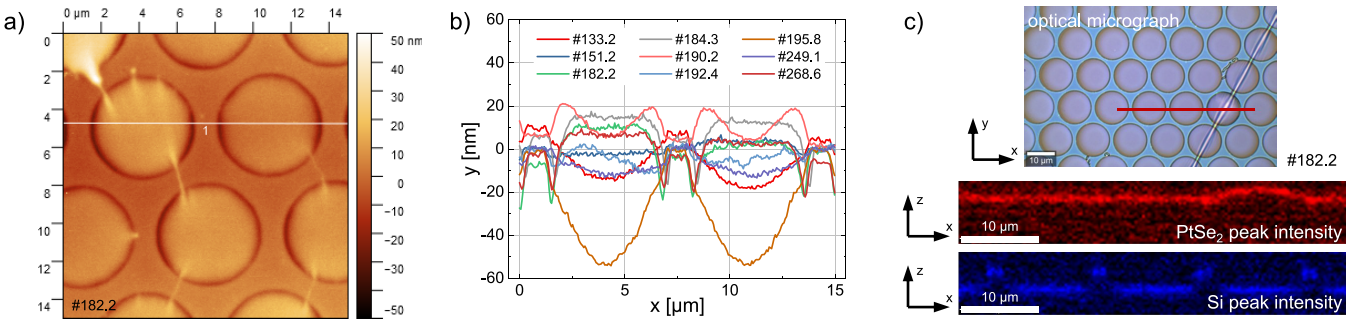

Figure 2. (a) AFM height map of a device with suspended $PtSe_2$/PMMA membranes. AFM scan images of 8 additional chips are shown in Figure S3. (b) Height profiles extracted from the AFM height maps of the 9 chips (Figure S3). (c) Raman depth scan along a line on a device with $PtSe_2$/PMMA membranes. The scan line is shown in red on the microscope image. The intensities of the main $PtSe_2$ peak (E_g peak at ~178 rel. cm^{-1}) and the Si peak (at 520 rel. cm^{-1}) are shown in the two maps in red and blue.

truly exploit the advantages of 2D materials in membrane-based sensors.

In our study, we aim to approach the ultimate limit of 2D membrane-based sensors. We used nanocrystalline layered $PtSe_2$ from three different synthesis methods: thermally assisted conversion (TAC) of predeposited Pt layers,[30−33] metal−organic chemical vapor deposition (MOCVD),[34] and molecular beam epitaxy (MBE).[35−37] These three synthesis methods each have their own advantages and disadvantages. While MBE and MOCVD are more likely to result in well-aligned $PtSe_2$ layers with larger crystallites (grains), TAC is very easily scalable to industry-relevant wafer sizes and can simultaneously produce high-quality $PtSe_2$ films at low temperature (<450 °C), compatible with complementary metal-oxide-semiconductor (CMOS) back-end-of-line thermal budgets. Based on our knowledge of the process of fabricating suspended 2D material membranes on sealed cavity substrates,[21,38,39] we constructed and characterized pressure sensors from a total of 13 different growth batches with different synthesis parameters. The suspended $PtSe_2$ membranes were examined by means of atomic force microscopy (AFM) and Raman spectroscopy depth scans. The pressure sensors were measured in an automated pressure chamber, and their sensitivity was extracted. In parallel, the piezoresistive gauge factor (GF) was determined from $PtSe_2$ samples of the same growth batches, and its influence on the sensor sensitivity is shown. Finally, we also show $PtSe_2$ pressure sensors fabricated by the same methods on top of CMOS application-specific integrated circuit (ASIC) substrates from a semiconductor foundry. This demonstrates that our technology can be implemented in well-established CMOS fabrication lines.

RESULTS

$PtSe_2$/Poly(methyl methacrylate) (PMMA) membrane-based pressure sensors with closed cavities and bottom contacts were fabricated as described in the Methods section. $PtSe_2$ synthesized by TAC, MOCVD, or MBE was transferred to target substrates and thereby suspended above pre-etched cavities using a frame-based transfer process and a subsequent patterning step. A schematic of the device cross section is shown in Figure 1b together with the process flow. A summary of the fabricated and analyzed chips is shown in Table 1.

Each chip had up to 48 sensor devices depending on the area covered with $PtSe_2$ during the transfer, with six different membrane diameters ranging from 1.5 to 12 μm. Each of the devices comprised arrays of these suspended $PtSe_2$/PMMA membranes. The yield of intact membranes after transfer and patterning (lithography, etching, and resist removal) was generally high. Broken membranes occurred only in places where small bubbles or wrinkles had formed during transfer or where particles prevented good adhesion of $PtSe_2$ to SiO_2. In those places, liquid chemicals (developer, solvent) were able to penetrate the interface and delaminate the $PtSe_2$. The fraction of devices with an estimated 90% or more of intact membranes with respect to the number of devices covered with $PtSe_2$ after transfer ranged between only a few % to 100%, with its mean at approximately 71% (see left side of Figure S1). However, during pressure sensor characterization at a later stage, a large fraction of all wire-bonded devices was measured successfully, no matter if only few membranes were intact (see right side of Figure S1). This shows that only a small number of intact membranes (in theory, one) is sufficient for a highly sensitive $PtSe_2$-based pressure sensor.

Variations in device performance caused by the manual nature of the transfer process could be minimized in the future when large-scale, nonmanual transfer processes are utilized. Such processes already exist for 2D materials[40] and are further explored in research such as in the European (Experimental) Pilot Line Project.[41]

Optical microscope images of the fabricated devices are shown in Figure 1d-e and Figure S2. The color difference between chips originates from factors such as the difference in $PtSe_2$ thickness in the channel areas and by overetching during the patterning process in the surrounding areas of the SiO_2 substrate.

Atomic force microscopy (AFM) confirmed the suspended nature of the $PtSe_2$/PMMA membranes above the void, 2.0−2.5 μm deep cavities, as shown in Figure 2a and Figure S3. The membranes show a rather flat topography, with a maximum deflection of approximately 50 nm across a scanned membrane diameter of 5.2 μm, as depicted in Figure 2b. The difference in the deflection and the surface morphology between the chips can be attributed to small changes in the manual transfer process, differences in the adhesion of $PtSe_2$ to its growth substrate and therefore different applied tensions during delamination, and differences in the nanocrystalline structure of the various $PtSe_2$ films.

Additionally, Raman depth scanning[42] was performed on devices with 12 μm membrane diameters. This method uses several line scans with consecutive laser focus planes in the z-direction to reconstruct two-dimensional images of the device cross sections (see Figure 2c and Figure S5). The intensity

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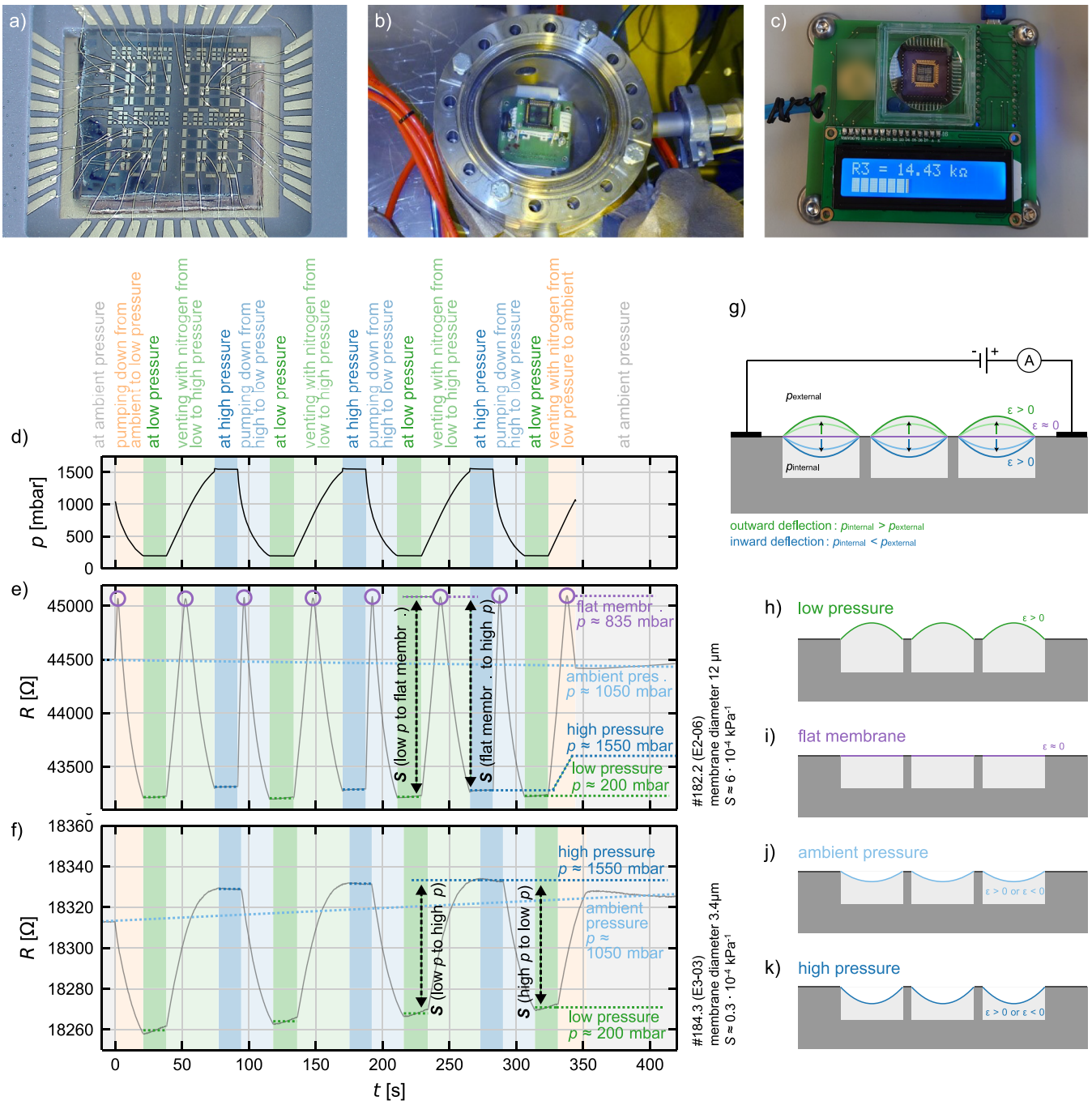

Figure 3. Measurements of the $PtSe_2$/PMMA pressure sensors. (a) A $PtSe_2$ pressure sensor chip wire bonded into a chip carrier. (b-c) Photographs of the pressure chamber for sensor characterization and the pressure sensor demonstrator, respectively. (d) An example measurement curve of the change in pressure over time as recorded by a commercial reference sensor. Note that the small jumps at high pressure are interpreted as measurement artifacts caused by the switching of the electronic valves, not depicting the actual pressure inside the chamber at the particular moments in time. (e) An example measurement curve of a $PtSe_2$/PMMA pressure sensor with a large membrane diameter (12 μm). The resistance is maximized when the membranes are flat, as indicated by the purple circles. For both the low- and high-pressure cases, tensile strain dominates along the $PtSe_2$, and the resistance decreases. The sensitivity between the resistance maxima of the flat membranes and the levels of low and high pressure was extracted as indicated. The device has a high sensitivity of approximately 6×10^{-4} kPa^{-1}. (f) Exemplary measurement curve of a $PtSe_2$/PMMA pressure sensor with a small membrane diameter (3.4 μm). Due to the combination of tensile and compressive strains, high pressure leads to an increase in the measured resistance, while low pressure leads to a decrease. The sensitivity is extracted as indicated between the levels of high and low pressure. The device has a low sensitivity of approximately 0.3×10^{-4} kPa^{-1}. (g) Schematic of the working principle of the piezoresistive pressure sensor. (h-k) Sketched membrane deflection for the cases of low pressure, a flat membrane, ambient pressure, and high pressure, as indicated in the measurement curves in (e) and (f).

maps of the $PtSe_2$ Raman peak (E_g peak at ~178 rel. cm^{-1}) show that the $PtSe_2$/PMMA membranes are freely suspended, while the intensity maps of the silicon (Si) Raman peak display the profile of the 2.0−2.5 μm deep cavities below.

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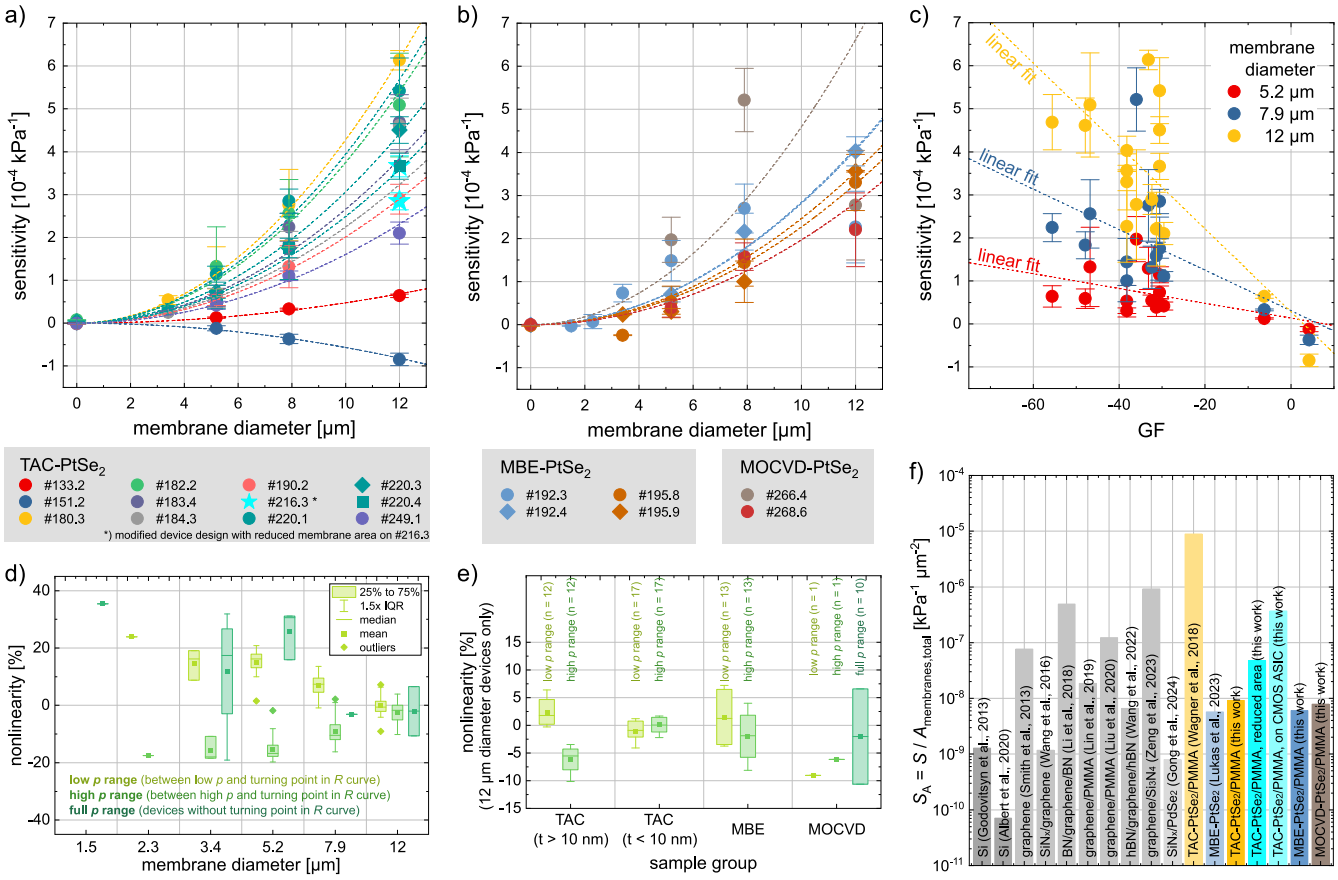

Figure 4. (a-b) Sensitivity of the $PtSe_2$/PMMA pressure sensors vs the membrane diameter of the respective device, plotted for 18 different chips. Parabolic fits (without offset and without linear terms) are shown for each chip. (c) Dependence of the sensitivity on the piezoresistive gauge factor (GF) of $PtSe_2$. The graph includes the data points from all chips from graphs (a) and (b), categorized by membrane diameter. Linear fits for the three different membrane diameters are plotted. In (a), (b), and (c), the error bars show the range of extracted sensitivity values for the individual devices. (d) Nonlinearity (NL) dependence on the membrane diameter. Depending on the sensor characteristics, the NLs extracted from the full pressure range or the two high- and low-pressure ranges are shown. (e) Boxplot of NLs extracted from all devices with the same membrane diameter of d = 12 μm, grouped by material growth and thickness range for TAC-$PtSe_2$. (f) Comparison of the mean sensitivity normalized to the membrane area (S_A) for various piezoresistive pressure sensors (see also Table 2).

Four-probe back-gated transfer measurements were conducted using six-port reference devices without membranes fabricated on the same substrates as the pressure sensors. The field-effect charge carrier mobility μ_F and sheet resistance R_{sheet} of the transferred $PtSe_2$ films were determined as described in the Methods section and are displayed in Figure S6. Most $PtSe_2$ films show R_{sheet} in the range of a few kΩ to a few 100 kΩ and a maximum μ_F between 1 and 12 $cm^2/(V\ s)$. One chip of MOCVD-$PtSe_2$ (#266.4) has a higher R_{sheet} of approximately 10 MΩ up to 1 GΩ and, at the same time, a very low μ_F.

The piezoresistive gauge factor (GF) was determined for all different batches of $PtSe_2$ films (except for one MBE film, for which no additional material from the same batch was available). The $PtSe_2$ was exposed to a defined strain, and the electrical resistance was measured, as described in the Methods section and shown in Figure S7, Figure S8, and Figure S9. The extracted GFs are listed in Table 1. The GF varies between the samples, ranging from −55.6 to +4.2, while most values are close to approximately −35. The origin of the spread of the GF is related to the layer thickness as well as the nanocrystalline structure of the $PtSe_2$ and is difficult to predict.[18,19] The GF is an important indicator of the resulting sensitivity of the membrane-based pressure sensor.

The wire-bonded pressure sensor chips were characterized in an automated pressure chamber with various gas pressures between 200 mbar and 1550 mbar (see Figure 3a-b). Pressure, temperature, and relative humidity were monitored by commercial reference sensors inside the chamber. For all measurements, the chamber was purged with nitrogen to ensure a low relative humidity (<15%) and therefore minimize the reaction of the sensor to a change in relative humidity. The temperature was stable between 22 and 25 °C. The chips were exposed to ambient light during the measurements, which, as verified in a reference measurement (see Figure S10a), did not lead to significant additional drifts of the sensor output due to its low intensity.

The device resistance was recorded while the pressure inside the chamber was cycled between low and high pressure (see Figure 3d-f as well as Figure S11 and Figure S12). Due to the difference in the pressure inside the cavities sealed by the $PtSe_2$ membranes, $p_{internal}$, and the external pressure $p_{external}$, the membrane is deflected and thereby strained. A schematic of this operation principle is shown in Figure 3g. The strain leads to a change in the electric resistance of $PtSe_2$, $\Delta R \propto GF \cdot \varepsilon$. The signal shape of the devices varies depending on several factors, mainly the membrane diameter of the device and the PMMA thickness, as previously analyzed and simulated.[21] In this study,

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ACS Nano 2025, 19, 7026−7037

the PMMA thickness was kept the same for all fabricated and measured chips: We used approximately 60 nm of PMMA A2 950k, which was selected as a compromise between sufficient mechanical stability for the transfer and sufficient thinness to ensure the high sensitivity of the sensors.

For a PMMA thickness of approximately 60 nm, the sensors exhibit two clearly distinguishable signal shapes, both of which are shown in Figure 3e-f. The device in Figure 3e has comparably large membranes with diameters of 12 μm. The $PtSe_2$ in this device dominantly experiences tensile strain in both directions of deflection (outward or inward for low and high pressures, respectively). Therefore, resistance minima can be observed for both high- and low-pressure cases in the R curve of this device, where the tensile strain is maximized and, due to the negative GF, the device resistance is minimized. The maxima in R are observed at a pressure of approximately 835 mbar, corresponding to the minima in tensile strain, i.e., a nondeflected, flat membrane. The exact pressure of the resistance maximum varies from device to device and depends on the pressure history. At an ambient pressure of approximately 1050 mbar, the membranes are therefore not unstrained but have already deflected inward. The different cases are shown in the schematics in Figure 3h-k. For the devices exhibiting the described signal shape, the sensitivity was extracted between the low pressure level and the flat-membrane resistance maximum, as well as between the mentioned resistance maximum and the high pressure level (as indicated in Figure 3e).

A different signal shape was observed for several devices with a smaller membrane diameter, such as for the device shown in Figure 3f with a membrane diameter of 3.4 μm. Here, the piezoresistively dominating type of strain changes from dominating tensile strain for the low-pressure case to a combination of tensile and compressive strain across each membrane (with a possible slight domination of compressive strain) for the high-pressure case. Compressive strain occurs in the $PtSe_2$ film due to its position at the bottom of the double-layer stack of $PtSe_2$ and PMMA, where the PMMA is approximately 3 to 18 times as thick as the $PtSe_2$. The dominating strain occurs around the edge of the membrane, as shown previously.[21,43] As a result, the measured devices show a resistance minimum for the low-pressure case and a resistance maximum for the high-pressure case, between which the sensitivity was extracted.

The extracted sensitivity is plotted against the membrane diameter in Figure 4a-b. The error bars show the ranges of the extracted sensitivities for each chip. A total of 264 devices across the 17 different chips with $PtSe_2$ from 13 different growth batches (i.e., various growth methods and/or growth parameters) were characterized, using the main device layout. Additionally, 14 devices without membranes were measured as reference devices and showed only a minor response with very low sensitivity, approximately 2 orders of magnitude lower than the sensitivity extracted from those devices with membranes, attributed to small changes in relative humidity (see four exemplary curves in Figure S13). These reference devices are plotted with a membrane diameter of zero in Figure 4a-b.

Generally, a trend of increasing sensitivity with increasing membrane diameter can be observed. This is expected due to the increase in strain with increasing membrane diameter.[21] Parabolic fits are calculated and plotted for all different chips, following the quadratic dependence of the membrane area on its diameter. However, multiple factors influence the sensitivity of the sensors in addition to the membrane diameter, such as the total active area (i.e., the area of the channel that is covered by intact membranes; see also Table S1), and processing variations, which cause differences in the pretension of the membranes. The parabolic fit nevertheless matches the data well for many chips.

One chip (#151.2) shows an opposite signal shape, and therefore, a sensitivity with the opposite sign is extracted (see Figure S11c and Figure 4a). This can be explained by the GF of this $PtSe_2$ film which, in contrast to all other samples, has a positive sign. Computational analysis[19] predicts GF of both signs in nanocrystalline $PtSe_2$, depending on the prevalent stacking phases. The dependence of the sensitivity on the GF is further shown in Figure 4c, where the sensitivity values of all the measured devices with the three largest membrane diameters are plotted against the GF. Despite the significant spread of the data, linear fits visualize the clear trends of higher sensitivities with larger membrane diameters as well as higher sensitivities with larger GF magnitudes.

The membrane thickness t is expected to influence the sensitivity as well, as an increasing t leads to a less flexible membrane. Here, the influence of the PMMA layer is neglected due to its significantly lower Young's modulus and therefore higher flexibility. According to theoretical calculations,[7,44] the sensitivity S should follow $S \propto t^{-2/3}$, as plotted in Figure S14. Several data points deviate from the fit line significantly, especially the data point of sample #151.2 with negative S and positive GF, in contrast to all other data. This shows that the GF clearly is an influence on S. Furthermore, there is a general trend of higher magnitude GF with decreasing $PtSe_2$ film thickness t, complicating the differentiation between the effects of GF and t on S.

The device design with a large $PtSe_2$ channel and hundreds to thousands of membranes in each single device (see Table S1) has the disadvantage of low sensitivity normalized to the membrane area $S_A = S/A_{membranes,total}$ but was chosen earlier when the transfer process still resulted in lower yields of intact membranes. To show that a much higher S_A is possible with the demonstrated technology, one chip (#216.3) was fabricated with enlarged Ti/Pd contact pads, covering significant parts of the cavity array and therefore reducing the active membrane area of the devices. Details on this chip can be found in Figure S15. The extracted sensitivity S of the two measured devices with reduced active membrane areas was on the same order of magnitude as that of the previously characterized chips (see turquoise-colored stars in Figure 4a), and the extracted sensitivity normalized to the membrane area (S_A) was greater by a factor of 5−6 compared to that of the chips with $PtSe_2$ from the same batch. For future device designs (and as already considered in the later-designed devices on CMOS ASIC substrates, see below), a much smaller footprint with fewer membranes per device should therefore be considered to achieve an even greater S_A.

The nonlinearity (NL) of the $PtSe_2$ pressure sensors was evaluated for all measured devices. The maximum R, corresponding to the flat membrane state of minimum strain, leads to a very nonlinear response across the whole pressure range from low to high pressure. Therefore, the NL was calculated for two ranges for each device, from low pressure to 50 mbar below the flat membrane pressure and from 50 mbar above the flat membrane pressure to high pressure, according to $NL(p) = (R_{p,measured}-R_{p,linear})/(R_{p,max}-R_{p,min})$, where $R_{p,measured}$

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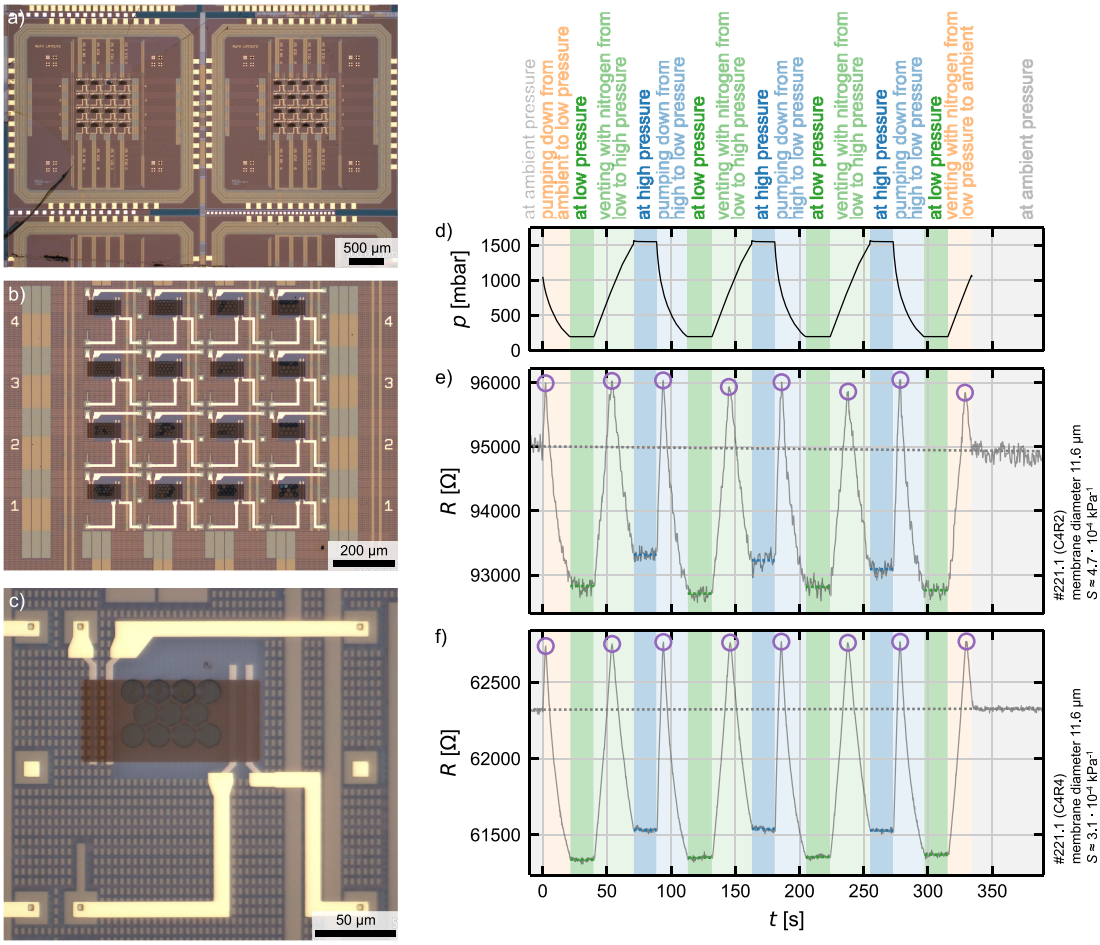

Figure 5. (a-c) Optical microscope images of $PtSe_2$/PMMA pressure sensors on CMOS ASIC substrates. (d) Reference curve of the chamber pressure during measurement. (e-f) Measurement curves of two $PtSe_2$/PMMA pressure sensors on CMOS ASIC substrates.

is the measured sensor resistance at pressure $p = (p_{max}\text{-}p_{min})/2$, between the resistances $R_{p,max}$ and $R_{p,min}$ at the upper and lower bounds of the respective range, p_{max} and p_{min}. $R_{p,linear}$ is the theoretical resistance of the sensor at pressure p assuming a linear relation of R and p between $R_{p,max}$ and $R_{p,min}$.[45,46] R-p plots of several devices are shown in Figure S16a-d, with the ranges for NL extraction indicated. The NL is dependent on the membrane diameter d (see Figure 4d), with an increase in d leading to a better (i.e., lower) NL. Almost all $PtSe_2$ pressure sensors with d = 12 μm reach a NL below 4%, while several even show a NL below 1% in both pressure ranges (see Figure 4e and, for example, chip #216.3 with a reduced active membrane area in Figure S16a).

Long-term measurements were performed on two devices on chip #220.1 (see Figure S10b), which had previously demonstrated high sensitivity and rather little drift. Starting from ambient pressure, the pressure was decreased to 200 mbar and kept constant for more than 16 min. After several minutes at 200 mbar, a drift of the device resistance toward higher values was observed, which can be attributed to slow leakage of the gas encapsulated below the membranes and, therefore, a slow reduction in the membrane deflection and strain. It was also seen in subsequent measurements that the pressure at which the device resistance was maximized was shifted to lower pressures, indicating that the flat membrane state was now reached at a lower pressure, corresponding to the pressure inside the cavities. Nevertheless, the drift is not significant on the order of seconds. In fact, a very slow drift of a pressure sensor back to its most sensitive configuration under a permanent change in ambient conditions might be favorable for certain applications.

In addition to the devices discussed to this point, pressure sensors were also fabricated on top of commercially fabricated dedicated CMOS ASIC substrates with read-out circuitry (including multiplexers for device selection) in the layers below the pressure sensors. Microscope images of two dies on a CMOS ASIC substrate, a matrix with 16 devices, and a single device are shown in Figure 5a, b, and c, respectively. The measured devices had membrane diameters of 11.6 and 13.5 μm. Measurement curves of two devices are shown in Figure 5d-f, while more data can be found in Figure S17. The average extracted S ranged between 3.1×10^{-4} kPa^{-1} and 4.7×10^{-4} kPa^{-1}, i.e., in the same range as the devices on non-CMOS substrates. The devices on the CMOS ASIC substrates were designed with smaller membrane arrays due to space restrictions, leading to a much higher S_A (see Figure 4f and Table 2).

CONCLUSIONS

The present work shows that large-scale-synthesized $PtSe_2$ possesses great potential as a piezoresistive membrane material in pressure sensors. A large data set of devices, with $PtSe_2$ from three different synthesis methods, each featuring several synthesis batches with differing parameters, was analyzed. A

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Table 2. Comparison of the Mean Sensitivity and the Mean Area-Normalized Sensitivity of Si-Based and 2D-Material-Based Pressure Sensors

device structure	mean sensitivity [10^{-4} kPa^{-1}]	suspended area [μm^2]	mean sensitivity normalized to membrane area [10^{-8} kPa^{-1} μm^{-2}]	reference
Si membrane with boron-implanted piezoresistors	0.24	$\pi\cdot(80^2\text{-}20^2)$ = 18,850	0.13	Godovitsyn et al., 2013[49]
Si membrane with boron-implanted piezoresistors	0.32	450 × 1,000 = 450,000	0.0071	Infineon MultiMEMS platform pressure sensor for tire-pressure monitoring system (TPMS)[45]
suspended graphene without PMMA, graphene grown by CVD	0.3	6 × 64 = 384	7.7	Smith et al., 2013[7]
graphene on perforated SiN_x membrane, graphene grown by CVD	2.8	490 × 490 = 240,100	0.12	Wang et al., 2016[5]
BN/graphene/BN, graphene grown by CVD	1.9	6 × 64 = 384	49.5	Li et al., 2018[11]
suspended graphene with 50 nm PMMA, graphene grown by CVD	0.29	$20 \times \pi\cdot 5^2$ = 1,571	1.83	Lin et al., 2019[12]
suspended graphene with 50 nm PMMA, graphene grown by CVD	0.74	$3 \times \pi\cdot 8^2$ = 603	12.3	Liu et al., 2020[8]
hBN/graphene/hBN, graphene grown by CVD	2.9	210 × 210 = 44,100	0.66	Wang et al., 2022[13]
suspended graphene with 100 nm Si_3N_4, graphene grown by CVD	5.3	9 × 64 = 576	92.4	Zeng et al., 2023[14]
graphene/hBN/graphene membrane (simulated only)	4.5	6 × 6 = 36	1,249	Zeng et al., 2024[50]
$PdSe_2$ on SiN_x membrane	3.9	700 × 700 = 490,000	0.08	Gong et al., 2024[29]
suspended $PtSe_2$/PMMA, $PtSe_2$ grown by TAC	13.9	157	885	Wagner et al., 2018[20,43]
suspended $PtSe_2$ without PMMA, $PtSe_2$ grown by MBE	3.8	66,162	0.57	Lukas et al., 2023[21]
suspended $PtSe_2$ with 60 nm PMMA, $PtSe_2$ grown by TAC	6.1	66,162	0.93	this work (#180.3, d_{mem} = 12 μm)
	3.7	8,822 (approx.)	4.1	this work (#216.3, d_{mem} = 12 μm, device E1−06)
	2.8	5,881 (approx.)	4.8	this work (#216.3, d_{mem} = 12 μm, device E1−12)
	4.7	1,268	36.9	this work (#221.1, d_{mem} = 11.6 μm, device C4R2, CMOS ASIC substrate)
suspended $PtSe_2$ with 60 nm PMMA, $PtSe_2$ grown by MBE	4.0	66,162	0.61	this work (#192.4, d_{mem} = 12 μm)
suspended $PtSe_2$ with 60 nm PMMA, $PtSe_2$ grown by MOCVD	5.2	60,536	0.86	this work (#266.4, d_{mem} = 7.9 μm)

fabrication process to reliably fabricate suspended $PtSe_2$/PMMA membranes across sealed cavities with a high yield was established. The measured pressure sensors reproducibly showed sensitivities of up to higher than 6×10^{-4} kPa^{-1} and low nonlinearities of down to <1% in several devices. The sensitivity has been shown to clearly depend on the membrane diameter and the piezoresistive gauge factor of the $PtSe_2$ film. We have demonstrated that a reduction in the device size through a decrease in the number of membranes within a device is possible, leading to a significant increase in the area-normalized sensitivity. This will allow the manufacturing of pressure sensors with high sensitivity but a much smaller device footprint than the current state-of-the-art MEMS technology. We have further demonstrated the feasibility of integrating $PtSe_2$ pressure sensors with CMOS technology, improving the technology readiness of $PtSe_2$-based MEMS and NEMS technology.

METHODS

Substrate Fabrication. Before the $PtSe_2$ transfer, target substrates based on 150 mm p-doped Si wafers were prepared. For the marker layer, stepper lithography was done, and the markers were etched by reactive ion etching (RIE) with C_4F_8 and SF_6. After a second step of stepper lithography for the cavity layer, 2.0−2.5 μm deep cavities were etched into the Si using RIE, again with C_4F_8 and SF_6 chemistry. After a subsequent cleaning step in a mix of H_2O_2 and H_2SO_4 the wafers were thermally oxidized to grow 90 nm of SiO_2 on top of the Si for passivation. Oxide growth after etching allows passivating cavity sidewalls and floors, erasing the possibility of short circuits from collapsed $PtSe_2$ membranes later on.

Stepper lithography with a resist double layer of lift-off resist (LOR) 3A and the photoactive AZ5214E resist was executed to deposit and pattern bottom contacts consisting of evaporated titanium (Ti, 5 nm) and palladium (Pd, 10 nm). Even though the wafer surface was uneven due to the etched cavities, the metal lift-off was successful thanks to the resist stack. A final stepper lithography and lift-off step was done to evaporate and pattern 300 nm thick aluminum (Al) pads on top of the previously patterned metal contacts in the probing pad areas for later wire bonding. Lastly, the wafers were diced to 2 cm square chips.

Due to adhesion issues with the Al pads on the Pd surface in the final step of resist stripping with TMAH-containing developer after transfer and patterning (see below), several chips were alternatively fabricated with gold (Au) bond pads. In this case, the above-mentioned Ti/Pd deposition and the subsequent gold (Au) bond pad deposition, instead of the Al deposition, were performed by contact lithography on several 2 cm pieces diced from the wafers after thermal oxide growth. The metal stack used for each respective chip is indicated in Table 1. Note that in all chips, the metal contacting the $PtSe_2$ was Pd.

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ACS Nano 2025, 19, 7026−7037

For one chip (#216.3), lithography for Ti/Pd metallization was performed with the help of a maskless aligner (Microtech LW405C), extending the metal contacts to cover significant parts of the cavity array and therefore decreasing the active membrane area. Au bond pads were subsequently deposited by contact lithography.

CMOS ASIC Substrate Fabrication. The CMOS wafers used for integration of the $PtSe_2$ pressure sensors were manufactured using a standard commercial technology provided by X-FAB Silicon Foundries SE. The 200 mm CMOS wafers utilize a 0.18 μm analog CMOS process node with up to six metallization layers. The CMOS technology includes a wide range of active devices and high-performance analog devices.

Wafer-scale postprocessing was started by etching the vias to the topmost CMOS metal layer by inductively coupled plasma etching (ICP-RIE). Titanium tungsten (TiW)/Au (10 nm/100 nm) via metallization was deposited by sputtering and patterned using a wet etching process. In the next step, Ti/Au (2 nm/30 nm) was deposited by lift-off for the bottom contact metals. The wafers were then diced into single CMOS microsystem chips. All postprocess patterning steps were done by standard UV-lithography.

$PtSe_2$ Growth. $PtSe_2$ from various synthesis methods was used.

Thermally Assisted Conversion (TAC). Thin Pt films were initially sputtered onto Si/SiO_2 substrates using a Cressington magnetron sputter coater. These films were then converted by TAC to $PtSe_2$ in a custom-built cold wall TAC and CVD system. As a precursor, selenium (Se) powder (>99.5% purity, VWR) was heated to 228 °C and transported to the samples by a carrier gas flow, consisting of varying parts of N_2 and H_2 in the range of 50−500 sccm. The conversion was carried out for 120 min at a substrate temperature of 450 °C and at a low pressure of <10 mbar. Samples #184 and #190 were converted at a higher temperature of 550 °C. After conversion, the $PtSe_2$ films tended to be approximately 2.5−3 times thicker than the initial Pt layer.

Molecular Beam Epitaxy (MBE). MBE-$PtSe_2$ samples were synthesized in a 2-in. MBE reactor supplied by Dr. Eberl MBE-Komponenten GmbH (Germany). The sapphire (0001) (c-plane) substrates were purchased from Kyocera Corporation (Japan). The sapphire was first chemically cleaned with acetone/propanol and then a 100 nm-thick molybdenum film was deposited on the back to improve radiative heating. It was outgassed under ultrahigh vacuum (10^{-10} mbar) at 500 °C overnight and then annealed at 900 °C for 15 min. A Se flux was supplied by a valved Se cracker source filled with ultrahigh purity (7N) Se, which was heated to 290 °C, and the cracker temperature was fixed at 600 °C. A Pt flux originated from high purity (4N) Pt heated in an electron beam evaporator. During synthesis, the sapphire (0001) substrate was heated to the desired growth temperature (463 and 520 °C for samples #192 and #195, respectively) and simultaneously exposed to Pt flux (0.003 Å/s) and Se flux (0.2 Å/s and 0.5 Å/s for samples #192 and #195, respectively). Sample #195 was annealed after growth at 690 °C for 30 min under the same Se flux as used during growth. After synthesis, the substrate was cooled down to 200 °C within 20 min, continuously under Se flux.

Metal−Organic Chemical Vapor Deposition (MOCVD). MOCVD growth of $PtSe_2$ was carried out within a custom-built cold-wall reactor.[34,47] Cleaned 20 mm × 20 mm Si chips with a 90 nm SiO_2 layer were placed on the substrate plate and heated up to 600 °C under low pressure conditions. Se powder (>99.5% purity, VWR) was evaporated at 225 °C and carried toward the reaction chamber by a H_2 flow. (Trimethyl)methylcyclopentadienylplatinum(IV) ($(CH_3)_3(CH_3C_5H_4)Pt$) (Strem Chemicals, 99% purity) was heated to 40 °C and used as metal−organic Pt precursor. The layer thickness was controlled by the process time, which is around 10−15 min for $PtSe_2$ thicknesses of approximately 3−5 nm.

$PtSe_2$ Transfer. The various $PtSe_2$ films were transferred to the target substrates using a frame-based temperature-assisted dry transfer method, as previously demonstrated for graphene.[39] A very thin layer of approximately 60 nm PMMA A2 950k was spin-coated onto the $PtSe_2$ films on their growth substrates. After baking at 180 °C, frames of transparent plastic foil and heat-resistant polyimide tape were prepared and attached to the edges of the PMMA surface on the growth substrates. Here, polyimide tape with acrylic adhesive (instead of standard silicone adhesive) was used to enhance the chemical stability of the transfer frame in potassium hydroxide (KOH) solution. In the next step, each transfer frame with the attached PMMA/$PtSe_2$/growth substrate was placed inside a beaker filled with cured polydimethylsiloxane (PDMS), to which the back side of the growth substrate firmly adhered. A pipet was used to push a few milliliters of a 4 mol/L KOH solution below the transfer frame to the edge of the growth substrate. Intercalation of the KOH solution between the $PtSe_2$ and the growth substrate eventually entirely detached the transfer frame with $PtSe_2$/PMMA from the growth substrate (see Figure 1c). After careful removal from the KOH solution, the frame was rinsed in DI water thoroughly and finally placed in air to dry.

The $PtSe_2$/PMMA was then placed on top of a target substrate with its transfer frame on a hot plate at 95 °C, and the adhesive was attached to prevent any sidewards motion of the transferred frame. The temperature of the hot plate was then increased to approximately 160 °C to soften the PMMA above its glass transition temperature and therefore allow the $PtSe_2$ to smoothly adhere to the target substrate. After successful complete adhesion, the $PtSe_2$/PMMA was carefully cut along the inner edge of the transfer frame with a sharp scalpel, and the frame was subsequently removed. The hot plate temperature was increased to 180 °C, and the samples were baked for 10 min.

$PtSe_2$ Patterning. $PtSe_2$/PMMA was patterned into the device channel shapes on all samples at a 2 cm chip level using contact lithography. The PMMA was not removed to mechanically support the $PtSe_2$ membranes during the fabrication process and the later device operation. LOR 3A was used between PMMA and the photoactive AZ5214E resist to prevent the mixing of the AZ5214E resist and PMMA and therefore the formation of an insoluble layer at their interface. The bottom-to-top layer stack during the lithography step was therefore $PtSe_2$, PMMA, LOR 3A, and AZ5214E. After exposure, AZ Developer was used for development. AZ Developer does not contain TMAH and therefore does not lead to any delamination or corrosion of the Al pads. AZ Developer also does not dissolve LOR 3A. LOR 3A, PMMA and $PtSe_2$ were then etched by a low-power CF_4/O_2 plasma during RIE. After etching, a low-power O_2 plasma treatment was used to remove any cross-linked polymer from the top of the photoresist layer that could otherwise remain after removal in solvents. Finally, on the chips with Al bond pads, the AZ5214E photoresist and LOR were removed by using DMSO at room temperature. Alternatively, in the case of substrates with Au bond pads and in the case of CMOS ASIC substrates, flood exposure and a 30 s dipping in a TMAH-containing developer were used to remove the LOR 3A and AZ5241E photoresist after etching and O_2 plasma treatment. This avoided the use of DMSO, which in some cases had led to the thinning or partial removal of the PMMA layer and therefore to the collapse of membranes. Optical microscope images of the final devices before wire bonding are shown in Figure 1d-e and Figure S2, as well as in Figure 5 (devices on CMOS ASIC substrates). The channel area on each fabricated device of the in-house-fabricated substrates, comprising the total membrane array area plus the surrounding passive $PtSe_2$ area, was 320 μm × 320 μm and included between 585 and 12,257 individual membranes, depending on the membrane diameter (see Table S1).

Piezoresistive Characterization. To determine the piezoresistive gauge factor (GF) of the various $PtSe_2$ films, small pieces of the same $PtSe_2$ films used for sensor fabrication were transferred onto prepared flexible polyimide (Kapton) substrates, bridging a few-mm gap between the nickel (Ni) contact pads. The samples were glued to a steel beam, and wires were soldered to the Ni contacts. The steel beam was then bent in a controlled way by applying a weight so that a tensile or compressive strain of ε = 0.0044% was applied to the sample. The setup is described in more detail in refs.[18,20] A Keithley 4200-SCS parameter analyzer was used for sampling the strain gauge resistance R while repeatedly applying and removing the attached mass over several minutes. The piezoresistive gauge factor GF was

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ACS Nano 2025, 19, 7026−7037

then extracted using GF = $\Delta R/(R_0 \cdot \varepsilon)$,[48] where ΔR is the change in device resistance from the initial value R_0.

Raman Spectroscopy. A WITec alpha300 R Raman microscope with a 532 nm laser and a 1800 g/mm grating was employed for Raman cross-sectional depth scanning[42] of the membrane devices. The focal point of the laser beam had an approximate diameter of 300 nm and a depth of ≤1 μm in the direction of the beam. We therefore chose $^1/_3$ μm as lateral pixel size and set the pixel spacing in the z-direction was to 1 μm. A power of only 0.1 mW was used since a power of just 0.3 mW was found to be already sufficient to burn through and destroy the suspended $PtSe_2$/PMMA.

Atomic Force Microscopy (AFM). AFM scanning of the membrane devices was performed using a Bruker Dimension Icon atomic force microscope in tapping mode. In particular, 15 μm × 15 μm scans of the suspended PMMA/$PtSe_2$ membranes were recorded using a scan rate of 0.25 Hz.

Electrical Characterization. A Cascade Summit 12000 A semiautomatic probe station connected to a Hewlett-Packard 4156B Precision Semiconductor Parameter Analyzer and a Hewlett-Packard E5250A Low Leakage Switch Mainframe was used for electrical measurements of the back-gated test structures. Measurements were done by the Keysight WaferPro Express test routine software. The field-effect mobility was calculated according to $\mu_F = (\partial(I_D/V_{diff})/\partial V_{BG}) \cdot L_{inner} \cdot d_{ox}/(W \cdot \varepsilon_{r,ox} \cdot \varepsilon_0)$ from the four-probe field-effect measurements on the six-port devices, where I_D is the current along the $PtSe_2$ channel, V_{diff} is the voltage between the two inner contacts, V_{BG} is the back-gate voltage, $L_{inner} \approx 25$ μm is the distance between the two inner contacts, $d_{ox} = 90$ nm is the thickness of the gate oxide, $W \approx 10$ μm is the $PtSe_2$ channel width, and $\varepsilon_{r,ox} = 3.9$ and ε_0 are the relative permittivity of the gate oxide and the vacuum permittivity, respectively. The values for W and L_{inner} were estimated from the dimensions on the photomask. We also extracted the sheet resistance from the same measurements according to $R_{sheet} = V_{diff} \cdot W/(I_D \cdot L_{inner})$.

The 20 mm chips were manually diced into approximately 6 mm square pieces and then wire-bonded into 44-pin ceramic chip carriers (LCC44) using 25 μm diameter Au wire with a tpt HB16 wire bonder by ball bonding (see Figure 3a). The chip carriers were then inserted into a pressure chamber setup built in house and previously used by Wagner et al.[20] and Lukas et al.,[39] enabling automation of the valves for pressure control and facilitating synchronized data acquisition of the included reference sensors and the device under test (DUT) (see Figure 3b). The chamber pressure was repeatedly modulated between approximately 200 mbar and 1,500 mbar using a vacuum pump and nitrogen (N_2) gas. A Keithley 4200-SCS parameter analyzer was used for the electrical measurement of the $PtSe_2$-membrane-based pressure sensors by sampling for several minutes. The sensitivity S was extracted as in $S = \Delta R/(R_0 \cdot \Delta p)$, with device resistance R_0 at ambient pressure p_0, and the difference in resistance $\Delta R = R - R_0$ at the applied pressure difference $\Delta p = p - p_0$.

A technology demonstrator (see Figure 3c) was built to showcase the $PtSe_2$ pressure sensor functionality without the need for a pressure chamber or parameter analyzer. The demonstrator houses the pressure sensor chip inside a plastic enclosure glued to a printed circuit board (PCB). The PCB features an Arduino and a display, as well as small switches to select the device to be read. A rubber tube is connected to the plastic enclosure and to a manual 250 mL syringe, allowing to reduce the gas pressure by pulling the syringe. The sensor resistance is digitally filtered and then displayed. A change in the resistance under a change in pressure can be observed, qualitatively demonstrating the functionality of the sensor. The demonstrator is powered through a USB connection (5 V). Using the Arduino Integrated Development Environment (IDE) on a computer, multiple sensor responses over time can also be displayed in a graph.

The CMOS ASIC substrates were connected to an additional dedicated PCB to address the devices through the CMOS circuitry. The column and row of the device to be read were set through a Python script controlling the PCB. The Keithley 4200-SCS parameter analyzer was then connected to the PCB for the measurement.

ASSOCIATED CONTENT

Data Availability Statement

All data is available upon reasonable request to the authors.

Supporting Information

The Supporting Information is available free of charge at https://pubs.acs.org/doi/10.1021/acsnano.4c15098.

Evaluation of the yield of devices, optical microscopy images of devices, AFM height maps and profiles, Raman depth scans, four-probe back-gated transfer measurements, measurement curves of the $PtSe_2$ resistance and two $PtSe_2$/PMMA pressure sensors, sensitivity plotted against $t^{-2/3}$, device resistance versus pressure curves, and different device dimensions (PDF)

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Notes

The authors declare no competing financial interest.

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