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Molecular Beam Deposition (MBD) and Characterisation of High-k Material as Alternative Gate Oxides for MOS-Technology

Dissertation
von

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Abstract

Until now the forecast of the Semiconductors Industry Association (SIA) concerning the dimension shrinking and the performance improvement of the electrical devices, reported in the International Technology Roadmap for Semiconductors (ITRS), matched very precisely the development of semiconductor process technology. But today the traditional scaling is indeed approaching the fundamentals limits of the materials constituting the building blocks of the CMOS process. A big and unresolved challenges in the traditional process shrinking approach is the gate insulator. To be able to follow the dimension shrinking according to the ITRS, the SiO_2 film thickness should become below 1nm within the next three years. This thickness corresponds to few atomic layers, which means that the direct tunnel leakage current through the insulator will increase. The high leakage current and the inadequate reliability for a SiO_2 layer of less than 1.5nm thickness require a replacement for SiO_2. To obtain high gate capacitance and inhibit tunneling, relative thick insulator of high dielectric constant (high-k) are needed to replace silicon dioxide (SiO_2) as gate oxide. Therefore new materials have to be introduced into the basic CMOS structure to replace the existing ones to further extend device scaling and the reduction of the production costs.

The present research thesis focuses on the proposition and investigation of three alternative gate oxide systems: aluminium-, praseodymium and lanthanum oxide (Al_2O_3, Pr_2O_3 and La_2O_3, respectively). For each one of these system, the growth process by Molecular Beam Deposition (MBD) has been optimised and electrical and physical characterisation has been performed to gain a better understanding of important factors associated with alternative gate dielectrics from both a theoretical and experimental points of view. Moreover, the optimisation of the interface between gate dielectric and the silicon substrate is taken into account during the development of the deposition processes.

The first part of the thesis concerns the aluminium oxide. Aluminium oxide (Al_2O_3) is one of the first systems which have been studied to replace silicon dioxide as gate dielectric because of its large barrier height, dielectric constant twice that of SiO_2, high stability and robustness. The basic properties of Al_2O_3 films grown on silicon substrate are well understood and for this reason alumina can be used as reference to investigate on new materials for alternative gate oxide .

Beyond the aluminium oxide, lanthanide oxides have been considered as long term solution to the high-k question. In particular praseodymium oxide (Pr_2O_3) and lanthanum oxide (La_2O_3) have attracted the attention because of their high dielectric constant (20-30) and thermal stability on silicon substrate until 1000K.

The properties of thin lanthanide oxide films as dielectric system for microelectronic application are not yet completely known and intensive research is running to find out if this dielectric will cover all the requirement needed for the new gate oxide material. In particular the major drawback of lanthanide oxide is given by its high sensibility to humidity, which leads to degradation of the dielectric film.

This thesis will try to give an answer to the open questions on the investigated materials and will show the direction for future investigations.

Contents

Chapter 1

Introduction

1.1. Dimension Shrinking in CMOS Technology

The semiconductors industry is continuously prospering since the early 1970s and it is without any doubt the main driving force for the new information age. The main reason for this sustained growth is the decrease in device feature size which enables improved functionality at a reduced cost.

In the last thirty years the dimension shrinking and the performance improvement of the electrical devices have been predicted very well by the Semiconductors Industry Association (SIA) in the International Technology Roadmap for Semiconductors (ITRS), where a 15-year outlook on the major trends of the semiconductor industry is given [ITSR].

In 1975 Gordon Moore, the founder of Intel Inc., build the fundament of the ITRS-roadmap. In his "law" G. Moore predicted that the number of transistor on a chip would quadruple every 36 months [Moore75]. As such, the semiconductor industry could gain 30% more every year. He updates his prediction in 1985 reducing the cycle of quadrupling to 24 months. It is very fascinating to see how the device-scaling has strictly followed this law for the last thirty years. The future technology generation predicted by the ITRS in its 2004 version are shown in Table 1-1.

According to the ITRS the expected physical gate length will be 53nm in 2005. This is a very important parameter as the shrinking of the transistor gate length (L) reduces the carriers travelling time between source and drain, hereby improving the device speed.

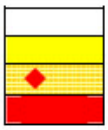
The physical sizes of the devices are miniaturised with the same factor S according the scaling method. For this reason the shortening of the transistor channel length leads to the corresponding scaling of gate area and gate oxide thickness in order to maintain the same transistor parameters such as threshold voltage and capacitance [Sze81, Section 8.5].
After thirty years now the traditional scaling is indeed approaching the fundamentals limits of the materials constituting the building blocks of the CMOS process [ITRS, Buch99, Wong02].

One of the bigger hurdles in the traditional process shrinking approach is the gate insulator. To be able to follow the dimension shrinking according to the ITRS, the SiO_2 film thickness should become below 1nm within the next three years. This thickness corresponds to few atomic layers, which means that the direct tunnel leakage current through the insulator will increase. The high leakage current and the inadequate reliability for a SiO_2 layer of less than 1.5nm thickness require a replacement for SiO_2.Therefore new materials have to be introduced into the basic CMOS structure to replace the existing ones to further extend device scaling and the reduction of the production costs.

Table 1-1 Low Standby Power Technology Requirements [ITRS, table 48c]

Year of Production	*2003*	*2004*	*2005*	*2006*	*2007*	*2008*	*2009*
Technology Node		*hp90*			*hp65*		
DRAM ½ Pitch (nm)	*100*	*90*	*80*	*70*	*65*	*57*	*50*
MPU/ASIC Metal 1 (M1) ½ Pitch (nm)	*120*	*107*	*95*	*85*	*76*	*67*	*60*
MPU/ASIC ½ Pitch (nm)	*107*	*90*	*80*	*70*	*65*	*57*	*50*
MPU Printed Gate Length (nm)	*65*	*53*	*45*	*40*	*35*	*32*	*28*
MPU Physical Gate Length (nm)	*45*	*37*	*32*	*28*	*25*	*22*	*20*
Physical gate length low standby power (LSTP) (nm) [1]	75	65	53	45	37	32	28
EOT: equivalent oxide thickness (physical) for LSTP (nm) [2]	2.2	2.1	2.1	1.9	1.6	1.5	1.4
Electrical thickness adjustment for gate depletion and inversion layer effects (nm) [3]	0.8	0.8	0.7	0.7	0.7	0.4	0.4
Equivalent electrical oxide thickness in inversion (nm) [4]	3	2.9	2.8	2.6	2.3	1.9	1.8
Nominal gate leakage current density limit (at 25°C) (A/cm^2) [5]	4.4E-03	5.1E-03	9.4E-03	1.5E-02	2.3E-02	3.1E-02	4.8E-02
Nominal LSTP power supply voltage (V_{dd}) (V) [6]	1.2	1.2	1.2	1.2	1.1	1.1	1.1
Saturation threshold voltage (V) [7]	0.50	0.50	0.51	0.52	0.50	0.47	0.47
Nominal LSTP NMOS sub-threshold leakage current, $I_{sd,leak}$ (at 25°C) (μA/μm) [8]	1.0E-05	1.0E-05	1.5E-05	2.0E-05	2.5E-05	3.0E-05	4.0E-05
Nominal LSTP NMOS saturation drive current, $I_{d,sat}$ (at V_{dd}, at 25°C) (μA/μm) [9]	410	440	470	510	510	670	700
Required "mobility/transconductance improvement" factor [10]	1.0	1.0	1.0	1.0	1.0	1.3	1.3
Sub-threshold slope adjustment factor (full depletion/multiple-gate effects) (0–1) [11]	1.0	1.0	1.0	1.0	1.0	1.0	1.0

Manufacturable solutions exist, and are being optimized
Manufacturable solutions are known
Interim solutions are known
Manufacturable solutions are NOT known



1.2. Alternative gate dielectrics

The traditional scaling, which has been the driving force of the semiconductor industry for the last 30 years, is reaching the fundamental limits of the standard materials for planar CMOS devices. New materials have to be introduced into the basic CMOS structure.

The most critical point for the shrinking to the 100nm-feature-size is the introduction of an high dielectric constant (high-k) material as alternative gate oxide. Among all materials for MOS devices, the gate oxide remains one of the most critical since it plays a fundamental role in "field effect" control. Thermally grown oxide (SiO_2) has been used as gate dielectric since the introduction of the MOSFET devices. The natural choice of silicon dioxide is due to its very good compatibility with silicon substrate, grow-process simplicity on it and nearly perfect insulator properties. However, the phase-out of SiO_2 is needed as early as the 100nm node due to the high leakage currents and inadequate reliability for SiO_2 dielectric layer of less than 1.5nm thickness [ITRS].

Extensive research is under way to replace the traditional silicon dioxide /dual –doped polysilicon gate stack process with high-k gate dielectric and new gate electrode materials.

In general the capacitance (C) of a MOS capacitor is given as:

$$C = \varepsilon_0 \varepsilon_r \frac{A}{t_{ox}} = \varepsilon_0 \varepsilon_{SiO_2} \frac{A}{t_{SiO_2}}$$

where ε_r is the relative permittivity of the gate oxide (dielectric constant), ε_0 is the permittivity of vacuum, A the capacitor area, and t_{ox} the gate oxide physical thickness. By assuming the same capacitance is achieved using SiO_2 as dielectric, the Equivalent Oxide Thickness (EOT) is given by:

$$EOT = t_{ox} \frac{\varepsilon_{SiO_2}}{\varepsilon}$$

which means that with an high dielectric constant (ε) a thick gate dielectric layer gives an appropriate capacitance value equal to that of an equivalent thin silicon dioxide.

The relative permittivity of a material is typically given by ε_r and the relation between k and ε depends on the choice of units. Anyway, it is always the case that k is proportional to ε and for this reason in this thesis the definition k = ε is used.

The advantage of using a thick high-k gate oxide is the elimination of direct tunneling, as illustrated in figure 1.1. Therefore high-k materials are excellent candidates for replacements of the traditional SiO_2 gate oxide.

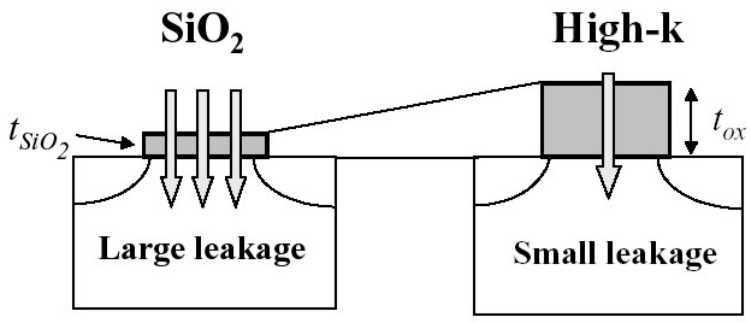


Figure 1.1 Suppression of the direct tunnel leakage current through the gate insulator by introducing alternative gate oxides having a high dielectric constant (high-k).

The evolving near-term solutions for the gate dielectric problem are materials like oxynitride, Si_3N_4 and Al_2O_3. These dielectrics have relatively low ε value compared with others high-k materials but they are very well studied and can be easily integrated into the conventional CMOS process. In general materials having dielectric constant around 10 are suggested for short term and materials having ε>20 for long term solution.

The dielectric constant ε is not the only parameter to be taken into consideration when choosing an alternative gate oxide. A crucial point for the control of leakage current in MOS devices are the band-gap of the dielectric and band alignment with respect to silicon, while high barrier height favors low leakage current. Bandgaps of 4-5eV with a barrier height of more than 1eV is necessary to limit thermionic emission and Fowler-Nordheim tunneling [ITRS, Sze81]. Furthermore, negligible trap densities in dielectric layers are required to suppress Frenkle-Poole tunneling [Frenk38]. Finally thermal stability with respect to silicon is another important factor to be taken into account since high temperature annealing are typically employed in standard CMOS processes.

The most comprehensive study on the thermal stability of binary oxide with respect to silicon at 1000K has been published by Hubbard and Schlom [Hubba96]. In this work they evaluated the free energies of reactions for producing known oxide or silicate products. Metal oxide were characterized as thermodynamically stable or unstable in contact with

silicon. All binary oxides are thermodynamically unstable with silicon at 1000K except the Li_2O, most of the alkaline earth oxide (BeO, MgO, CaO, and SrO), the column IIIB oxide (Sc_2O_3, Y_2O_3 and La_2O_3), ThO_2, UO_2, ZrO_2, HfO_2 and Al_2O_3. Among these material, BeO, MgO, CaO, SrO, Y_2O_2, Pr_2O_3, Nd_2O_3, ThO_2, ZrO_2 and Al_2O_3 have been studied and appear to be free of reaction layer on silicon. There is sufficient data to conclude that BeO, MgO and ZrO_2 are stable, but insufficient data for the others. It is also possible to have ternary or higher multi-component-oxides for direct integration with silicon, i.e., combination of binary oxides that are all thermodynamically compatible with silicon, e.g. $ZrSiO_4$, $LaAlO_3$, Y_2O_3-ZrO_2, $MgAlO_4$, etc. However, for those high-k dielectrics that are unstable in direct contact with silicon, an engineered interfacial layer will be required in order to take advantage of their potential dielectric characteristics.

A summary of which elements M have an oxide (M_{ox}) that may be thermodynamically stable in contact with silicon at 1000K is shown in figure 1.2 .

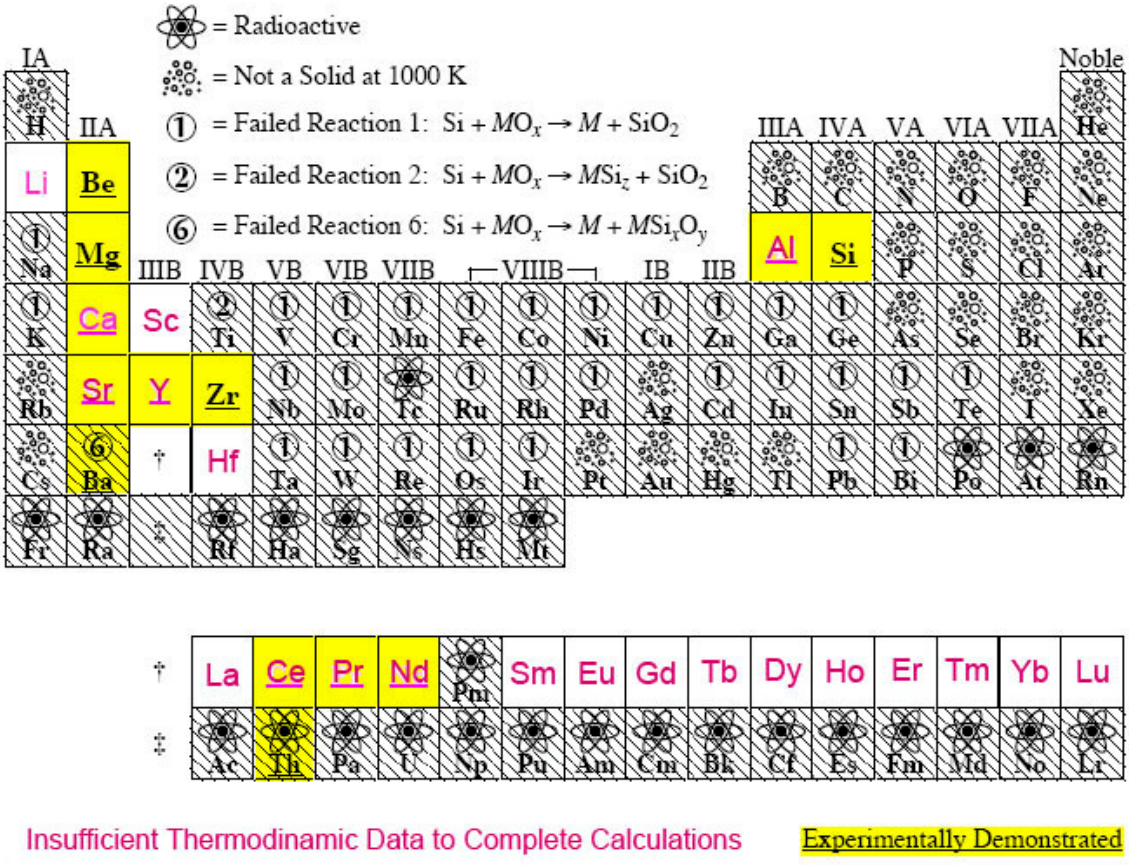


Figure 1.2 Summary of which elements M have an oxide (Mox) that may be thermodynamically stable in contact with silicon at 1000K, based on [Hubba96]. Elements M having no thermodynamically-stable or potentially thermodynamically-stable oxide (Mox) are shaded and the reason for their elimination is given. Also shown are the elements M having an oxide Mox that has been experimentally demonstrated to be stable in direct contact with silicon. Performing the thermodynamic analysis at room temperature rather than 1000K does not alter the conclusion of the thermodynamic stability analysis for oxides Mox of any of the elements [Schlom].

A list of high-k materials is reported in table 1-2 and the band-gap and band alignment for some of the systems is illustrated in figure 1.3.

Until now, none of the above materials has emerged as the most likely candidates to meet all the complex requirements associated with processing, device performances and reliability. Research focuses on the individuation of the alternative gate oxide considering different growth techniques, their optimization for the deposition of high-k materials and studying the corresponding gate stack system: high-k dielectric, interfacial layers, gate electrode and compatibility with CMOS process flow.

Table 1-2 Selected material and electrical properties of high-k dielectric

Material	**ε**	**Band Gap [eV]**	**ΔEC [eV]**	**Crystal Structure**
Binary Oxides				
SiO_2	3,9	9	3,5	Amorphous
Si_3N_4	7	5.3	2.4	Amorphous
Al_2O_3	9	8.7	2.8	Amorphous
Y_2O_3	15	6	2.3	Cubic amorphous upto 850°C anneal
La_2O_3	20-30	6	2.3	Hexagonal, cubic, amorphous
Ta_2O_5	25	4.4	< 1	Orthorhombic
TiO_2	80	3.5	1.2	Tetragonal (rutile, anatase)
HfO_2	20	6	1.5	Monoclinic, tetragonal, cubic
ZrO_2	12-25	5,8	1.4	Monoclinic, tetragonal, cubic
Er_2O_3	7			
Pr_2O_3	31	2,5-3,9		Crystalline with interfacial amorphous layer Pr-Si-O
Gd_2O_3	14			amorphous upto 850°C anneal
Silicates				
$3(HfO2)_x(SiO2)_{1-x}$	11	6	1.5	Amorphous upto 800°C
$3(ZrO2)_x(SiO2)_{1-x}$	10 - 12	6	1.5	Amorphous upto 800°C

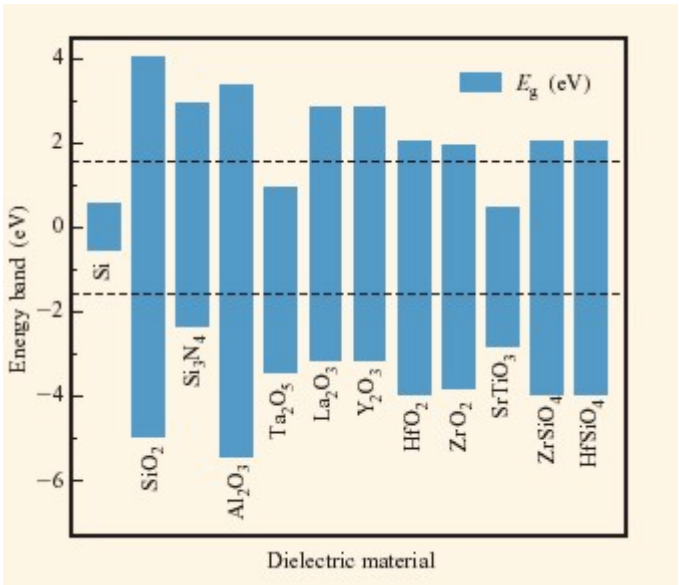


Figure 1.3 Band-gap and band alignment of high-k gate dielectrics with respect to silicon. The dashed lines represents 1eV above/below the conduction/valence band. After [Wong02, figure 2]

1.3. Scope of the present research and thesis outline

This research thesis focuses on the proposition and investigation of three alternative gate oxide systems, which are aluminium-, praseodymium and lanthanum oxide (Al_2O_3, Pr_2O_3 and La_2O_3, respectively). The choice of these system was based on the main criteria for high-k dielectrics, i.e. thermal stability, band-gap and band alignment as well as interface properties with silicon substrate.

The growth process was optimised in UHV-system by molecular beam deposition (MBD) for the three systems under consideration. The high-k gate dielectric stacks have been studied using physical and electrical characterisation techniques to gain a better understanding of important factors associated with alternative gate dielectrics from both a theoretical and experimental points of view.

Detailed electrical characterisation has been performed on metal-oxide-semiconductor (MOS) capacitors. The material characterisation is concentrated on understanding the physical and chemical properties of the gate stacks on an atomic or near-atomic scale.

In the first part of the thesis aluminium oxide is investigated in order to have a reliable reference. Aluminium oxide (Al_2O_3) is one of the first systems which have been studied to replace silicon dioxide as gate dielectric. Its large barrier height (8.7eV), large band offset with respect to silicon and a dielectric constant (ε=8-10) double than SiO_2 makes of Al_2O_3 an interesting candidate for a short term solution of the gate oxide problem. Moreover aluminium oxide is a very stable and robust material, extensively studied for many application in microelectronics and it can be easily integrated into the conventional CMOS process. The basic properties of Al_2O_3 films grown on silicon substrate are well understood. For this reason alumina is a good reference material to investigate on new alternative gate oxide.

Very promising candidates for alternative gate dielectric are the lanthanide oxides (rare earth oxides). In particular praseodymium oxide and lanthanum oxide have attracted the attention because of their dielectric constant (20-30) and thermal stability on silicon substrate until 1000K.

The first rare earth oxide investigated in this thesis is praseodymium oxide. The possibility to grow Pr_2O_3 thin films on silicon substrate by molecular beam deposition (MBD) was already reported in literature and the promising electrical results of the MBD-grown layer made of this system the ideal candidate to optimise the deposition process of lanthanide oxides in UHV.

The second investigated rare earth oxide is the lanthanum oxide. The advantage of La_2O_3 compared to the others lanthanide oxides are the higher band-gap and band-offset with respect to silicon and the stronger resistance to crystallisation.
The properties of thin lanthanum oxide films as dielectric system for microelectronic application are not yet completely known and intensive research is running to find out if this dielectric will cover all the requirement needed for the new gate oxide material. In particular the major drawback of lanthanum oxide, as all others rare earth metal oxide, is given by its high sensibility to humidity, which leads to degradation of the dielectric film.
This thesis will try to give an answer to the open questions and will profile the direction for future investigations.

The experimental techniques involved in the deposition process and characterisation of the high-k materials are presented in Chapter 2.

The optimisation of the MBD process and the characterisation of the grown films is illustrated for Al_2O_3, Pr_2O_3 and La_2O_3 respectively in chapters 3, 5 and 6 while chapter 4 is about the investigation on the interface between dielectric and silicon substrate (interface engineering) and its influence of the electrical properties of the gate stacks.

Finally, conclusion and results emerging from the studies of the alternative gate oxide considered in this thesis are summarised in chapter 7 and a direction for future investigation is proposed.

Chapter 2

Deposition and Characterisation Methodologies

The Metal-Insulator-Semiconductor (MIS) diode is the most useful device in the study of the electrical properties of the gate dielectric material and the quality of the interface between the silicon substrate and the gate oxide. In general MOS systems have been extensively investigated because they are directly related to most planar devices and integrated circuits. A comprehensive and in-depth study of the Si-SiO_2 MOS diode can be found in *MOS Physics and Technology* by Nicollian and Brews [Nico82] and in *Physics of Semiconductor Device* by Sze [Sze81]

The MIS- structure is illustrated in figure 2.1. A metal plate (gate) is separated from the semiconductor substrate by a thin insulating layer, where d is the thickness of the insulator and V is the applied voltage on the metal field plate.

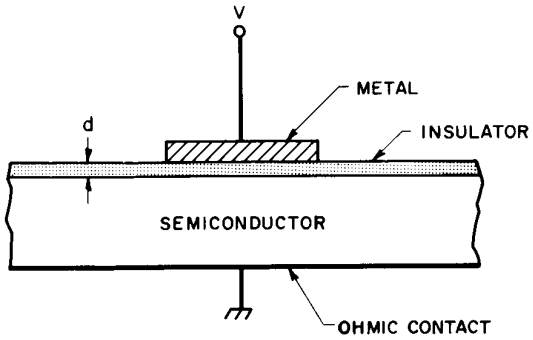


Figure 2.1 Cross section of a Metal-Insulator-Semiconductor (MIS) diode

In this study, low doped silicon wafers (p^-, <100>) have been used as substrate material to fabricate MIS structures. First of all the wafers were wet-cleaned using the recipe indicated in table 2-1. After that they were loaded in an Ultra-High-Vacuum (UHV) reactor where alternative gate oxides were grown by Molecular Beam Deposition (MBD).
The process flow for the preparation of MIS capacitors can be summarised as follow:

- Si-substrate wet cleaning
- Loading in UHV
- Gate oxide deposition by MBD
- Post-growth annealing (furnace annealing or RTP)
- Aluminium-electrode evaporation

A clear understanding of various physical phenomena occurring at silicon surface was for a long time limited by the fact that it is almost impossible to properly characterise surface and interface in the ambient atmosphere. Clean surfaces are very reactive towards gas molecules and other particles and therefore change rapidly.

A proper study of surfaces and interfaces became possible in the last decades due to the development of Ultra-High-Vacuum (UHV) techniques. In this chapter we describe a number of experimental techniques intensively used for the preparation and characterisation of gate oxide thin films. Such techniques are employed to investigate the physical properties of MBD-grown aluminium-, praseodymium- and lanthanum oxide.

Table 2-1 RCA cleaning for silicon wafers

Process Step	Solution	Process Conditions
RCA 1	5 H_2O 1 NH_3 (25%) 1 H_2O_2 (30%)	15 min 50°C
washing	DI-Water	
RCA 2	5 H_2O 1 NH_3 (25%) 1 H_2O_2 (30%)	15 min 50°C
HF-last	100 H_2O 1 HF	30 s Room Temperature Without light

2.1. Molecular Beam Deposition

Molecular Beam Epitaxy (MBE) is a technique developed in the early 1970s to grow high-purity thin epitaxial layers on crystalline substrate. The word epitaxy derives from the Greek “epi” meaning surface and “taxia” meaning arrangement and refers to the process of growing complex structures with an atom-by-atom arrangement on a substrate surface which is maintained at elevate temperature in ultrahigh vacuum.

A schematic illustration of the essential part of an MBE system is shown in fig. 2.2. The source materials are placed in evaporation cells and reactive gas can be introduced in the process chamber by gas-inlets. Moreover, the substrate is heated to the needed temperature and, if necessary, rotated to improve the film homogeneity.

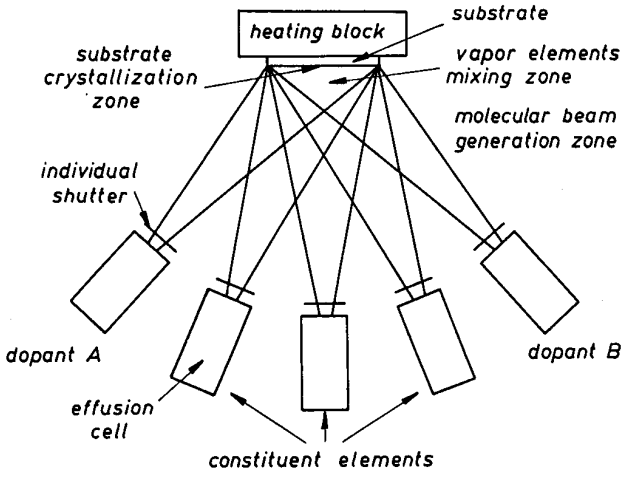


Figure 2.2 Schematic illustration of the essential part of an MBE system. After [Herm89]

The epitaxial layers are formed by reaction between the atomic beams of the constituent materials and the surface atoms of the substrate. MBE is a very flexible technique since it allows to modify the composition of the grown epitaxial layer simply changing the arrival rates of the constituent elements and dopants, which depend on the evaporation rates of the respective sources. An exhaustive description of MBE process and application can be found in [Park85, Herm89].

To describe the epitaxial growth, normally the MBE system is divided into three zones because of the different physical reactions taking place in an MBE [Herm89]. In the first zone the atomic and molecular beams are generated. In the second one beams created by different sources get in contact forming a special gas mixture. In the third zone the gas mixture reach the substrate and the epitaxial growth take place. The principal physical processes that play a role in MBE growth are listed below and illustrated in figure 2.3:

i) adsorption of the atoms and molecules impinging on the substrate;

ii) surface migration and dissociation of the adsorbed molecules;

iii) incorporation of the atoms into the crystal lattice of the substrate;

iv) thermal desorption of the species not incorporated into the crystal lattice.

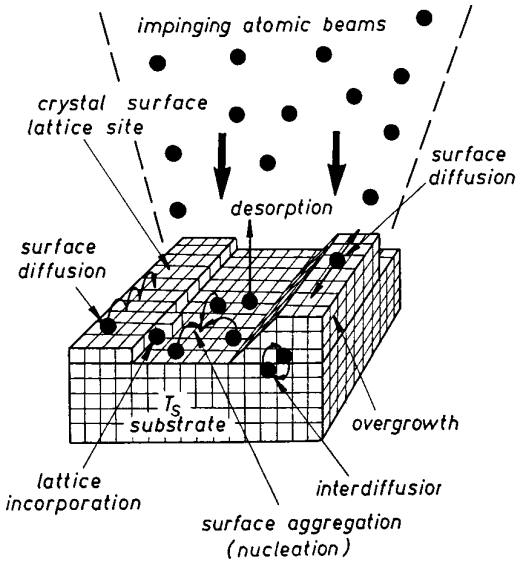


Figure 2.3 Schematic illustration of the surface processes occurring during film growth by MBE (after M.A. Herman and H. Sitter [Herm89])

Depending on the exchanged electron between the impinging atoms and the substrate ones, the adsorption process can be divided into physisorption and chemisorption. In physisorption (the name stays for physical adsorption) there is no electron exchanges between the adsorbate (gas atoms) and the adsorbent (substrate). Physisorption presents small activation energy ($0<E_A<1$ eV) and the reactive forces are van der Waals type [Neu98]. When electrons are exchanged between adsorbate and adsorbent, than the adsorption is called chemisorption and a chemical reaction characterised by high bonding energies takes place. After a certain time the atoms or molecules that have not reacted with the substrate will be let free by a thermal process called desorption that strongly depends

on the substrate temperature. The substrate temperature has also an high influence on the crystal quality of the grown layers: in general the grown layer is amorphous for low substrate temperature and polycrystalline or crystalline when the substrate is maintained at high temperature. The “low-” and “high- temperature” definition depends on the materials and on deposition parameters like the flux-rate of elements to be grown. Typically, very low constituent flux rate are necessary (Å/s) in order to assure the surface migration of the impinging species on the growing surface.

The low growth rate typical for conventional MBE techniques coupled with the necessity of very low unintentional impurity levels in the epitaxial layer lead to the conclusion that MBE growth should be carried out in an UHV environment. If the residual gas pressure in the process chamber is not low enough, the beam molecules coming from the cells may encounter the residual gas molecules during their way to the substrate. In this case the scattering processes would degrade the beam nature of the mass flow. The highest admissible value of the residual gas pressure is determined by the condition that the mean free path L of the molecules of the reactant beam penetrating the environment of the residual gas has to be larger than the distance from the beam source to the substrate surface. The mean free path is described as [Herm89]

$$L = \frac{1}{\sqrt{2}\pi n d^2}$$

where d is the molecular diameter and n the concentration of the gas molecules in the vacuum. The concentration of the gas molecules is function of pressure p and temperature T and is given by the formula [Herm89]:

$$n = \frac{p}{k_B T}$$

Another way to define the maximal residual gas pressure is to compare the time necessary to deposit a monolayer of the reactant beam and of the residual gas on the substrate: for a sufficient clean epilayer it is necessary that the relation between the deposition time of one monolayer of the reactive beam $t_1(b)$ and the deposition time of the residual gas vapor $t_1(v)$ is at least $t_1(b)=10^{-5}t_1(v)$ [Herm89].
Assuming that the residual gas in the vacuum reactor consist only of nitrogen molecules the calculated $t_1(v)$ would be $t_1(v)=10^{19}(5.74\cdot10^{22}p_i)^{-1}$. Solving the equation by saying that $t_1(v)$ has to be larger than or equal to 10^5s, it follows that the pressure of the residual gas in the vacuum reactor must be smaller or equal to $1.7\cdot10^{-9}$Pa.

Strictly speaking, the term “MBE” should be only used for epitaxial crystal growth on single crystalline substrate using a molecular beam. Therefore in this work the term “Molecular Beam Deposition” (MBD) is here used instead of MBE, since deposition of amorphous insulator materials on silicon substrate is the argument treated in this thesis work.

2.1.1 MBD of Alternative Gate Dielectrics

The development of the growth-processes of alternative gate oxide films on silicon substrates was carried out in an UHV-reactor (figure 2.4) by Molecular Beam Deposition. A detailed description of the specific system used in this thesis is argument of the PhD

thesis [Neu98]. This UHV-system has a residual gases pressure in the process chamber smaller than $1 \cdot 10^{-8}$ mbar, thus the contamination of the silicon substrate due to residual gas could be neglected.

The UHV-reactor is equipped with an effusion cell which was used for the evaporation of aluminium and an electron beam evaporation system (e-beam) for the evaporation of praseodymium- and lanthanum-oxide.

Aluminium-oxide layers were grown by exposing the silicon wafer to aluminium molecular beams in an oxidising ambient. The reactive gases (oxygen or ozone) were introduced in the chamber by a gas inlet and the working pressure was sufficiently high to allow the deposition of stoichiometric Al_2O_3-film ($1 \cdot 10^{-4}$mbar). The measured Al_2O_3-growth rate was around 0.5nm/min. A substrate temperature of 500°C was chosen in order to deposit an amorphous layer.

Praseodymium and lanthanum oxide require an electron-beam source to reach the evaporation temperature. Commercially available Pr_2O_3 (99.996%) and La_2O_3 powder (99.99%) were used as source material. When necessary oxygen reactive gas was introduced in the chamber by a gas inlet. The substrate temperature during deposition was set to the range of 500°C-700°C and the typical deposition rates were 1-3nm/min.

After deposition the wafers were transferred to a furnace or RTP-oven for post-growth annealing.

To electrically characterise the deposited films MOS capacitors were defined: aluminium electrodes were thermally evaporated on the gate oxide layer using a shadow mask and on the back-side of the wafer.

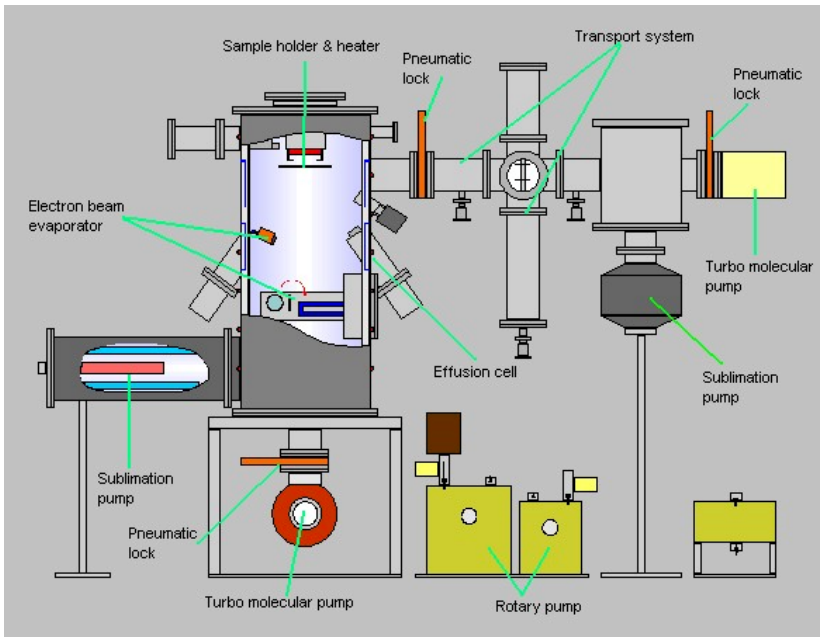


Figure 2.4 UHV-reactor used for Molecular Beam Deposition of alternative gate oxide.

2.2. Electrical Characterisation Methods

Electrical characterisation of the metal-oxide-semiconductor (MOS) capacitors is used to extract the electrical parameters from various gate dielectrics. The principal characterisation methods are capacitance vs. voltage C(V), current vs. voltage I(V) and conductance G(V) measurements. From these measurements the Equivalent Oxide Thickness (EOT), Capacitance Equivalent Oxide Thickness (CEOT), interface trap density (D_{it}) and current density at a given bias (J) are calculated. In this section, a brief review of the electrical characterisation techniques is given.

2.2.1 C(V) measurements

Capacitance vs. voltage characterisation of the MOS capacitors represents a well established and rapid method to determine important gate-dielectric parameters. The classical C-V theory has been widely reported by Nicollian and Brews [Nico82] for thick gate dielectrics. As the oxide thickness decreases the standard C-V methods has to be re-elaborated taking into account effects like substrate quantum mechanical effects and polysilicon gate-depletion. The influence of these factors in the extraction of the electrical parameters increases for very thin dielectric.

Quantum mechanics says that the density of inversion electrons reaches a peak at approximately 1 nm below the silicon surface. Hereby the gate capacitance and the inversion charge are reduced which results in an apparent increase in the equivalent oxide thickness on the order of 0.25 to 0.3 nm. Similarly depletion effects occur when the gate electrode is given by polysilicon: a finite polysilicon doping density requires a finite depleted thickness of polysilicon to accommodate the surface field. For this reason the electrically determined thickness is larger than the real physical thickness of the gate dielectric. The percentage of gate-capacitance attenuation becomes more significant as the oxide thickness is scaled down [Taur02].

A schematic overview of the various region associated with the gate stack of a MIS capacitor is reported in figure 2.5, where the interface region are highlighted.

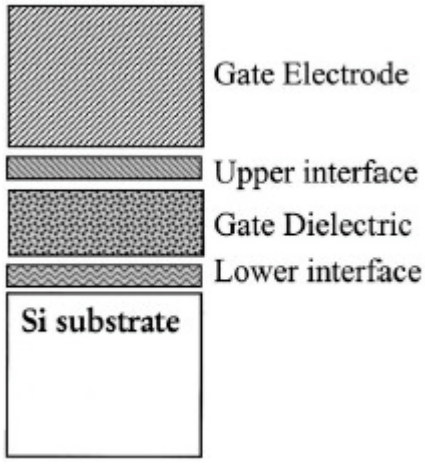


Figure 2.5 Schematic illustration of the important region of a MIS capacitors

Different modelling programs have been developed to extract the dielectric thickness from the experimental data: NCSU's CVC, UC Berkeley's QMCV and IBM's TQM are few of them. In this work, North Carolina State University's CVC has been used as standard

modelling tool because of its accurate and fast results. The physical oxide thickness and device parameters such as the substrate doping, flatband voltage and polysilicon gate doping are calculating by matching the experimental C(V) data to a physics-based theoretical model [Ahme00]. Using these parameters, the analysis program provide first-order models for polysilicon depletion and quantum mechanical effects using a least-squares error algorithm and returns the best-fit values of these parameters for a given C(V) characteristic.

2.2.1.1. C(V) and G(V) data acquisition and analysis

Important information on the properties and quality of the gate dielectric material can be extracted from C(V) and G(V) measurements on MOS devices.

C(V) characteristics allow the extraction of the equivalent oxide thickness EOT of the gate oxide. Depending on the extraction method used two oxide thickness values are indicated: one is the capacitance equivalent oxide thickness (CEOT), calculated from the capacitance measured in strong accumulation, and the other is the equivalent oxide thickness (EOT), which is the value after QM correction obtained using the NCSU CVC program [Haus96]. The presence of charge in the dielectric layer can be extracted by considering stretch-out, hysteresis or shift of the flat band voltage shift (V_{FB}) in the C(V) characteristics [Nico02, Baum03]

The study of the interface between gate oxide and silicon substrate is done by considering the equivalent parallel conductance G(V). Theory and procedure to extract the interface state density D_{it} from G(V) measurements is argument of section 2.2.2 of this chapter.

The capacitance vs. voltage measurements were performed on MOS capacitors using a shielded 4-point-prober in combination with a HP 4275A LCR Meter. The low-level signal frequency was set to 20 kHz. Capacitance and equivalent parallel conductance were measured ramping a voltage range between –3 V and +2 V. Prior to data acquisition, an open and short-circuit correction was performed.

The MOS capacitor can be approximated by three-element model consisting of a capacitance, C, a conductance, G, and a series resistance, r_S. Series resistance can cause a serious error in the extraction of interfacial properties. For this reason, the measured capacitance and conductance values for the MOS capacitors have been corrected following the methods developed by Nicollian and Brews [Nico82, Section 5.7] which are here briefly reported.

The series resistance can be measured considering the equivalent circuit of the MOS capacitor in depletion, as shown in figure 2.6a. At a given frequency, the greatest effect on the admittance is measured in strong accumulation. Figure 2.6b) shows the equivalent circuit of the MOS capacitor in strong accumulation, where the accumulation layer capacitance C_A is in parallel with $<Y_{it}>$. The equivalent circuit can be simplified because C_A is large, shutting $\langle Y_{it} \rangle$, becoming that in figure 2.6c). Because $C_A >> C_{ox}$, fig.2.6c) can be further simplified to figure 2.6d.

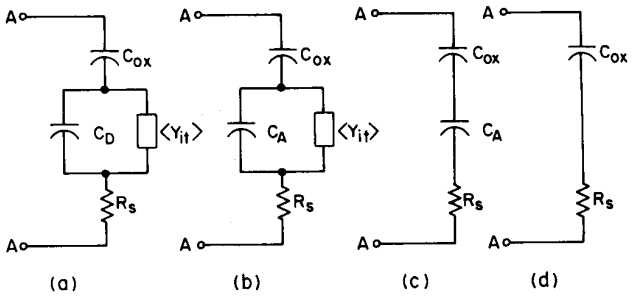


Figure 2.6 (a) Equivalent circuit of the MOS capacitor in depletion including series resistance, R_S; (b) Equivalent circuit of the MOS capacitor in strong accumulation; (c) simplified version of (b); (d) simplified version of (c) used in extracting values of C_{ox} and Rs from the admittance measured in strong accumulation [Nico82, figure 5.22].

To determine R_S, the MOS capacitor is biased into strong accumulation. The admittance Y_{ma} across the terminal A-A in figure 2.6d) in strong accumulation in terms of the capacitance C_{ma} and equivalent parallel conductance G_{ma} is:

$$Y_{ma} = G_{ma} + j\omega C_{ma} \tag{2.1}$$

Series resistance is the real part of the impedance $Z_{ma}=1/Y_{ma}$ or:

$$R_S = \frac{G_{ma}}{G_{ma}^2 + \omega^2 C_{ma}^2} \tag{2.2}$$

Capacitance C_{ox} is obtained by substituting R_S from (2.2) into the relation $C_{ma} = C_{ox} / \left(1 + \omega^2 R_S^2 C_{ox}^2\right)$ derived from the equivalent circuit in figure 2.6d) and solving for C_{ox}, which yields

$$C_{ox} = C_{\max}\left[1 + \left(\frac{G_{ma}}{\omega C_{ma}}\right)^2\right] \tag{2.3}$$

Corrected capacitance C_C and corrected equivalent parallel conductance G_C at the frequency of interest are:

$$C_C = \frac{\left(G_m^2 + \omega^2 C_m^2\right) C_m}{a^2 + \omega^2 C_m^2} \tag{2.4}$$

$$G_c = \frac{\left(G_m^2 + \omega^2 C_m^2\right) a}{a^2 + \omega^2 C_m^2} \tag{2.5}$$

where $a = G_m - \left(G_m^2 + \omega^2 C_m^2\right) \cdot R_S$ and Cm and Gm are the capacitance and the equivalent parallel conductance measured across the terminal of the MOS capacitor.

The effect of series resistance on capacitance and conductance is shown in figure 2.7 and 2.8, respectively. The absence of a peak in G(V) curve means that the device resistance produced the dominant loss, completely masking the interface trap loss.
The corrected capacitance, C_m, and the corrected conductance, G_m, obtained from (2.4) and (2.5) are show in figure 2.7 and 2.8, respectively (dotted line).

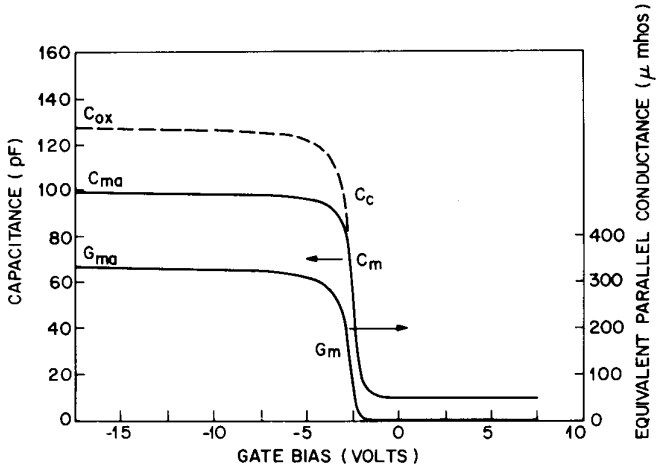


Figure 2.7 Capacitance and equivalent conductance measured at 1MHz as a function of gate bias at a sweep rate of 10mV/sec. The capacitance corrected for series resistance is shown as the dashed curve [Nico82, figure 5.23].

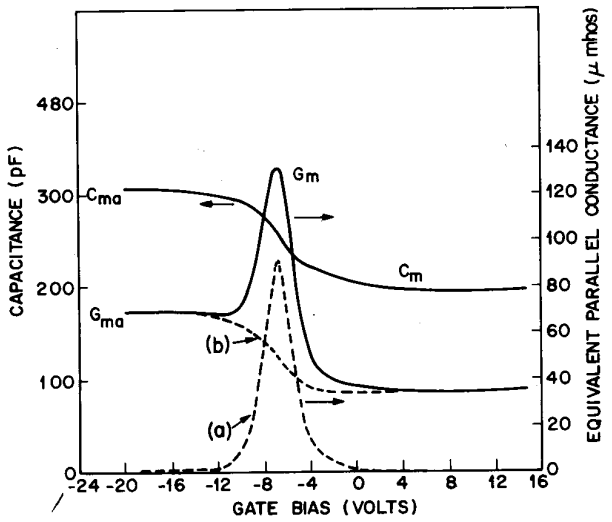


Figure 2.8 Capacitance and equivalent parallel conductance measured at 1MHz as a function of gate bias. The dashed conductance curve has been corrected for series resistance [Nico82, figure 5.24].

2.2.2 Interface State Characterisation

The interface between silicon substrate and gate dielectric represents one of the crucial parameters that directly influence MOS devices performances. Standard silicon oxide gate dielectric thermally-grown from Si-substrate shows very low interface state density (D_{it}). Moving to high-k materials, the gate dielectric is grown by deposition on the Si-substrate.

Therefore a less perfect interface with silicon will be produced, leading to an increase of interface state density (D_{it}), which strongly affects the drive current of the device.

D_{it} is one of the primary parameters used to characterise and monitor gate dielectric reliability and it also strongly correlates with the quality of the gate stack. A number of techniques have been developed for interface state measurements. In this research work, the conductance method first proposed by Nicollian and Goetzberger in 1967 and then developed by Brews [Brews83] has been used to characterise the interface properties of the MOS capacitors.

The Brew's method only need one curve (G_{it}/ω vs. v_s) to extract the interface state density D_{it}, where G_{it} is the interface trap conductance, ω the frequency in radians/sec and v_s the band bending. First of all, the capacitance and conductance measurements have to be corrected using the equation (2.4) and (2.5). After that, the interface trap conductance is calculated using the equation (2.6)

$$\frac{G_{it}}{\omega} = \frac{\omega C_{ox}^2 G_m}{G_m^2 + \omega^2 \left(C_{ox} - C_m\right)^2} \tag{2.6}$$

where C_m and G_m are the measured capacitance and conductance after correction.
The interface state density is given by:

$$D_{it} = \left(G_{it} / \varpi\right)_p / (q^2 A f_D) \tag{2.7}$$

where $\left(G_{it} / \varpi\right)_p$ is the maximum (peak) value of G_{it} / ω, q is the elementary charge, A is the capacity area and f_D is a ratio that can be calculated as follow:

- starting from the graphic G_{it} / ω vs. V_G and choosing the fraction of the width f_W, the $V_G(+)$ and $V_G(-)$ are extracted with respect to the $\left(G_{it} / \varpi\right)_p$ peak position.
- $V_G(+)$-$V_G(-)$ will be the entrance value in the band bending diagram (v_s vs. V_G). In this way, $v_s(+)$-$v_s(-)$ can be read on the y-axe.
- $v_s(+)$-$v_s(-)$ for the respective f_W allow the extraction of σ_s from figure 2.9 and f_D can be read from figure 2.10

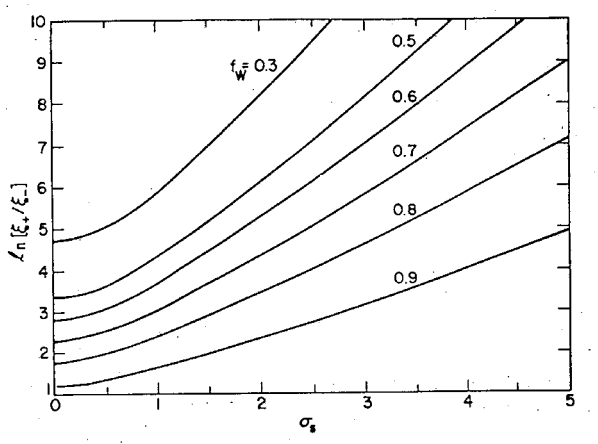


Figure 2.9 Experimental width parameter, $\ln(\xi_+/\xi_-)$ vs. interfacial broadening parameter, σ_s, for various choices of the fractional value for the width, f_W. The width $\ln(\xi_+/\xi_-)$ is $v_s(+)$-$v_s(-)$. [Brews83, figure 2].

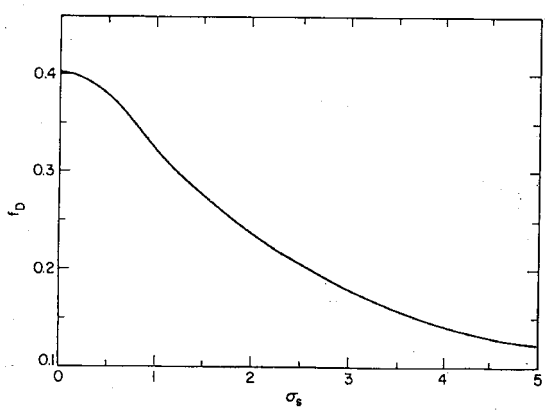


Figure 2.10 The ratio f_D vs. σ_s. [Brews83, figure 3].

2.2.3 I(V) measurements

The measurement set-up used for I(V) measurement was a Keithley Picoammeter Type 487 in combination with a shielded 4-point-prober. The current resolution of this setup is about 1 nA/cm^2. In order to filter leakage current from relaxation current the delay time between single measurement points is raised to 3-5 s for currents below 1 nA, while for currents above 1 nA the delay time is set to 250 ms.

Gate leakage current is normally used to characterise gate oxide and give important information about the conduction mechanism of the insulating layer. A list of the basic conduction processes is reported in table 2-2 ([Sze81], paragraph 7.3.4).

For an ultrathin insulator the dominating conduction mechanism is tunnelling through the gate dielectric. If the voltage applied on the gate electrode is lower than the metal barrier height, the electrons move from the metal Fermi level to the conduction band of the semiconductor through the total oxide thickness which is called Direct Tunneling. When the applied voltage (V_G) is higher than the barrier height of the metal gate, the electron will tunnel through a triangular barrier into the insulator conduction band. This conduction mechanism is called Fowler-Nordheim (FN) Tunneling. Direct tunnelling and FN tunnelling mechanism are illustrate inn fig. 2.11.

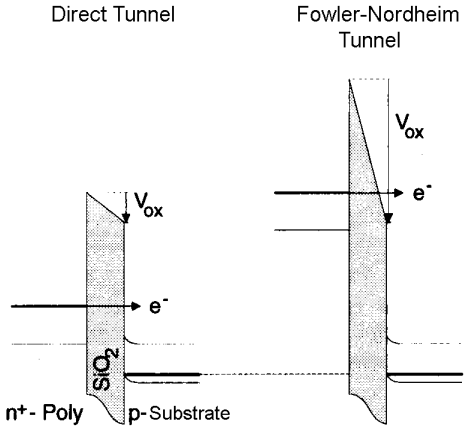


Figure 2.11 Direct Tunnel and Fowler-Nordheim Tunnel for the electrons in a NMOS-structure having an n^+ doped polysilicon gate.

Table 2-2 Conduction Mechanism in insulating films

Process	Expression	Voltage and Temperature Dependence
Schottky emission	$J = A \cdot T^2 \exp\left[\frac{-q\left(\phi_B - \sqrt{q\xi / 4\pi\varepsilon_i}\right)}{kT}\right]$	$\sim T^2 \exp(+a\sqrt{V}/T - q\phi_B / kT)$
Frenkel-Poole emission	$J \sim \xi \exp\left[\frac{-q\left(\phi_B - \sqrt{q\xi / 4\pi\varepsilon_i}\right)}{kT}\right]$	$\sim V \exp(+2a\sqrt{V}/T - q\phi_B / kT)$
Tunnel or field emission	$J \sim \xi^2 \exp\left[-\frac{4\sqrt{2m^*}(q\phi_B)^{3/2}}{3q\hbar\xi}\right]$	$\sim V \exp(-b/V)$
Space-charge emission	$J = \frac{8\varepsilon_i \pi V^2}{9d^3}$	$\sim V$
Ohmic	$J \sim \xi \exp(-\Delta E_{ae} / kT)$	$\sim V \exp(-c/T)$
Ionic conduction	$J \sim \frac{\xi}{T} \exp(-\Delta E_{ai} / kT)$	$\sim \frac{V}{T} \exp(-d'/T)$

A^*=effettive Richarson constant, ϕ_B=barrier height, ξ=electric field, ε_i=insulator permittivity, m^*=effective mass, d=insulator thickness, ΔE_{ae}=activation energy of ions, $a = \sqrt{q/(4\pi\varepsilon_i d)}$, and $V=\xi d$. b, c and d' are positive constant independent of temperature (T) and voltage (V).

2.3. Physical and Chemical Characterisation Methods

Chemical composition and physical structures of the gate stacks were studied by means of X-ray Photoelectron Spectrometry (XPS), Auger Electron Spectroscopy (AES), Rutherford Back Scattering Spectrometry (RBS) and high-resolution Transmission Electron Microscope (TEM).

2.3.1 X-ray Photoelectron Spectroscopy - XPS

X-ray photoelectron spectroscopy (XPS) is an analysis technique in surface and interface physics. It has its origins in the discovery of the photoelectric effect by Hertz [Dabr00], the energetic description given by Einstein and the publication of XP spectra for different metal by Robinson and Rawlinson. Starting from these study, Siegbahn et al. developed XPS in a sensitive, high resolution methods for the determination of the binding energy of the electrons. Today XPS is a standard technique capable to provide valuable information about the electronic structure in the film, also used to check the chemical composition and determine the stoichiometry of the sample.

In XPS measurements, the radiation is usually obtained from x-ray tubes with Mg or Al anodes (Mg $K\alpha$-1253.6 eV, Al $K\alpha$ –1486.6 eV). The XPS emission process is illustrated in figure 2.12. Photons interact with atoms in the surface region by photoelectric effect. A photoelectron ejected into the vacuum has an energy $E_K = h\nu - E_B - \phi$, where $h\nu$ is the energy of the incoming photon, E_B is the atomic binding energy, ϕ the work-function.
The measured photoelectron kinetic energy yields information about the binding energy of electrons and allows to identify different elements in the sample. Quantitative data can be obtained from peaks height or peaks areas, and identification of chemical state can be made

from the exact measurement of peak position. The mean free path of the escaping electron is usually in the range 5-20Å, which make XPS a surface sensitive technique.

In this thesis, the XPS analysis was performed in an ultrahigh vacuum Omicron XPS-system (base pressure $5 \cdot 10^{10}$ mbar) equipped with an hemispherical electron energy analyser (EA 125) and a DAR 400 twin-anode X-ray source, where the X-ray source can be chosen between Al Kα (energy 1486.6 eV) and Mg Kα (energy 1253.6 eV). Since the Mg Kα has a smaller full width at half maximum (FWHM) [OmiUG], i.e. a better analysis resolution, the Mg-anode was used for the reported measurements.

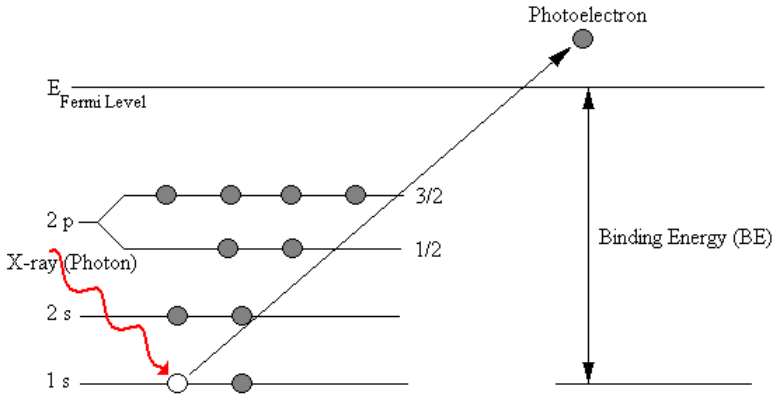


Figure 2.12 XPS emission process: photons interact with atoms in the surface region by the photoelectric effect. A photoelectron ejected into the vacuum has an energy $E_K = h\nu - E_B - \phi$, where hν is the energy of the incoming photon, E_B is the atomic binding energy, ϕ the work-function.

2.3.2 Auger Electron Spectroscopy - AES

Auger Electron Spectroscopy (*Auger spectroscopy* or AES) is, like XPS, a surface sensitive technique that use emission of low energy electrons in the *Auger process* [Briggs, Lüth]. This technique was developed in the late 1960's and derives its name from the effect observed for the first time by Pierre Auger, French physicist, in the mid-1920's [Auge25]. AES is used to study the surface chemical composition (element analysis) as well as depth profiling of the concentration of chemical elements presents in the sample.

AES is a surface sensitive technique because of the limited escape depth of the electrons. Typical probing depth in AES are in the range 10-30 Å.
The Auger process is explained in figure 2.13.

The basic Auger process starts with the removal of an inner shell atomic electron to form a vacancy. The excitation process is induced by exposing the sample to a beam of high energy electrons (typically having a primary energy in the range of 1 - 10 keV). Such electrons have sufficient energy to ionise all levels of the lighter elements and the core levels of the heavier elements. The inner shell vacancy is then filled by a second atomic electron from a higher shell. Since energy must be simultaneously released, a third electron, the Auger electron, escape carrying the excess energy in a radiation-less process. The process of an excited ion decaying into a doubly charged ion by ejection of an electron is called Auger process. Alternatively, the energy can be removed by an X-ray photon. For low atomic number elements the most probable transitions occur when a K-level electron is ejected by the primary beam, an L-level drops into the vacancy and another L-level

electron is ejected. For elements having higher atomic number LMM and MNN transition are more probable than KLL. As consequence, secondary electrons having sharply-defined energy are emitted. These can be than detected and analysed by electron analyser like for example Cylindrical Mirror Analyser (CMA).

In general the initial ionisation is a non-selective process and there will be many possible Auger transitions for a given element. Auger Spectroscopy is based upon the measurement of the kinetic energies of the emitted electrons. Each element of the analysed sample will give rise to a characteristic spectrum of peaks at various kinetic energy directly related to the differences in core-level energies: measuring these kinetic energies allows to identify the particular elements present in the sample, making exception of hydrogen and helium which have only one shell.

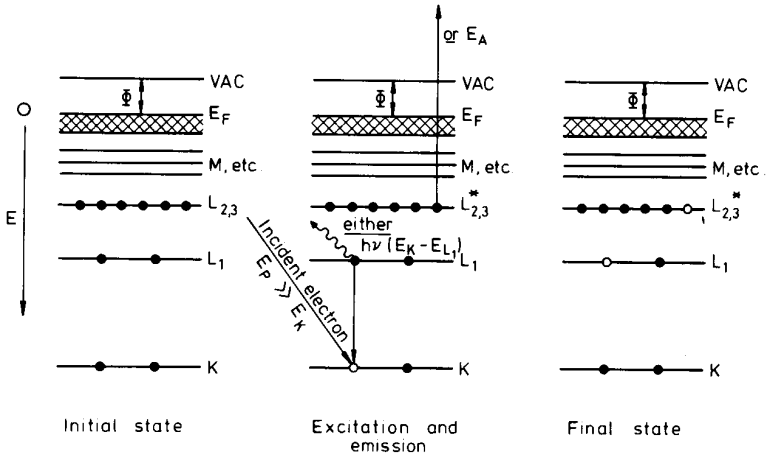


Figure 2.13 A schematic example of an Auger emission process. The system in its the ground state is reported on the left. In the centre an incident electron has created a hole in the core level K by ionisation. The hole of the K shell is filled by an electron from L_1, releasing an amount of energy which can appear as a photon or can be given up to another electron as in this case. The doubly ionised final state is shown on the right. After [Brig85]

2.3.3 Rutherford BackScattering Spectroscopy - RBS

Rutherford BackScattering Spectroscopy (RBS) is an ion beam analysis technique that allows the determination of both atomic mass and concentration of elemental target constituents as function of the depth under the surface. A short introduction in RBS analysis can be found in [Bird89]. In RBS measurements the number and the energy distribution of the energetic ions (usually He^+ ions with an energy within the range 1 - 4 MeV) back-scattered from atoms within the near-surface region of the solid targets are measured. This technique is most suited for the detection of elements which are heavier than the constituents of the substrate and for targets having atomic number $Z > 10$.
The back-scattering method is illustrated in figure 2.14.

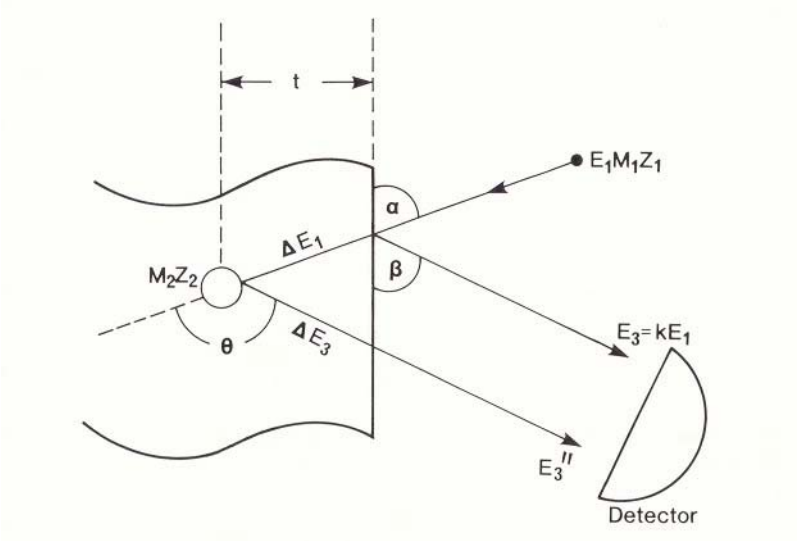


Figure 2.14 Rutherford BackScattering Spectroscopy (RBS). Schematic illustration of the parameters of RBS (after schematic Bird & Williams [Bird89], Fig. 3.1 pp 105)

A primary ion beam composed by ions having a mass M_1, atomic number Z_1 and energy E_0 are incident on a sample composed by atoms of mass M_2 and atomic number Z_2. Scattering of the ion by the samples nuclei gives information about mass, concentration and depth of the atoms that compose the analysed material. For those incident ions scattered by surface atoms, conservation of energy and momentum leads to a relationship of their energy after scattering E_3 to the incident energy E_1 through the kinematic factor K. This is a function of M_1, M_2 and θ.

$$E_3 = KE_1 \tag{2.8}$$

$$K = \left\{ \frac{(M_2^2 - M_1^2 \sin^2\theta)^{1/2} + M_1 \cos\theta}{M_2 + M_1} \right\}^2 \tag{2.9}$$

The concentration of the target constituents can be obtained from the Rutherford scattering cross-section σ, as reported in equation 2.10.

$$\frac{d\sigma}{d\Omega} = \left(\frac{Z_1 Z_2 e^2}{16\pi\varepsilon_1 E} \right)^2 \frac{4}{\sin^4\theta} \frac{\left\{ \left[1 - \left((M_1 / M_2) \sin\theta \right)^2 \right]^{1/2} + \cos\theta \right\}^2}{\left[1 - \left((M_1 / M_2) \sin\theta \right)^2 \right]^{1/2}} \tag{2.10}$$

The number of the scattered particles is measured by a detector (ΔA). This number can be then converted to the concentration of a particular element (N_M) in the target by the formula 2.11

$$\Delta A = \frac{d\sigma}{d\Omega} \Delta\Omega N_M Q \tag{2.11}$$

The incident particle lose energy in penetrating the sample in both direction: along the incident path before the scattering (energy loss ΔE_1) and after sputtering, along the exit path (energy loss ΔE_3). The total energy loss term is $\Delta E_{1,3}$ (equation 2.12)

$$\Delta E_{1,3} = K\Delta E_1 + \Delta E_3 \qquad (2.12)$$

The energy differences extracted from RBS spectra can be used to identify scattering depths and in this way to prove a depth profile of target constituents.

2.3.4 Transmission Electron Microscopy - TEM

Transmission Electron Microscopy (TEM) is a very powerful thin-film analysis technique, which is able to provide structural information at very high resolution. The conventional TEM is capable of imaging a specimen and returning the selected-area-diffraction pattern. The TEM is an electron-optical microscope that uses electromagnetic lenses to focus and direct an electron beam. Data is collected from the beam after it passes through the sample.

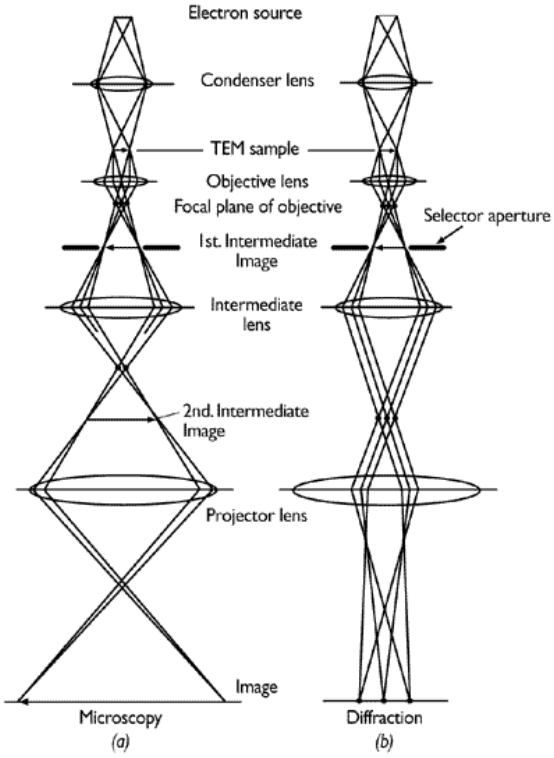


Figure 2.15 TEM optical system

The source radiation is generated using an electron gun. The resulting beam of electrons is focused into a tight, coherent beam by multiple electromagnetic lenses and apertures. The lens system is designed to control and focus the electron beam. The ray paths of the electrons are schematically represented in figure 2.15 [Philips]. The electron beam passes an electron- transparent sample and an enlarged image is formed using a set of lenses. The image is projected onto a photographic plate or recorded by a video camera. Whereas the

use of visible light limits the lateral resolution to a few tenths of a micron, the much smaller wavelength of electrons allows a resolution of about 0.2 nm. In general, resolution and magnification of a microscope are related to the wavelength and the energy of the radiation: the shorter the wavelength, the better the resolution.

Image contrast is obtained by the interaction of the electron beam with the sample: a part of the electrons will be diffracted. By means of an aperture one or more diffracted beams are selected for the formation of the image. In this way one can distinguish between different materials, as well as image individual crystals and crystal defects.

Various techniques are then used to collect data from the electrons that have passed through the sample. For example image data can be collected by means of a fluorescent screen that is hit by the electron beam. The resulting image may be recorded on a photographic film or with a CCD camera linked to a computer.

Chapter 3

Deposition process optimisation and characterisation of thin Al_2O_3 films grown by means of MBD

This chapter proposes an optimisation of the Molecular Beam Deposition (MBD) process for aluminium oxide films on silicon substrate.

Al_2O_3 samples grown with the developed process have been electrically and physically characterised. Stoichiometry and morphology of the Al_2O_3 films were studied by AES, XPS and TEM, and the electrical properties investigated by current density vs. voltage J(V) and capacitance vs. voltage C(V) characterisation.

The structure of the chapter can be illustrated as follow: in the first section (Section 3.1) the Al_2O_3 system is introduced and its physical properties are illustrated.

The second section (Section 3.2) introduces the influence of the different process parameters during MBD and their optimisation for Al_2O_3 deposition. Moreover, the thermal stability of UHV-grown aluminium oxide is shortly presented.

The results illustrated in Section 3.2 are deeply investigated in Section 3.3, in which the electrical quality of the MBD-grown aluminium oxide films has been investigated using current density vs. voltage J(V) and capacitance vs. voltage measurements C(V) of MOS capacitors.

The last section (Section 3.4) concerns with the physical characterisation of the Al_2O_3 films grown using the optimised process.

3.1. Physical properties of Al_2O_3

Aluminium oxide (Al_2O_3) has been one of the first candidates being investigated to replace silicon dioxide as gate dielectric because of its large barrier height (8.7eV), large band offset with respect to silicon and a dielectric constant (ε=8-10) double than SiO_2 [Wilk01]. It is a very stable and robust material, extensively studied for many application in microelectronics, especially in memory applications. The basics properties of Al_2O_3 films grown on silicon substrate are well understood and for this reason alumina can be used as reference to investigate on new materials for alternative gate oxide.

The necessity to investigate for other alternative candidate is principally due to the fact that Al_2O_3-system has a dielectric constant only twice the one of silicon dioxide (ε_{Al2O3}=8-10, compared to ε_{SiO2}=3.9), so the introduction of this system as gate oxide only allows a relatively short term solution for the microelectronic industry. Moreover, aluminium oxide has a low stopping power against oxygen diffusion and boron penetration [Gusev01], both factors which influence the device structure (thicker interface oxide) and performance (variation of the substrate doping in the channel region).

However, the high interest on aluminium oxide is correlated to the fact that Al_2O_3 is one of the few metal oxide that is thermodynamically stable on silicon and the Al_2O_3/Si interface imitates, to a certain extent, the SiO_2/Si interface [Alme03]. Unfortunately, the electrical quality of the SiO_2/Si interface cannot be entirely reproduced by the Al_2O_3/Si system or by any other alternative dielectric considered so far. The reason for this behaviour is the different growth process used for silicon dioxide and for others alternative dielectrics on silicon.

In case of SiO_2 gate oxide the dielectric layer is grown on silicon substrate by thermal oxidation, during which the silicon substrate is exposed to a reactive atmosphere containing oxygen. This oxidation process is typically done at high temperature (T>1000°C). In this way, the upper layers of the Si- substrate are converted into SiO_2 [Dabro, Chapter 6].

Instead of that, alternative gate oxide are produced by deposition of the dielectrics layer directly on silicon substrate. Unfortunately, the deposition process does not allow the growth of a perfect interface between the gate dielectric and the silicon substrate. This kind of process always leads to the formation of defects at the interface region which can acts as electron sources or traps, drastically reducing the reliability of the device. Nevertheless, it as been reported that post-deposition annealing at moderate temperature in neutral atmosphere can reduce the interface state density and the leakage current down to acceptable limits. This interface improvement is due to a very thin silicon oxide or silicate layer grown between the high-k and the silicon substrate, which will smooth the interface and will relax the strain caused by structural defects and structural misfits of the different compounds [Alme03].

Different deposition techniques are used to grow Al_2O_3 thin films on silicon. A complete review of deposition methods and electrical results concerning aluminium oxide is reported in ref. [Wilk01] and [Alme02].

In figure 3.1 the phase diagram for the Al-O system is reported [LB-IV/5a]. The α-Al_2O_3 is the only stable compound in the system, however several metastable modifications are known. The structure of all modifications can be seen as a close packed O^{2-} -sublattice. At octahedral and tetrahedral sites there are Al-ions or vacations. The polymorphism is due to changing the stacking of the O^{2-} -layers and distributing Al-ions and vacations. Crystal structures for the Al-O system are indicated in Table 3-1.

Aluminium oxide films deposited at substrate temperature lower than 550°C result amorphous [Guha01], while at a deposition temperature of 650°C there is the appearance of crystalline microstructure, indicating the transition to the cubic γ form of Al_2O_3. Others studies indicate similar transition depending on the heating temperature [Chou91; Fuku96]: starting from amorphous La_2O_3, the oxide will reveal the formation of γ–Al_2O_3 for temperature in the range of 650-800°C, and finally crystallise in the α-Al_2O_3 form in the range 1000-1200°C.

Table 3.1 Crystal structure for Al-O system

Phase	Structure	Type
α-Al_2O_3	hex	α-Al_2O_3
Metastable phases		
γ-Al_2O_3	cub	Al_2MgO_4
θ-Al_2O_3	mon	b-Ga_2O_3
x-Al_2O_3	hex	
χ-Al_2O_3	hex	

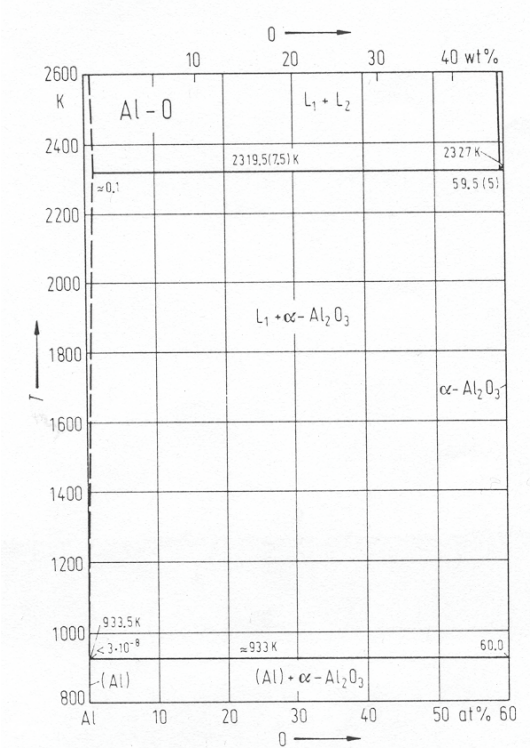


Figure 3.1 Al-O phase diagram (after Landolt-Börnstein [LB], IV/5 – Subvolume G)

3.2. Process optimisation and thermal stability of MBD-grown Al_2O_3 thin films

The deposition process and thermal stability of aluminium oxide thin films grown by means of MBD has been optimised for UHV-system. The principle of MBD deposition and a description of the UHV-system can be found in Chapter 2. Substrate temperature, oxygen partial pressure and different oxidizing source have been taken in consideration during the process optimisation. After deposition, the Al_2O_3 films have been annealed. The thermal stability of the gate oxide and the influence of the annealing ambient (nitrogen and oxygen) on the properties of the aluminium oxide have been considered.

3.2.1 Influence of substrate temperature

One of the principal parameters that influences the physical characteristics of the deposited layer in a molecular beam deposition process is the temperature of silicon substrate. Depending on the substrate temperature, the deposited layer can be amorphous, polycrystalline or crystalline. The poly-crystalline films are highly undesirable because grain boundaries represent alternative, fast transport paths for electrons in the gate dielectric layer, which result in an important increase of the leakage current. As an ideal mono-crystalline layer is very difficult to be obtained, gate oxide having amorphous structure are wished to reduce leakage current.

In this work, experiments have been done to find out the ideal substrate temperature for Al_2O_3 deposition in UHV-system and a substrate temperature smaller than 550°C has been used during deposition process in order to grow an amorphous layer. Different samples have been grown under the same process conditions (pre-deposition preparation, ambient, gas pressure, deposition rate) and only changing the substrate temperature in the range

25°C – 530°C. The process conditions, thicknesses and substrate temperatures are indicated in table 3-2. Current density vs. voltage measurements of MBD-grown Al_2O_3 films show that the higher the substrate temperature, the lower the leakage current for samples having a comparable thickness (Subsection 3.3.1.1, figure 3.2).

Table 3-2 Influence of substrate temperature during Al_2O_3 deposition process. The process parameters are summarized.

Wafer no.	**Thermal Desorption**	**$T_{substrate}$** [°C]	**Ambient / Pressure** [mbar]	**$t_{Physical}$** [nm]	**$J_{Leakage}$ @ -1V** [A/cm^2]
1341	Y	RT	Oxygen /1*10^{-4}	12	0.06
24012/1	Y	400	Oxygen /1*10^{-4}	7	3·10^{-5}
08012/2	Y	450	Oxygen / 1*10^{-4}	7	3·10^{-6}
16042/4	Y	500	Oxygen /1*10^{-4}	6	1·10^{-8}
16042/3	Y	530	Oxygen / 1*10^{-4}	6	5·10^{-8}

3.2.2 Influence of oxygen partial pressure

Another fundamental parameter that influences the physical characteristics of the deposited layer in a molecular beam deposition process is the oxygen partial pressure during Al_2O_3 growth. Hence, the second part of the experiments concerns with aluminium oxide layers grown by exposing the silicon wafer to aluminium molecular beams in oxygen ambient.

The electrical characterisation of samples grown under different oxygen pressure shows that for oxygen partial pressure lower than 1·10^{-4} mbar, the aluminium flow is predominant and an Al-rich layer will be deposited (Subsection 3.3.1.2, figure 3.5). A stoichimetric Al_2O_3 layer can be obtained in UHV-system working with an oxygen partial pressure equal to 1·10^{-4} mbar. Moreover, this was the maximal oxygen pressure that could be used in the UHV-system, since working with p_{O2} higher than 1·10^{-4} mbar would lead to the oxidation of the aluminium source (Al-crucible), enabling further Al-evaporation as illustrated in figure 3.4 (Subsection 3.3.1.2).

Process conditions, oxygen pressure, thickness and substrate temperature are indicated in table 3-3.

Table 3-3 Influence of oxygen partial pressure during Al_2O_3 deposition process. The process parameters are summarized

Wafer no.	**Thermal Desorption**	**$T_{substrate}$** [°C]	**Ambient / Pressure** [mbar]	**$t_{Physical}$** [nm]	**$J_{Leakage}$ @ -1V** [A/cm^2]
11083/1	Y	500	Oxygen /1*10^{-5}	5	0.02
11083/3	Y	500	Oxygen /5*10^{-5}	5	7·10^{-5}
11083/4	Y	500	Oxygen / 1*10^{-4}	5.4	5·10^{-9}

3.2.3 Ozone Enhanced Growth of Aluminium Oxide

Ozone was investigated as oxidizing source to be integrated in the aluminium oxide deposition process. The advantage of the ozone compared to oxygen is that O_3 is an higher reactive gas, so that Al_2O_3 deposition at low substrate temperature should be possible.

Ozone (O_3) is a light blue gas, with a very intensive and characteristic smell and a boiling point of 112°C. A detailed summary of ozone properties can be found in [Neu98].

At atmospheric pressure ozone can partially dissolve in water. At standard pressure and temperature the solubility of ozone is thirteen times that of oxygen. O_3 has an oxidation potential of 2.07 V. This means that ozone is a strong oxidizer, in fact it is one of the strongest oxidizers available for water treatment. It can also be very dangerous, since concentrated mixtures of ozone and oxygen with more than 20% ozone can become explosive in both fluids and gases.

Ozone is fairly unstable in a watery solution; its half-life in water is about 20 minutes. Its half-life strongly depends from temperature: at room temperature O_3 has a half-life of 12 hours, while it reduces to 1.5s at 250°C [Ozone].
Typical O_3 half-life vs. Temperature values are reported in Table 3-4.

Aluminium oxide films were grown in UHV using oxygen and ozone as oxidising source. For both gases, the partial pressure was fixed at $p_{O2/O3}=1\cdot10^{-4}$mbar. This pressure was chosen taking into account the investigation on the influence of the oxygen pressure on aluminium oxide films, as previously reported (subsection 3.2.2).

The ozone flux was produced by an ozone generator connected to the UHV process-chamber. A description of the ozone generator can be found in the PhD Theses "Ultrahochvakuum (UHV)-kompatible Herstellung von Niedertemperaturoxiden für die Mikroelectronik" [Neu98].
The influence of the substrate temperature ($T_{Substrate}$) was investigated by growing aluminium oxide at room temperature (RT) and at $T_{Substrate}$=500°C. The process parameters are reported in Table 3-5.

Current density vs. voltage characterisation shows that ozone enhanced deposition at room temperature already allows the growth of Al_2O_3 samples having low leakage current (Subsection 3.3.1.3, figure 3.6). More information can be extracted from capacitance vs. voltage characterisation C(V) (Subsection 3.3.2.1, figure 3.9), from which it can be seen that Al_2O_3 grown in ozone ambient at room temperature has lower capacity in inversion region, hence a lower dielectric constant compared to oxygen grown samples.

The reason of the capacity reduction evidenced during ozone enhanced oxidation of aluminium is probably the formation of silicon dioxide layer at the interface between gate oxide and silicon substrate. This SiO_x layer is responsible of the low leakage current evidenced in J(V) measurements, but it also strongly reduces the dielectric constant of the gate oxide and increase the equivalent oxide thickness of the deposited layer. These experiments suggest that a process control during the first phases of the oxidation process is very difficult in presence of ozone ambient.

Table 3-4 Typical ozone half-life vs. temperature. These values are based on thermal decomposition. No wall effects, humidity, organic loading or other catalytic effects are considered [Ozone].

Temperature [°C]	**O_3 half-Life**
-50°C	3 months
-35°C	18 days
-25°C	8 days
20°C	3 days
120°C	1.5 hours
250°C	1.5 seconds

Table 3-5 Process condition for MBD-Al2O3 grown in ozone ambient compared with samples grown in oxygen ambient**.**

Wafer no.	Thermal Desorption	$T_{substrate}$ [°C]	Ambient / Pressure [mbar]	$t_{Physical}$ [nm]	ε
16042/4	Y	500	Oxygen /$1*10^{-4}$	6	8
03052/6	Y	500	Ozone /$1*10^{-4}$	6	6
03052/7	Y	RT	Ozone / $1*10^{-4}$	7	6.3

3.2.4 Influence of the annealing ambient

To investigate the influence of the annealing ambient and the thermal stability of the MBD-grown aluminium oxide, Al_2O_3 films were annealed ex-situ at 600°C in nitrogen and oxygen ambient.

Capacitance vs. voltage characteristics of the $Al/Al_2O_3/Si$ capacitors highlight important differences depending on the annealing procedure of the aluminium oxide (Subsection 3.3.2.2). Annealing in oxygen ambient leads to a strong reduction of the capacitance in accumulation region, which indicate a reduction of the dielectric constant ε of the gate oxide. The influence of the oxygen content have been investigated by annealing Al_2O_3 samples, grown under the same condition, in nitrogen ambient and nitrogen with 10% oxygen. Annealing in presence of oxygen strongly reduced the dielectric constant of the system.

3.2.5 Influence of the Si-substrate preparation before Al_2O_3 deposition

One of the key step for the introduction of high-k materials as gate oxide for CMOS devices is the optimisation of the interface between silicon substrate and the dielectric layer. Interface engineering and the influence of the Si-interface preparation on MOS capacitors having Al_2O_3 as gate oxide is argument of Chapter 4 of this work theses. Here a short summary of the pre-deposition treatments studied in relation with Al_2O_3 deposition are reported (Table 3-5).

Growing aluminium oxide on silicon wafer which have seen a thermal desorption of the SiO_2 layer formed during RCA cleaning (chemical oxide) already furnish satisfactory results. Anyway, the introduction of a carbon removal step before dielectric deposition leads to an evident amelioration of the electrical performances of the MOS capacitors and suggests that C-burning strongly improves the interface quality between gate oxide and semiconductor.

Table 3-6 Si-substrate preparation before Al_2O_3 deposition

Si-substrate preparation before Al_2O_3 deposition *MBD - Al_2O_3* *Annealing in furnace* *(nitrogen, 600°C, 30 min)*	**Quality**
Chemical Oxide	-
Chemical Oxide + TD	+
Chemical Oxide + C-burning	++
Chemical Oxide + C-burning + TD	-
HF-last + C-burning	++

3.3. Electrical characterisation

The electrical quality of the MBD-grown aluminium oxide films has been investigated by means of current density vs. voltage J(V) and capacitance vs. voltage measurements C(V) of MOS capacitors. After deposition, aluminium contacts were evaporated to perform electrical characterisation. A description of the measurement set-up and measurement conditions are reported in Chapter 2 (2.2.1 and 2.2.2).

3.3.1 Current Density vs. Voltage (J-V) Measurements

Current density vs. voltage characterization gives a first important indication about the quality of the gate oxide. The conduction mechanism for Al_2O_3 films may be affected by defects and trapping states present in the deposited films [Carter01]. Current density vs. voltage measurements for aluminium oxide thin films MBD-grown in UHV system have been used in a first moment to qualify and optimise the deposition process and in a second moment to study the conduction mechanism in Al_2O_3 films.

3.3.1.1. Influence of substrate temperature on J(V)

The influence of the substrate temperature ($T_{Substrate}$) on the quality of Al_2O_3 gate oxide was studied for a temperature range 25°C – 530°C. Process conditions used during the deposition, thickness and substrate temperature are introduced in subsection 3.2.1 and summarised in table 3-2.

Current density vs. voltage characteristics are reported in figure 3.2 for as-grown aluminium oxide samples. J(V) measurements of Al_2O_3 as-grown films evidence that the higher the substrate temperature the lower the leakage current for samples having comparable thickness. Only aluminium oxide films grown with a substrate temperature equal or higher than 500°C have low leakage current. For this reason, further investigation have been concentrated on Al_2O_3 deposition within the temperature range $T_{Substrate}$=500–530°C.

In figure 3.3, current density vs. voltage J(V) measurements for Al_2O_3 films grown with a substrate temperature $T_{Substrate}$=500°C and $T_{Substrate}$=530°C are reported. As-grown and furnace annealed (N_2, 600°C, 30min) characteristics are compared.

The leakage current ($J_{Leakage}$) for as-grown aluminium oxide films deposited in UHV is in the same range for both samples grown with $T_{Substrate}$=500°C and $T_{Substrate}$=530°C (open symbols, figure 3.2). After nitrogen annealing important differences are evidenced between the two samples: Al_2O_3 film grown with a substrate temperature of 500°C (fig. 3.3, down triangles) has low leakage current comparable with as-grown sample. $J_{Leakage}$ strongly increase for the sample grown with $T_{Substrate}$=530°C (fig. 3.3, square symbol).

The reason for this behaviour could be explained by the beginning of crystallisation process. [Kundu02a, Copel01, Krug00] report that oxidation of Al_2O_3 films on Si(100) for temperature higher than 550°C can causes instabilities in the film due to extensive intermixing. As well, it is reported that depending on the process conditions crystallisation of aluminium oxide can already starts for substrate temperature in the range of 550°C [Guha01].

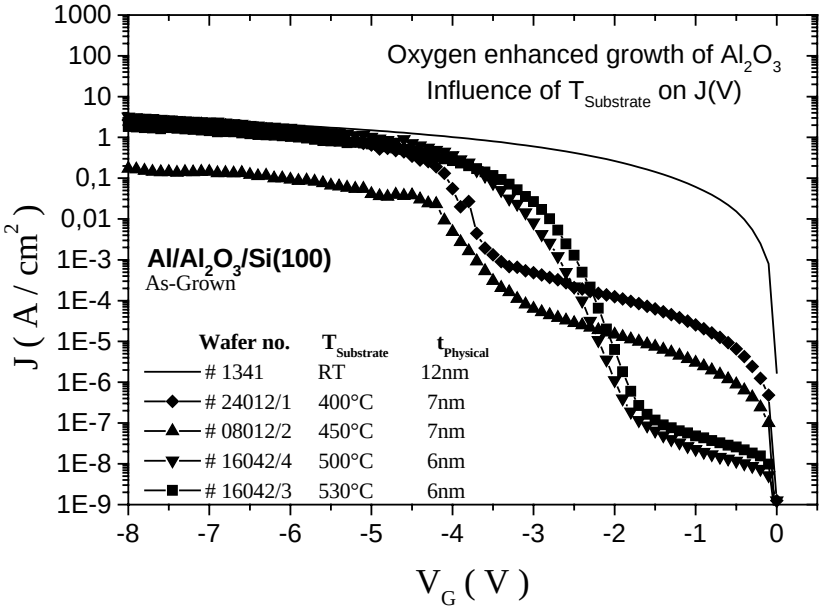


Figure 3.2 As-Grown samples. Leakage current vs. gate voltage J(V) of MOS capacitors having an Al_2O_3 gate oxide grown under the same process conditions (ambient, gas pressure, deposition rate) and substrate temperature in the range 25°C – 530°C. The higher the substrate temperature the lower the leakage current for samples having a comparable thickness. Process condition summarised in Tab. 3-2.

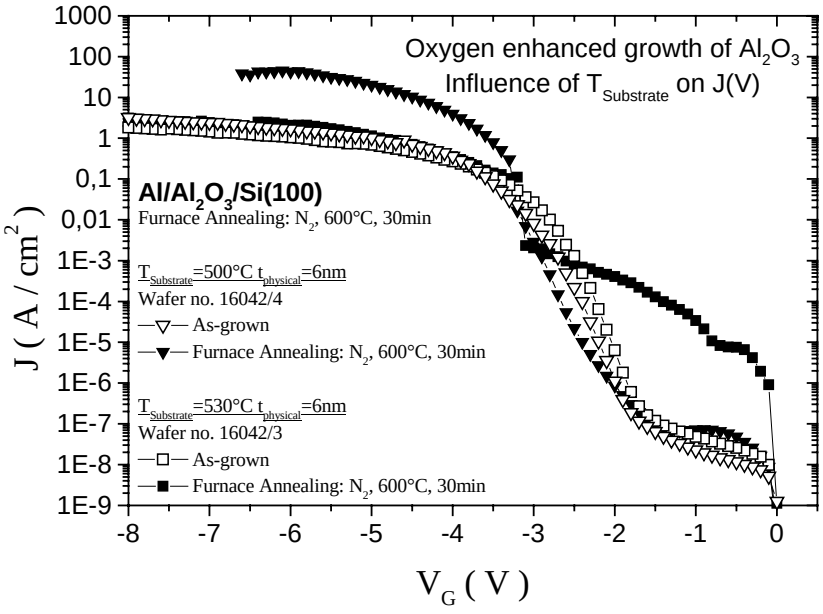


Figure 3.3 As-grown (open symbols) and furnace annealed (N2, 600°C, 30min – close symbols) samples. Leakage current vs. gate voltage J(V) for Al_2O_3 films grown with $T_{Substrate}$=500°C and $T_{Substrate}$=530°C. Excessive substrate temperatures during aluminium oxide growth lead to high leakage current due to the beginning of the crystallization in the deposited film.

3.3.1.2. Influence of the oxygen pressure on J(V)

The influence of oxygen partial (p_{oxygen}) pressure during Al_2O_3 deposition in UHV-system has been investigated on the electrical properties of aluminium oxide films grown under different ambient pressure (subsection 3.2.2).

Depending on the oxygen pressure the stoichiometry of the Al_2O_3 deposited layers strongly varies. For low oxygen pressure the aluminium flow will be predominant and an Al-rich layer would be deposited. For high oxygen pressure the excess of O_2 reacts with the silicon substrate forming a SiO_x layer at the interface with silicon substrate, reducing hereby the dielectric constant of the dielectric stack.

Another important consequence of the high oxygen pressure is the possible oxidation of the aluminium source (Al-crubible), producing a thin Al_2O_3 film on the melted aluminium which closes the crucible and disable further aluminium evaporation.

Maintenance work of the UHV system after Al evaporation in high oxygen partial pressure ($p_{O2}>1\cdot10^{-4}$ mbar), in fact, evidenced a double inhibition process: from one side the oxygen gas start oxidising the surface of the melted aluminium, from the other side part of the evaporated aluminium stays on the crucible walls where it is oxidised (Al_2O_3 powder was visible on the crucible's walls after UHV processing for $p_{O2}>1\cdot10^{-4}$ mbar). It is known that if liquid aluminium is in a O_2-rich ambient, the Al surface undergoes to a rapid oxidation. Just after 40s of oxidation about a 1nm thick aluminium oxide is formed on the Al surface [Kundu03]. For long processing time in high oxygen pressure the two phenomena evidenced above forms a Al_2O_3 cap on the crucible which disables further aluminium evaporation (figure 3.4).

Current density vs. voltage characteristics for aluminium oxide films grown with different oxygen partial pressure are reported in figure 3.5. Process conditions, oxygen pressure, thickness and substrate temperature are indicated in table 3.3.

As can be observed from the J(V) characteristics the leakage current of the gate oxide decreases by increasing the oxygen partial pressure. For low oxygen pressure (p_{oxygen} $<1\cdot10^{-4}$ mbar) the aluminium flow is predominant and an Al-rich layer will be deposited. XPS analysis (reported later) shows that stoichimetric Al_2O_3 layer can be obtained in UHV MBD system by growing the samples with an oxygen pressure equal to $1\cdot10^{-4}$ mbar.

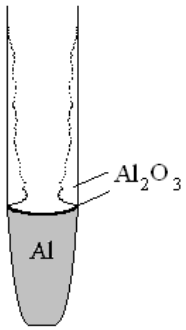


Figure 3.4 Inhibition processes during aluminium evaporation. Part of the Al-beam oxidised on the crucible's walls (white powder). Moreover, the aluminium source undergoes to a rapid oxidation (surface in contact with oxygen). For long processing

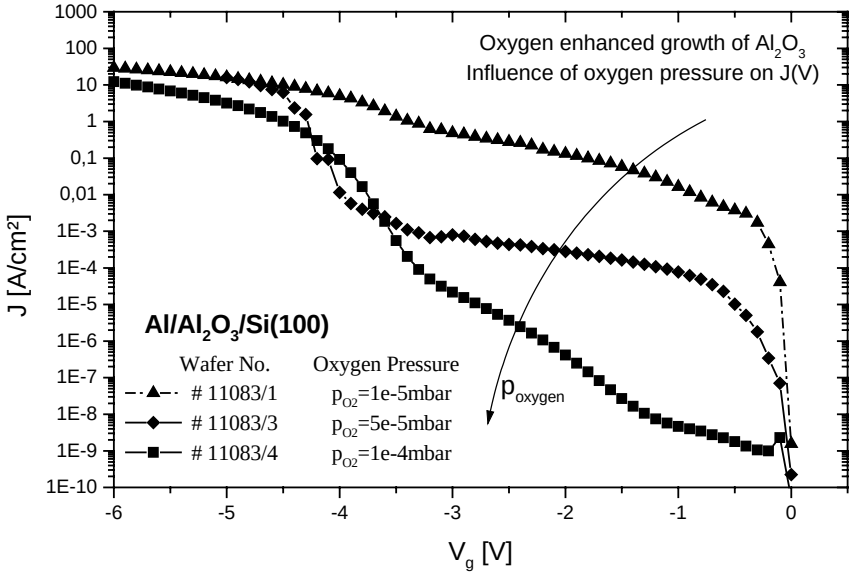


Figure 3.5 Leakage current vs. gate voltage J(V) Al_2O_3 gate oxide on Si(100). Samples grown under different oxygen partial pressure. Process condition summarised in Table 3-3. For oxygen partial pressure lower than $1 \cdot 10^{-4}$ mbar, the aluminium flow is predominant and an Al- rich layer will be deposited. Stoichimetric Al_2O_3 layer can be obtained in UHV MBD system by growing the samples with an oxygen pressure equal to $1 \cdot 10^{-4}$ mbar.

3.3.1.3. Ozone Enhanced Growth of Aluminium Oxide

The capability to grow aluminium oxide films in UHV ambient using low substrate temperature to guarantee the deposition of amorphous layers is the basis for the investigation using ozone as oxidizing gas. It is known that ozone is a strong oxidizer (paragraph 3.2.3) which promotes the reaction between Al- and O- already at low temperature (T<550°C).

Aluminium oxide films having the same physical thickness (Table 3-5) were grown in oxygen and ozone ambient with a constant pressure of $p=1 \cdot 10^{-4}$mbar and different substrate temperature (25°C and 500°C). The current density vs. voltage characteristics J(V) are reported in figure 3.6. The J(V) measurements show that aluminium oxide grown by ozone enhanced deposition at a substrate temperature of 25°C has already low leakage current (fig. 3.6, cross symbol).

If the substrate temperature increases, the half-life of ozone is strongly reduced [ozone] and O_3 quickly dissociates in O_2. This phenomena can be highlighted growing aluminium oxide films at high temperature in both O_2 and O_3 ambient. Al_2O_3 samples grown with a substrate temperature of 500°C in ozone and oxygen atmosphere (fig. 3.6, square symbol for O_3- and pyramids for O_2-ambient) do not present significant differences.

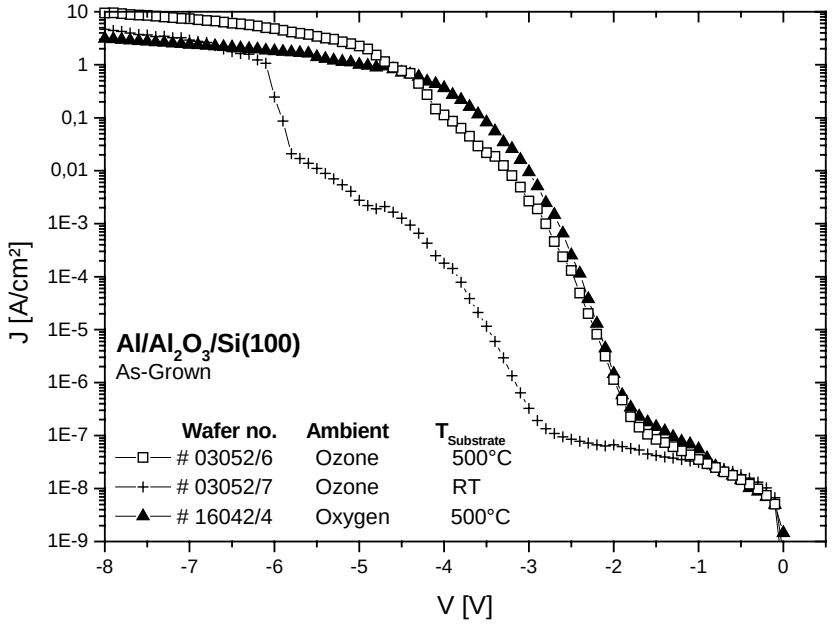


Figure 3.6 J(V) characteristics for ozone enhanced deposition of Al_2O_3 compared with aluminium oxide samples grown in oxygen ambient. The wafers have been processed at the same oxidizing partial pressure ($p_{O3/O2}=1\cdot10^{-4}$mbar) and different substrate temperature. Process condition summarised in Table 3-5.

3.3.1.4. Conduction Mechanism in Al_2O_3

In general the conduction mechanism depends on the thickness of the gate dielectric. For thicker layers two current regimes can be distinguished. At low voltages the current density gradually increases; this transient current strongly depends on the delay time used for the measurement. At higher voltages, MBD Al_2O_3 films present the expected Fowler-Nordheim (FN) Tunneling conduction mode, highlighted by a straight line in the FN-characteristics reported in fig. 3.7.

The typical FN plot can be found according to the equation (3.1):

$$J = \frac{q^3 E^2}{8\pi h \phi_B} \exp\left(-\frac{8\pi\sqrt{2m^*}\cdot \phi_B^{\,3/2}}{3hq\cdot E} \right) \;\rightarrow\; \ln\left(\frac{J}{E^2}\right) = \ln A + \frac{B}{E} \qquad (3.1)$$

$$\text{with } B = -\frac{8\pi\sqrt{2m^*}\sqrt{q}}{3h}\phi_B^{3/2} = -6{,}83\cdot10^9\left(\frac{m^*}{m}\right)^{1/2}\phi_B^{\,3/2} \qquad \left[\frac{\mathrm{V}}{\mathrm{m}}\right]$$

where J is the current density, E is the oxide field, q is the electronic charge, m_0 is the free electron mass, m* is the electron mass in the oxide and ϕ_B is the barrier height in eV.

According to equation 3.1, the slope B is a function of the effective electron mass m* and the barrier height ϕ_B of the dielectric; keeping one of the two values constant, the remaining parameter can be calculated (extracted data in fig. 3.7). Fixing the value of

Al_2O_3 barrier high ϕ_B=2.8eV the extracted effective electron mass for MBD-grown Al_2O_3 is m*=0.5 m_0, which identify Al_2O_3 [Kim02].

When the thickness of the aluminium oxide layers is reduced, the trap distance may be such that a significant amount of trap-assisted direct tunneling is measured and the leakage mechanism is a combination of direct tunnelling and defect-related conduction. This conduction mechanism can be observed in the high leakage current measured for MBD-Al_2O_3 film with a physical thickness of 1.5nm and illustrated in figure 3.8. Similar results have been also reported by Carter et al. [Carter01].

High breakdown fields (V_{BD}), close to silicon dioxide value, have been evidenced for very thin Al_2O_3 films (figure 3.8): for aluminium oxide layers having a thickness of 1.5nm, the breakdown happens at V_g=-2V, giving a breakdown field $E_{BD}=V_g/t_{ox}$ =10MV/cm.

For thicker aluminium oxide layers grown in UHV (5-10nm), the breakdown field extracted from J(V) measurements are included in the range 2-7MV/cm. These values are slightly smaller than V_{BD} for silicon dioxide ($V_{BD(SiO2)}$=10MV/cm, p. 407 [Sze]) and stays in the same range than literature reported data for Al_2O_3. In fact, the indicated breakdown fields for aluminium oxide are less than 5MV/cm for amorphous films [Machanda98][Carter01], and higher V_{BD} of 8-10MV/cm are reported for crystalline Al_2O_3 films [Shahj02].

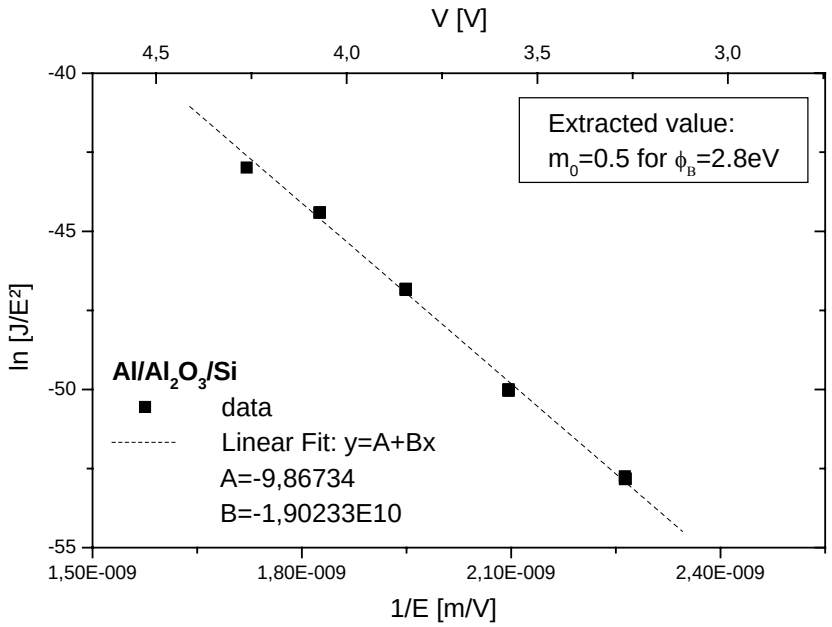


Figure 3.7 Fowler-Nordheim plot of Al_2O_3 film (5nm) at high voltage. Straight line characteristic of FN-tunneling.

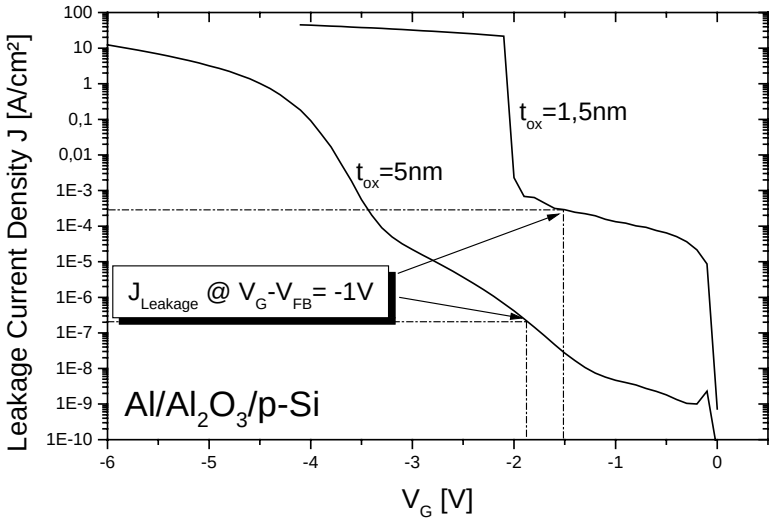


Figure 3.8 Leakage current density vs. gate voltage respectively for 5nm MBD Al_2O_3 and 1.5nm MBD Al_2O_3 physical thickness

3.3.2 Capacitance vs. Voltage (C-V) Measurements

Capacitance vs. voltage characterization has been used to determine fundament parameters which characterise the gate oxide layer in an MOS capacitors: dielectric constant (ε), equivalent oxide thickness (EOT) and interface state density (D_{it}).

3.3.2.1. Ozone Enhanced Growth of Aluminium Oxide

A deep study of the physical and electrical properties of aluminium oxide films grown in ozone ambient is possible by means of capacitance vs. voltage measurements. Al_2O_3 thin films have been grown by MBD in oxygen and ozone ambient. The process parameters are reported in Table 3-5.

Current density vs. voltage J(V) measurements (figure 3.6) confirms the high-oxidizing property of ozone. This can be derived from comparable leakage currents of aluminium oxide samples grown in ozone ambient with a substrate temperature $T_{Substrate}$=25°C and Al_2O_3 films grown using oxygen as oxidizing gas and a $T_{Substrate}$=500°C.

Capacitance vs. voltage C(V) characteristics of aluminium oxide samples grown in ozone ambient at room temperature are reported in figure 3.9. The C(V) have been measured for 20MHz.

As-grown samples have low hysteresis, indicating that few mobile charges are present in the dielectric. On the other hand they show high interface state density ($D_{it}=3\cdot10^{13}eV^{-1}cm^{-2}$), highlighted in figure 3.9a) by the high conductance peak G(V).

After furnace annealing in nitrogen at 600°C for 30 min, the hysteresis is further reduced and the D_{it} shrinks of one order of magnitude (figure 3.9b).

The dielectric constant extracted from C(V) measurement is around 6 for both as-grown and furnace annealed aluminium oxide. This low ε is explained by the growth of a SiO_x layer at the interface between Al_2O_3 and silicon substrate. A confirmation of the presence of a silicon oxide layer at the interface with the substrate is also given by the evident two peaks in G(V)-curve for annealed samples (fig. 3.9b, bottom), which indicates a two-layer system .

The C(V) measurements for aluminium oxide films having similar physical thickness, grown in oxygen and ozone ambient with a constant pressure of $p=1\cdot10^{-4}$mbar and different substrate temperature (25°C and 500°C) are reported in figure 3.10. As reference, the expected theoretical curve is also reported [Sze].

Al_2O_3 films grown in ozone ambient have lower dielectric constant (ε) compared to oxygen-growth ones (see table 3-7). Moreover, only O_2 grown films have C(V) shape close to the theoretical behaviour (fig. 3.10, pyramid symbols), while ozone-grown samples show bumps in the depletion region indicating a two-layer system (figure 3.10, square and cross symbols).

The principle parameters that can be extracted from C(V) and G(V) measurements are reported in table 3-7. In particular, starting from the value of the capacitance measured in accumulation, the dielectric constant of the Al_2O_3 film is calculated and the equivalent oxide thickness (CEOT) is obtained. Interface state densities calculated by Brews theory [Brews83] are as well reported.

As anticipated in paragraph 3.2.3, the reported C(V) curves suggest that during ozone enhanced aluminium oxidation a silicon oxide layer is formed at the silicon interface. This SiO_x layer is responsible of the low leakage current observed in the J(V) measurements, but strongly reduces the dielectric constant of the gate oxide (from 8 to 6) and increase the equivalent oxide thickness of the gate-stack.

Scope of this research work is to find a deposition process which allows the growth of aluminium oxide film having high dielectric constant, as close as possible to the theoretical value ε_{Al2O3}=9-10. The thicker interface oxide formed during Al_2O_3 growth in ozone ambient and observed in the C(V) measurement limits prevent from reaching this topic. For this reason, oxygen have been chosen as standard oxidising ambient.

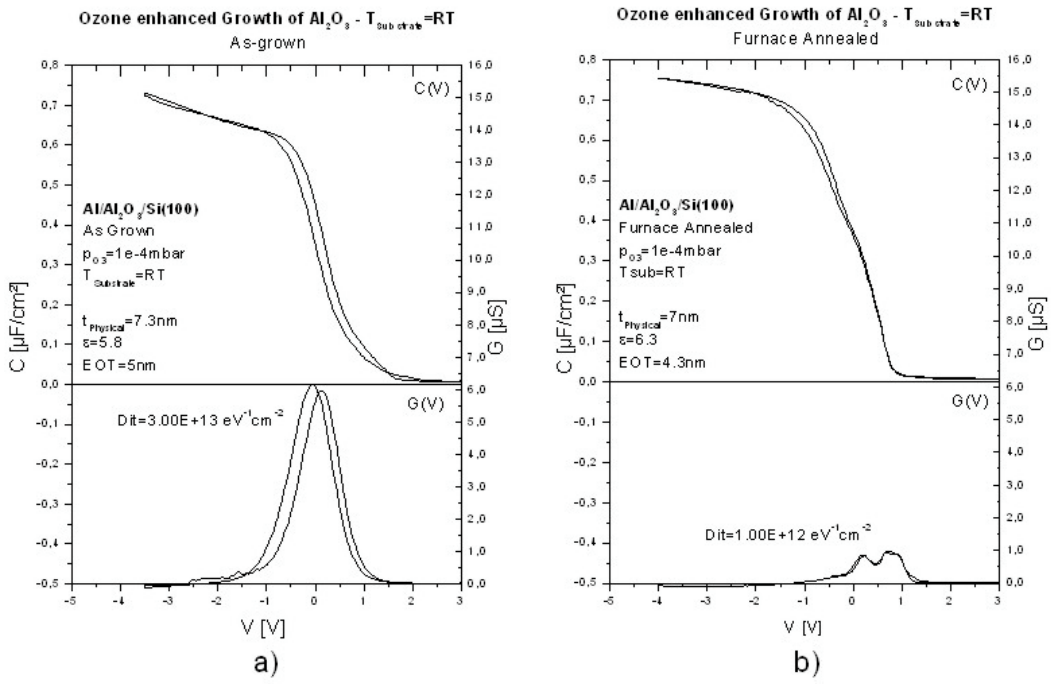


Figure 3.9 C(V) and G(V) hysteresis measurements 7nm-thick Al_2O_3 film grown in O_3 ambient at room temperature. Frequecy=20MHz. a) as-grown: high D_{it}; b) furnace annealed (N_2, 600°C, 30min: hysteresis and D_{it} are reduced

Table 3-7 EOT and D_{it} extracted from C(V) measurements. All the annealing have been done in nitrogen for 30 min at 600°C.

Process (Wafer no.)		C/A F/cm²	T_{Al2O3} nm	ε_r	CEOT nm	Dit [$eV^{-1}cm^{-2}$]
Oxygen Ambient (# 16042/4)	Furnace					
p=1·10^{-4}mbar	Annealing	9,50E-07	7,2	8	3,6	5,00E+11
Tsub=500°C	N_2, 600°C, 30min					
Ozone Ambient (# 03052/6)	Furnace					
p=1·10^{-4}mbar	Annealing	9,50E-07	5,5	6	3,6	7,00E+11
Tsub=500°C	N_2, 600°C, 30min					
Ozone Ambient (# 03052/7)	Furnace					
p=1·10^{-4}mbar	Annealing	8,00E-07	7,0	6.3	4,3	1,00E+12
Tsub=RT	N_2, 600°C, 30min					

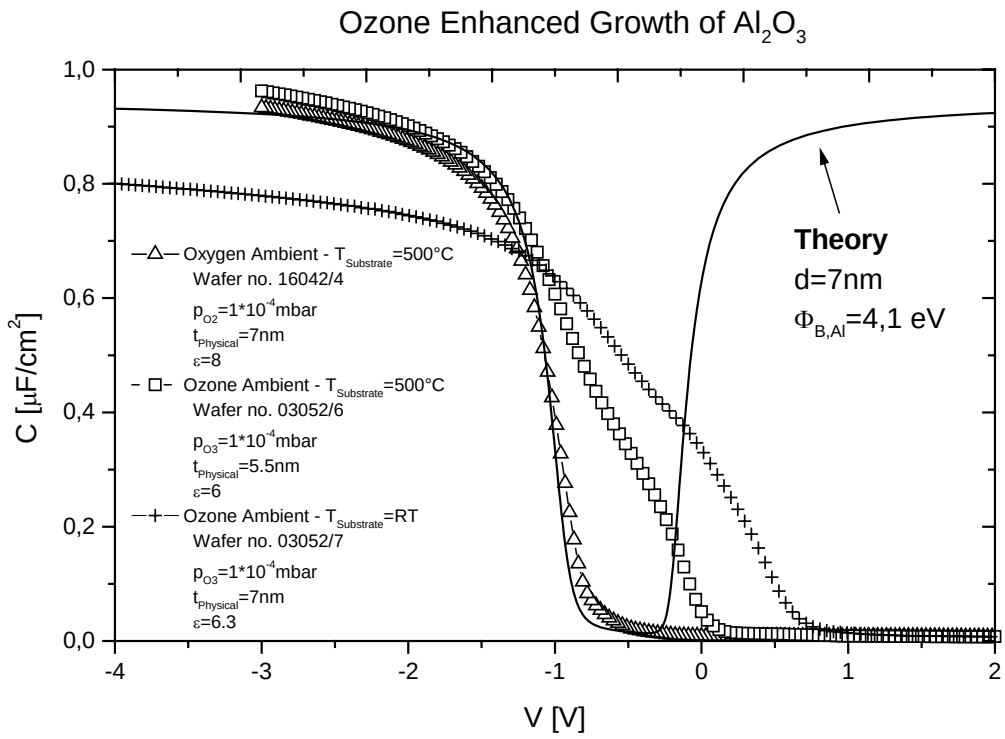


Figure 3.10 Comparison between C(V) measurements for aluminium oxide films having the similar physical thickness, grown in oxygen and ozone ambient with a constant pressure of p=1·10^{-4}mbar and different substrate temperature (25°C and 500°C)

3.3.2.2. Optimisation of the annealing process

The optimisation of the post-growth annealing and the influence of annealing ambient have been investigated by means of capacitance vs. voltage measurements. All MBD-grown aluminium oxide films have been annealed ex-situ in furnace.

During the optimisation phase of the annealing process it has been evidenced that the heating- and cooling-times of the furnace under consideration were very long (10min for 100°C). This factor leads to difficult process-control and process-reproducibility since the samples will spend most of the time in an intermediate temperature-state which cannot be controlled.

For this reason, a maximal annealing temperature of 600°C has been chosen in order to have an effective annealing process and reasonable process time.

In figure 3.11 the capacitance vs. voltage measurements for a 7.5nm-thick Al_2O_3 films annealed in different ambient are reported. Taking the as-grown characteristic as reference (fig. 3.11, straight line) and investigating the variation of the C(V) curves after annealing, the main difference between N_2- and O_2-annealed films is the lower capacitance value measured in accumulation in case of oxygen annealing. Since the physical thickness of the aluminium oxide is the same for both nitrogen- and oxygen-annealed Al_2O_3, this lower capacitance is correlated with a reduction of the dielectric constant ε of the gate stack. Also in this case, as observed in the ozone experiments, the reason of the lower ε is to be reported to the growth of a silicon oxide layer at the interface between Al_2O_3 and substrate.

This result is also explained by the observation reported by Almeida et al. [Alme03], indicating that aluminium oxide is not a barrier for oxygen: during furnace annealing in presence of oxygen, this diffuses through Al_2O_3 film to reach the silicon substrate and forms there a SiO_x layer.

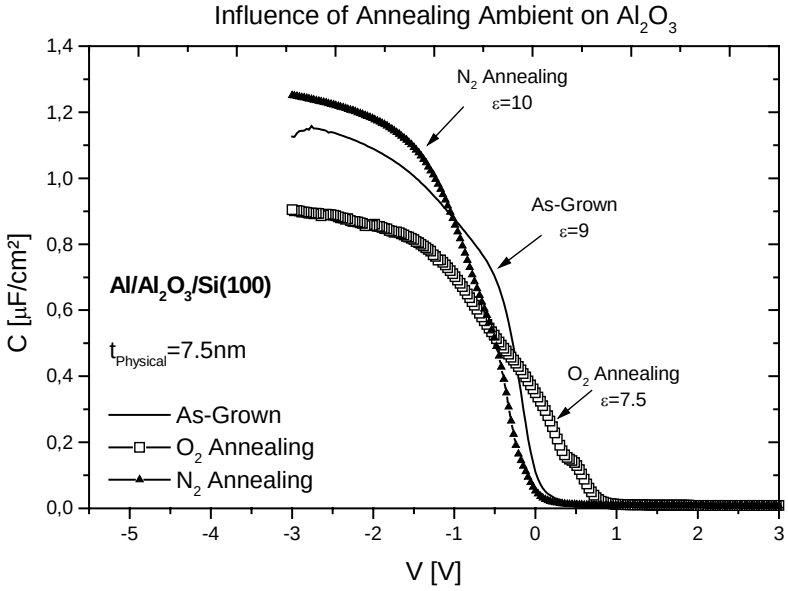


Figure 3.11 C(V) measurements for aluminium oxide grown in oxygen ambient and submitted to different furnace annealing. As-grown (straight-line), annealed in N_2 ambient (up triangle) and annealed in O_2 ambient (square). Frequecy=20MHz. Oxygen annealing produces the growth of an interface oxide which reduces the dielectric constant of the gate stack.

The next step will be to investigate the influence of the oxygen content on the annealing of aluminium oxide. At this scope, Al_2O_3 samples grown under the same conditions have been annealed in nitrogen ambient and in nitrogen with 10% percent oxygen. The results of the capacitance vs. voltage measurements are reported in figure 3.12.

Like it was expected, annealing in presence of oxygen strongly reduced the capacitance measured in accumulation for the $Al/Al_2O_3/Si$ system. Similar results have been reported in literature. Copel et al. [copel01], for example, observed that Al_2O_3 films deposited directly on Si(100) were stable under oxidation, but relatively low oxygen pressure were sufficient to cause substantial growth of SiO_2 underneath the aluminium oxide films. Yu et al. [Yu02] goes further in this investigation and affirms that the active oxidation source during annealing, responsible for the interface layer growth, is the oxygen present in an N_2 ambient and not the O_2 species present in the high-k films themselves.

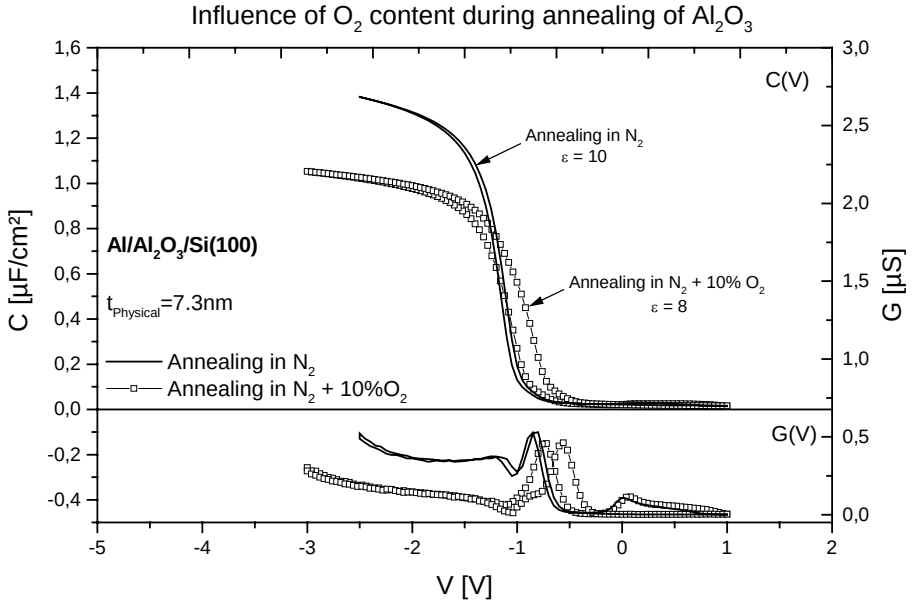


Figure 3.12 C(V) measurements for aluminium oxide grown in oxygen and submitted to different annealing: N_2 (black) and N_2-O_2 (blue) ambient. Frequecy=20MHz.

The influences of the annealing-temperature and annealing-ambient on Al_2O_3 films have been deeply investigated. [Copel01, Kundu02b] found out that degradation was not observed in the Al_2O_3/Si system for UHV annealing at temperature as high as 900°C. A diffusion-reaction model have been proposed by Krug and Almeida et al. [krug00, Alme00] in their study on rapid thermal annealing of aluminium oxide grown on silicon substrate. This diffusion-reaction model describes the role of oxygen during annealing: O_2 from the gas phase plays an essential role in promoting atomic transport and chemical reaction. Oxygen, aluminium and silicon atoms can take two different states: mobile and fixed. In the case of oxygen the mobile state corresponds mainly to O_2 diffusing during annealing, while in the case of Al and Si it corresponds to interstitial positioned atoms. When the Al_2O_3/Si structure is exposed to a given O_2 pressure, this oxygen diffuses through the initial Al_2O_3, reaching the silicon substrate and forming a silicon oxide at the interface between substrate and gate dielectric. As oxidised silicon occupies a larger

volume it will generate interstitial silicon atoms that are prone to move. Hence, silicon oxidation has two effects: it transform the state of oxygen from mobile to fixed and the state of some silicon atoms from fixed to mobile. Mobile silicon are spread through the sample into the Al_2O_3 regions: here mobile Si may displace Al, since the formation of silicon oxide is thermodynamically favoured over that of aluminium oxide. This reaction fixes silicon in the original Al_2O_3 region and transfers fixed aluminium and oxygen from Al_2O_3 networks to mobile states. In this way, mobile Al and O atoms could reach the surface and escape, reducing their total amount in the sample. Since interstitial Si is generated by oxidation of Si and interstitial Al is created by reaction involving interstitial Si, in the absence of Si oxidation there is neither Si and Al transport nor Al loss.

3.3.2.3. Capacitance vs. Voltage (C-V) characterization of MBD-grown Al_2O_3

The results of capacitance vs. voltage and conductance vs. voltage G(V) measurements for 5nm-thick aluminium oxide grown in UHV-system and annealed in nitrogen at 600°C for 30min are shown in fig. 3.13. The quality of the aluminium oxide was investigated by comparing the measuring data with the theoretical behaviour expected for the $Al/Al_2O_3/Si$ capacitor under investigation. The ideal MIS curve (fig. 3.13, doted line) has been calculated following the theory reported by Sze [Sze, chapter 7].

MBE grown Al_2O_3 has a nearly ideal C-V shape with negligible hysteresis (<10mV). The conductance peaks are also very low and the estimated interface state density D_{it} [Brews83] is smaller or equal to $1 \cdot 10^{11} eV^{-1} cm^{-2}$. Equivalent oxide thickness and flat-band voltage were calculated using the NCSU CVC program [Haus96]. The extracted flat band voltage for a set of sample with different thickness was in the range of –0.6V to –1V, which is very close to the expected value (V_{FB}= –0.8eV) calculated for the $Al\text{-}Al_2O_3\text{-}Si$ system with a Si-substrate resistance of 1–10 Ω·cm and a Al work-function of 4.1eV.

The physical Al_2O_3 thickness is related to the SiO_2 equivalent oxide thickness by the formula $t_{Al2O3}=(\varepsilon_{Al2O3}/\varepsilon_{SiO2})t_{SiO2}$, where ε_{Al2O3} and ε_{SiO2} are the dielectric constant of Al_2O_3 and SiO_2, respectively. The comparison between electrical- and physical-thickness measured by ellipsometer on a set of aluminium oxide samples grown by MBD leads to a dielectric constant ε in the range of 6 – 9 (figure 3.14), where ε increases by increasing the film thickness.

The lower dielectric constant measured for thin Al_2O_3 films indicates the presence of a thin silicon oxide layer at the interface with silicon substrate. This two-layer gate stack is also confirmed by the double peak in G(V) characteristic shows in figure 3.13.

The formation of an interface oxide layer is caused the interface treatment introduced to remove the carbon contamination before Al_2O_3 deposition (C-burning, see chapter 4) and by the presence of a small percentage of oxygen impurities in the nitrogen used during post-growth annealing.

The influence of this SiO_x layer on dielectric constant of the gate stack increases by reducing the Al_2O_3 film thickness as can be highlight from fig. 3.14. This is due to the fact that the total capacitance of the gate stack is given by the parallel of the capacitance of the SiO_x layer and the capacitance of the Al_2O_3 film. If the thickness of the interface oxide stays constant, at thinner aluminium oxide will correspond lower dielectric constant of the gate stack.

The thickness of the interface SiO_x formed during processing of the $Al/Al_2O_3/Si$ capacitors is a very important parameter because it gives the limit in scaling the gate oxide and the lower EOT that can be reached with the developed process. This thickness can be calculated by representing the equivalent oxide thickness EOT, calculated from the C(V)

measurements, as function of the Al_2O_3 physical thickness ($T_{Physical}$), as reported in figure 3.15. A linear interpolation gives an indication about the thickness of the interface layer between Al_2O_3 and silicon substrate. For MBD-grown Al_2O_3, furnace annealed in nitrogen for 30min at 600°Cm, the SiO_x interface layer in the range of 0.5nm. As such, EOT smaller than 0.5nm cannot be reached with the UHV-deposition process developed for Al_2O_3 thin films.

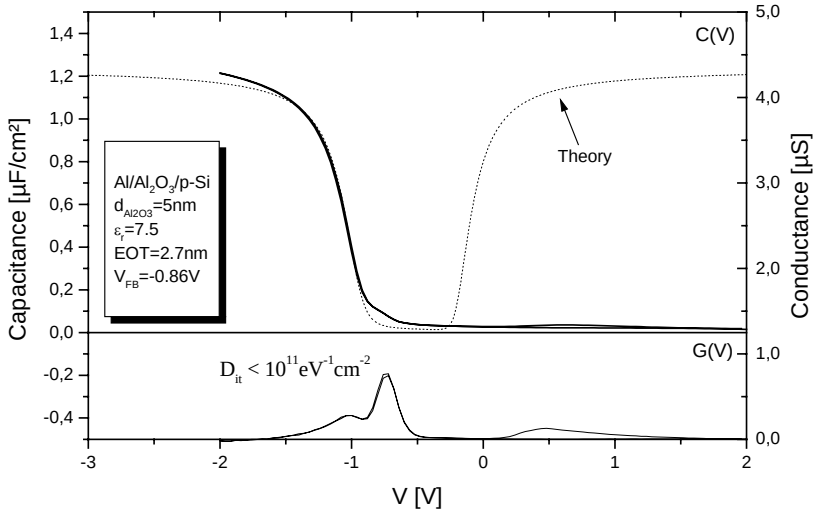


Figure 3.13 C(V) and G(V) measurements for 5nm-thick aluminium oxide grown in UHV-system and annealed in nitrogen at 600°C for 30min. The Al_2O_3 film has a nearly ideal C-V shape with negligible hysteresis (<10mV) and D_{it} smaller or equal to $1 \cdot 10^{11} eV^{-1} cm^{-2}$.

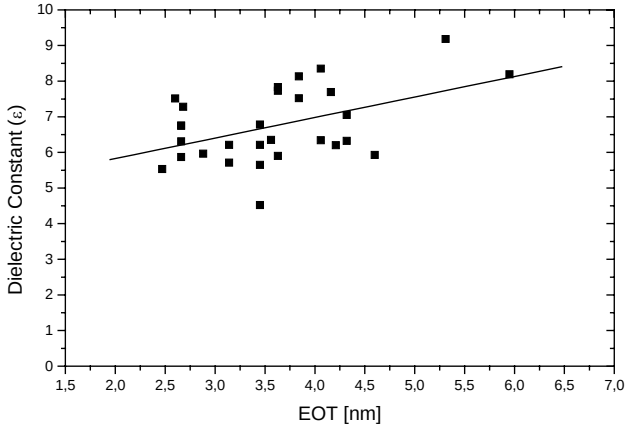


Figure 3.14 Dielectric Constant vs. EOT for a set of MBD-Al_2O_3 samples having different thickness. The thinner the Al_2O_3 layer, the smaller the ε of the gate-stack since the influence of the interface oxide increases

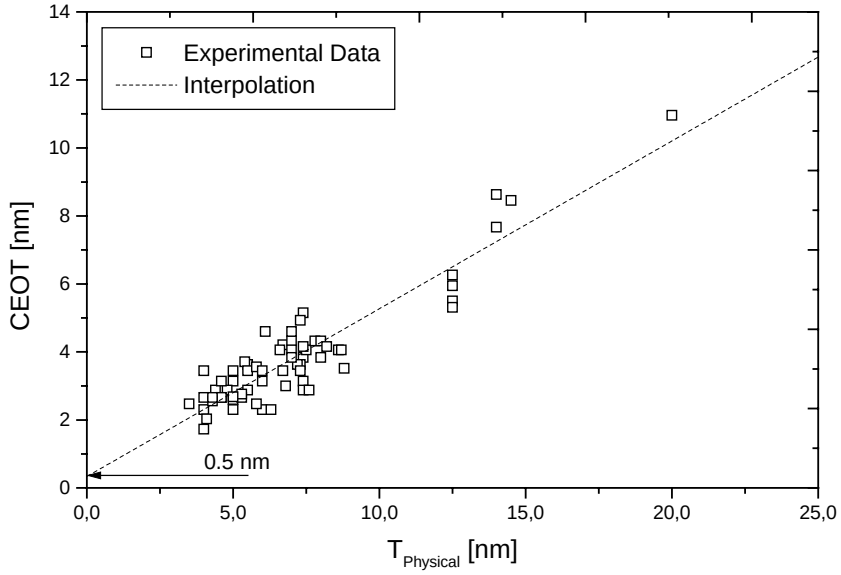


Figure 3.15 EOT vs. physical thickness for MBD-Al_2O_3. The interface-oxide thickness is around 0.5nm.

3.3.3 Comparison of MBD-Al_2O_3 with SiO_2 and Literature Reported Data

One of the principal parameters normally used to compare different dielectric in MOS structures is the leakage current of the gate oxide measured for a V_G-V_{FB}= –1V expressed in function of the equivalent oxide thickness ($J_{Leakage}$ vs. EOT).

High-k dielectric with an electrically equivalent oxide thickness have a lower leakage current than SiO_2. This is because the high-k physical thickness is related to the SiO_2 oxide thickness by the formula:

$$t_{Al2O3} = \frac{\varepsilon_{Al2O3}}{\varepsilon_{SiO2}} \cdot t_{SiO2}$$

where ε_{Al2O3} and ε_{SiO2} are the dielectric constant of Al_2O_3 and SiO_2, respectively. Hence, simply by increasing the dielectric constant the physical thickness gained and the leakage current through the gate oxide will be reduced.

Leakage current for the MBD aluminium oxide thin layer are compared with silicon oxide and literature data in fig. 3.16. The theoretical direct tunnel leakage current density was calculated using the formula reported by Simmon [Simmon63]:

$$J = A^1 \frac{V^2}{e\phi_B \cdot t_{ox}^2} \cdot \exp\left[- B^1 \frac{t_{ox}}{V} (2m)^{1/2} \cdot e\phi_B^{3/2} \right]$$

Where A^1 and B^1 are functions of the elementary charge q and the Planck constant h, t_{ox} is the physical oxide thickness, V the voltage, m the electron mass in the oxide ($m=0.32m_0$ for SiO_2), and ϕ_B is the barrier height (3.2V for the Si/SiO_2 system). The theoretical curve for Al_2O_3 was also calculated by the formula reported by Simmon using the same effective mass of silicon oxide and lower barrier height ($\phi_B=2.8eV$).

MBD Al_2O_3 samples grown with the optimised deposition and annealing processes have a leakage current density which is several orders of magnitude smaller than silicon oxide at

the same equivalent oxide thickness and stay in the range of the best reported literature values (figure 3.16).

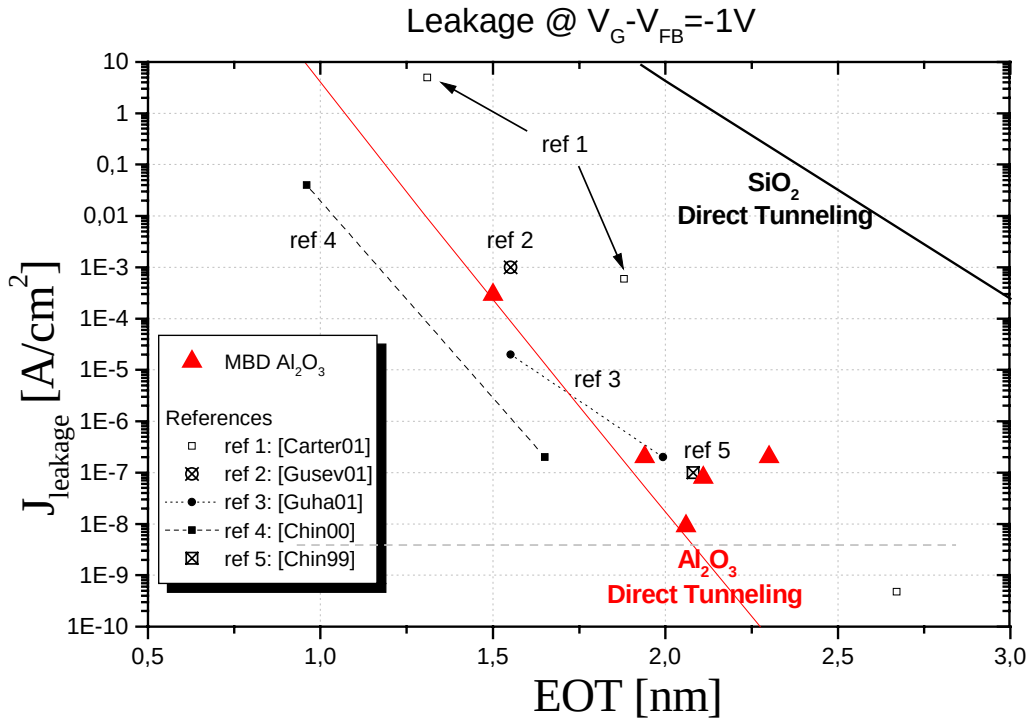


Figure 3.16 Leakage current density vs. EOT of MBE-Al_2O_3 compared with SiO_2 and literature reported data

3.3.4 Parameters for an optimised MBD process of Al_2O_3

The analysis of the experimental results lead to the following specification of the main process parameters for the MBD of aluminium oxide on silicon substrate:

- aluminium evaporation
- oxidising ambient: oxygen
- Substrate Temperature during deposition: $T_{Substrate}$=500°C
- Furnace Annealing: Nitrogen, 600°C, 30min

3.4. Physical Analysis of MBD-grown Al_2O_3 thin films

Aluminium oxide thin films grown by molecular beam epitaxy have been analysed using different techniques in order to study the film composition and stoichimetry. In particular, chemical composition and physical structures of the gate stacks were studied by means of Secondary Ion Mass Spectrometer (SIMS), X-ray Photoelectron Spectrometry (XPS), Auger Electron Spectroscopy (AES), Rutherford Back Scattering Spectrometry (RBS) and high-resolution Transmission Electron Microscope (TEM).

3.4.1 SIMS analysis

In fig. 3.17 a SIMS-Analysis of 12nm-thick Al_2O_3, grown in oxygen ambient (pressure $=1\cdot10^{-4}$mbar, $T_{sub}=500°C$) is reported. Analysed elements are ^{30}Si, ^{27}Al, and the $^{32}(O\text{-}O)$, respectively. It is not possible to measure ^{16}O because of limitations of the SIMS measurement tool (limited sensitivity of the channeltron). The graph displays the count rates versus depth.

Observation: the count rate of silicon increases about four orders of magnitude from noise (Si free Al_2O_3 layer) to a constant rate (Si wafer). The slow rise in the region from 3nm to 9nm indicates the diffusion of Si from the wafer into the Al_2O_3 layer.

Conclusion: the analysed Al_2O_3 layer is to thin to get equilibrium conditions in the count rates of Al and (O-O). The slow decrease in the count rates of Al and (O-O) for depth greater than 20nm is typical for SIMS.

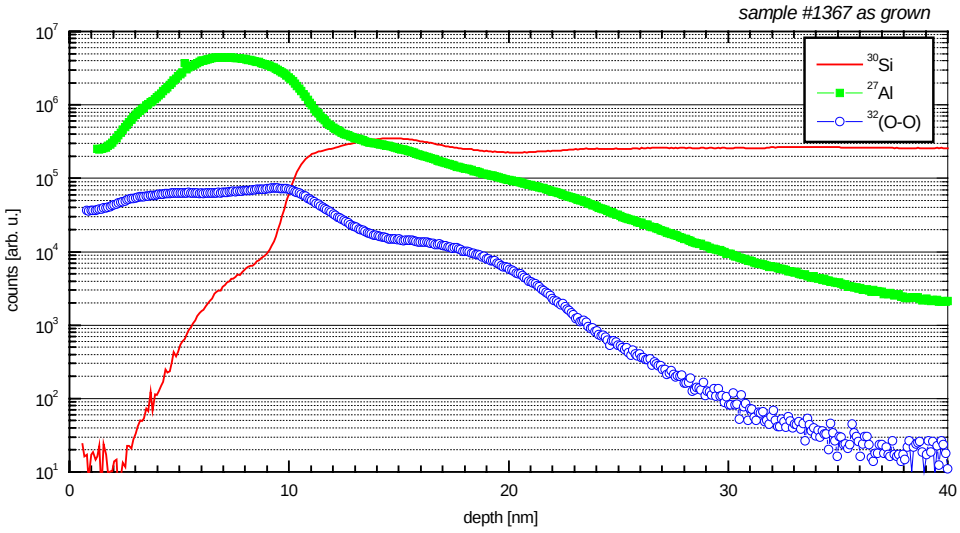


Figure 3.17 SIMS-investigation for 12nm-thick Al_2O_3 grown in oxygen ambient ($p_{O2}=1\cdot10^{-4}$mbar, $T_{sub}=500°C$). The slow rise in the region from 3nm to 9nm indicates the diffusion of Si from the wafer into the Al_2O_3 layer.

3.4.2 AES

A first investigation on the composition of the MBD aluminium oxide was done by Auger analysis. A surface-scan and the AES-spectrum after argon sputtering to remove the carbon contamination are reported in figure 3.18 for a 50nm-thick Al_2O_3.

This investigation technique was only used to detect the elements present in the sample, since it does not allow to measure the stoichiometry of the deposited material.

The position of the peaks in the spectrum are typical for a given element. In this case, three peaks can be clearly evidenced in the surface scan, corresponding respectively to aluminium (E=51eV), carbon (E=263eV) and oxygen (E=505eV).

The composition of the deposited layer inside the film was investigated after sputtering the sample surface to eliminate the carbon contamination due to contact with air. The deep-scan is show in figure 3.18b). It is evident that only aluminium and oxygen are present inside the MBD-grown Al2O3. The shift of the oxygen energy (from 505eV to 497eV) highlights that the detected oxygen is bonded with aluminium.

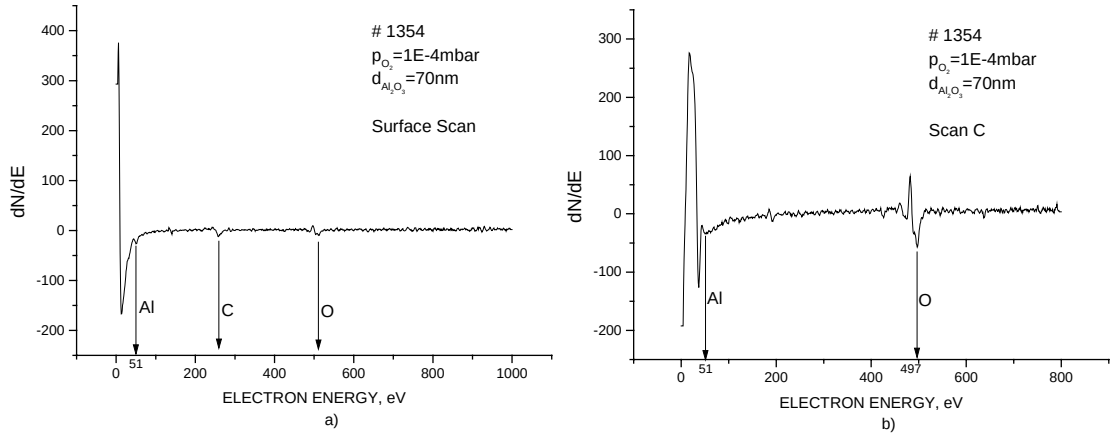


Figure 3.18 AES analysis on wafer #1354: a) superficial scan; b) depth scan

3.4.3 XPS

A complete information on composition and stoichiometry of the deposited layer can be obtained by X-ray Photoelectron Spectroscopy (XPS).

Before to start the investigations, the surface of the sample was sputtered with argon ions in order to eliminate possible carbon contamination. This step was necessary since the XPS analysis were done ex-situ and during transport from deposition chamber to XPS-system the oxide film get in contact with air, leading to carbon contamination of the sample surface as evidenced also from the AES analysis illustrated above.

In figure 3.19 the complete spectrum of a 7 nm annealed Al_2O_3-layer after 12 min Ar-sputtering (approximately 2 nm of the film was etched) is reported. Al_2O_3 film was grown on Si(100) surface at an oxidation pressure of $1 \cdot 10^{-4}$mbar and T_{sub}=500°C.

The molybdenum peaks visible on the spectrum are due to the substrate holder. The C 1*s* peak is at the borderline of the detection limit. Figure 3.20 illustrate the Al *2p*, Si *2p* and O *1s* core level spectra. The Al 2*p* and O 1*s* binding energies of 75 eV and 132eV respectively, indicate that the MBD-grown Al_2O_3 film is stoichiometric. The uniform nature of Al_2O_3 is also confirmed by the fitting of the Al 2*p* spectrum, for which no other aluminium sub-oxide are evidenced. The peak positions were corrected using the C 1*s* as

reference. The double-Si *2p* peak at 99eV and 102eV corresponds to the bulk Si and to Si-O bonding energy. This confirms the results highlighted by the C(V) characterisation, since a silicon peaks for BE=102eV suggests that a thin interface SiO_x layer is formed between the Al_2O_3 film and the silicon substrate.

The percentage of the detected elements can be calculated by measuring the respective peaks area and calibrating the value using specific tooling factors. This calculation can be easily done using a the software Present (Omicron): after background subtraction the major peaks were fitted using the indicated software and the peak areas and element concentration were calculated. The stoichiometry of the aluminium oxide layer grown by MBD was $Al_{(2 \pm 0.1)}O_{(3.2 \pm 0.1)}$, very close to the expected 2:3 value for stoichiometric Al_2O_3.

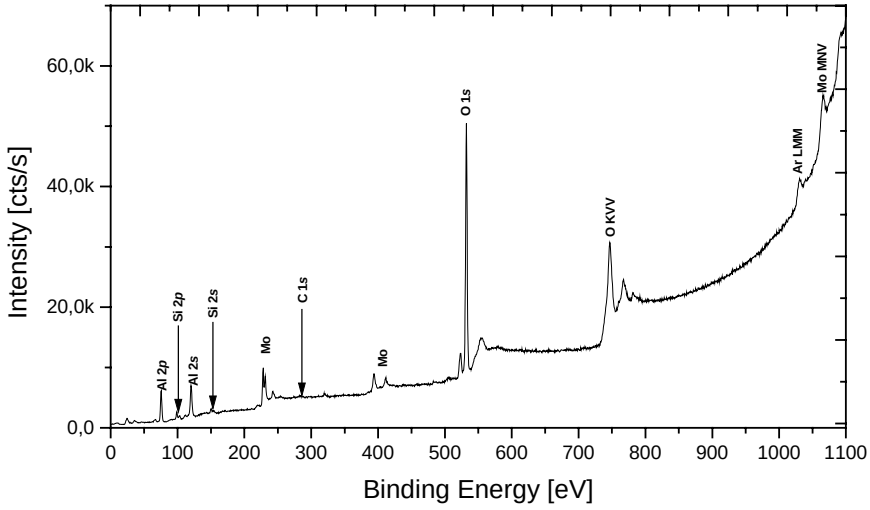


Figure 3.19 XPS depth profile analysis of a 7nm thick MBD Al2O3-layer after 12min sputtering (2nm depth).

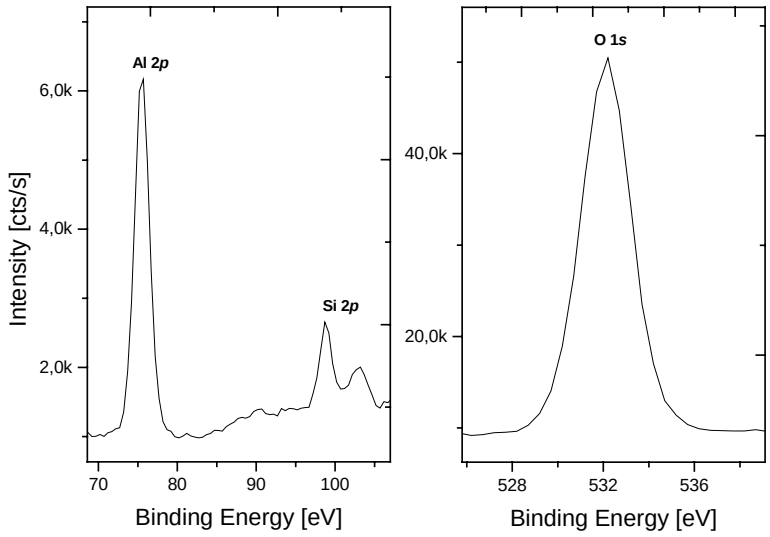


Figure 3.20 Al 2p, O 1s core-level spectra for MBD Al_2O_3 on Si(100) substrate

3.4.4 TEM

The quality of the MBD aluminium oxide films and the interface between the gate dielectric and silicon substrate were studied by cross section TEM (QS-TEM), High-Resolution TEM investigation done in collaboration with Infineon Technologies AG.

The TEM analysis show that the aluminium oxide grown in MBD system is amorphous and the silicon interface is smooth, with a thin interface oxide between the Al_2O_3 and the Si-substrate. The layer thickness was measured in different points and the results being in the range 3.3nm-3.6nm, very close to the expected value measured by ellipsometry.

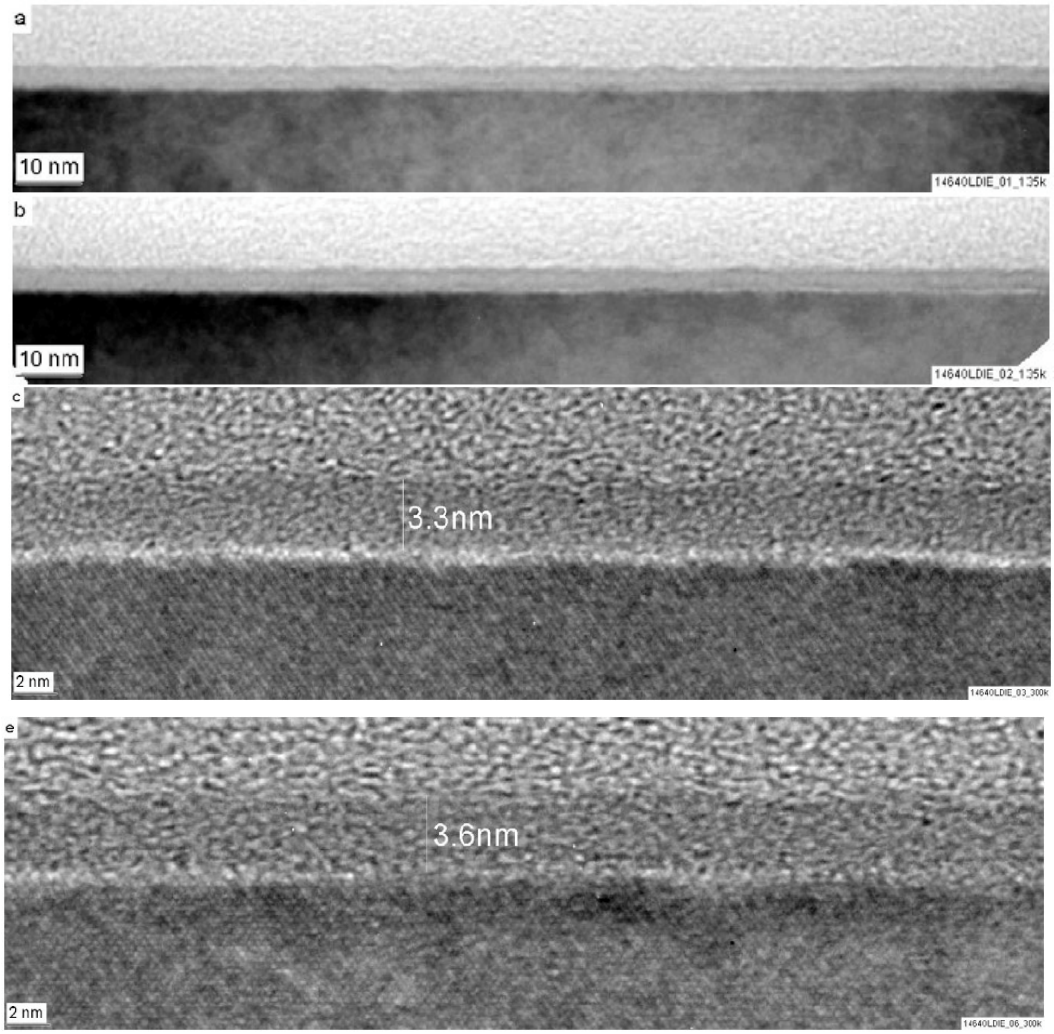


Figure 3.21 TEM analysis of Al_2O_3 MBD grown. 200kV QS-TEM. a) and b) wide view (10nm). Very smooth silicon interface. c), and e) particular. The measured thickness is in the range 3.3-3.6nm. The Al_2O_3 layer seems to be compact and amorphous. Any relevant thick silicon oxide between the Al_2O_3 and the Si-substrate can be observed.

3.5. Conclusion

Aluminium oxide thin films grown by MBD were studied in detail. The influence of the different parameters on the electrical properties of the UHV-grown Al_2O_3 layers have been analysed and the deposition was optimised.

Capacitance vs. voltage measurement highlights the formation of a thin interface oxide between Al_2O_3 film and silicon substrate which causes the reduction of the dielectric constant of the gate stack. The diminution of the ε value and the low stopping power against oxygen diffusion typical for aluminium oxide films lead to the conclusion that the interface oxide was given by SiO_x.

The composition of gate stack was studied by XPS analysis which reveals a nearly ideal stoichiometric $Al_{(2 \pm 0.1)}O_{(3.2 \pm 0.1)}$ film on a thin SiO_x interface layer.

J(V) and C(V) characterisation of $Al/Al_2O_3/Si$ capacitors confirm the good electrical properties of the processed gate oxide. In particular, the high quality of the interface was proved by the low interface state density extracted from G(V) measurements. The leakage current measured for V_G-V_{FB} = -1V was several orders of magnitude smaller than silicon oxide at the same equivalent oxide thickness and stays in the range of the best reported literature values.

Chapter 4

Interface Engineering

The optimisation of the interface between gate dielectric and the silicon substrate is a fundamental issue that has to be taken into account during the development of processes technologies for next device generation. Until today, thermally grown silicon dioxide (SiO_2) has been principally used as gate material. The principal advantage of this material is that it can be thermally grown from the silicon substrate. This growth process allows to obtain a burried interface between silicon substrate and SiO_2 which is very smooth and characterised by low state density D_{it}. Today, due to dimension shrinking, new gate dielectric have to be introduced for next device generation. Since the high-k material is tipically grown on silicon substrate by a deposition process (MBD, ALD, CVD, etc) the interface between dielectric and substrate plays a fundamental role: the surface roughness and imperfections influence the leakage current of the device and cause a high interface state densities D_{it}.

Experiments have been performed to study the surface roughness of Si(100) and Si(111) samples after native oxide removal process (thermal desorption) and after different heat treatment processes. In a first moment a series of combined Scanning Tunneling Microscopy (STM) and Auger Electron Spectroscopy (AES) studies have been done to investigate the substrate morphology. After that the influences of the different silicon surface treatments have been tested on MBD-Al_2O_3 sample. In both studies, a particular attention have been paid to carbon contamination present on the silicon substrate which can strongly damage the electrical performances of the devices.

This work was done in collaboration with T. Stimpel, UniBW-München. The effects of interface engineering in MOS capacitors with silicon nitride layers gate oxide were also investigated and the results reported in the PhD Thesis “Optimierung von Gate-Dielektrika für die MOS-Technologie” drew up by A. Ludsteck, UniBW-München.

4.1. Influence of heating time

Before to start any deposition process in UHV-system, typically the native oxide or the chemical oxide formed on the silicon wafer after cleaning process have to be removed from the Si-substrate. Native oxide removal on untreated silicon wafer and after RCA-cleaning have been studied. Figure 4.1a) shows the surface of an untreated Si sample after thermal desorption (T-D) of the native oxide layer at 900°C for 5 minutes. The measured roughness is several monolayers hight. No flat regions can be observed on the silicon surface in STM images. After heating the untreated silicon wafer in UHV for 15 minutes, large areas of the sample show an atomically flat surface (Figure 4.1b) and only some clusters can be seen, which can be several nanometers high. These clusters have to be attributed to remaining surface carbon contamination.

In the same way, the silicon oxide have been removed from Si-wafer cleaned with standard-RCA. The surface morphology after thermal desorption at 900°C for 5min is reported in fig. 4.1c). The surface roughness is in the same range as for untreated wafer (figure 4.1a). For RCA-cleaned sample heated at 900°C for 15min (fig. 4.1d), clusters as in figure 4.1b) are observed.

AES measurements performed on the silicon wafer after thermal desorption reveal in both cases a relevant amount of C on the Si-surface of the sample after temperature treatment, as shown in figure 4.2.

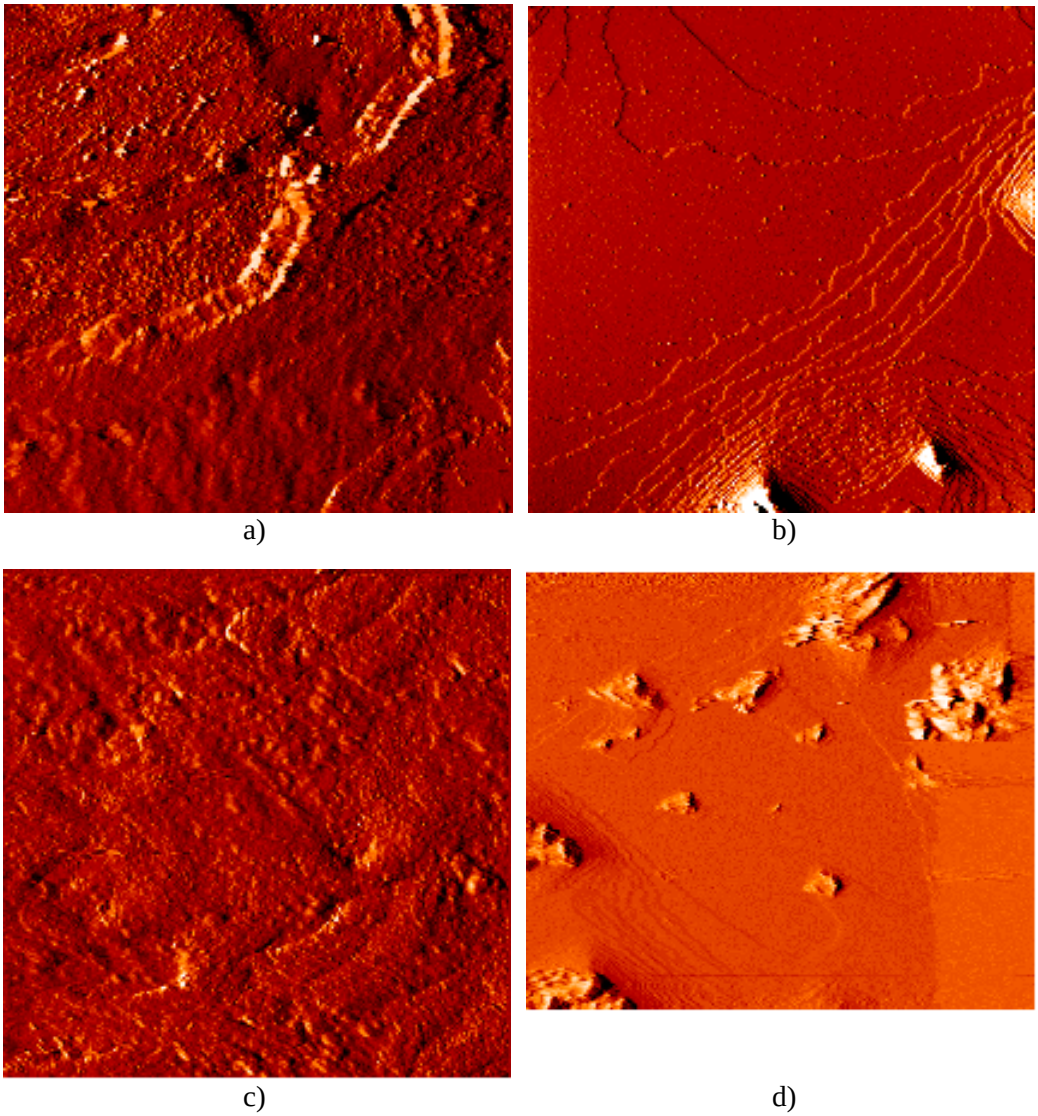


Figure 4.1 STM images of Si surface after thermal desorption of the native oxide layer of an untreated Si surface at: a) 900°C for 5 minutes (image size: 373×373nm^2); b) 900°C for 15 minutes (image size: 373×373nm^2) and of an standard-RCA cleaned Si surface at c) 900°C for 5 minutes (image size: 373×373nm^2) and d) 900°C for 15 minutes (image size: 373×310nm^2)

This first part of the experiments show that the thermal desorption of native- or chemical-oxide (T-D) on both untreated and RCA-cleaned samples produces a very rough

Si-surface for short processing time (900°C – 5min), while carbon clusters are formed if the heating time is prolonged (900°C - 15min). These C-clusters are a sure source of defects in case the silicon wafers treated with T-D are used to build electrical devices. As reported above, the C-cluster are some nanometers high, which can be more than the gate oxide thickness, producing short-circuits in the MOS-structure.

In the second part of the experiments, Si-samples were first prepared by heating treatment in UHV at 1200°C for 15 minutes. These process conditions are typically used to obtain atomically flat surface since all surface contaminants – mainly C – diffuse into the bulk Si. In this way, it is possible to avoid storage effects and eventually chemical-induced increase of surface roughness before oxide desorption.

After having prepared the Si-samples with atomically flat surface, they were exposed to air for 15 minutes, then transferred back into UHV and heated to 900°C for 5 minutes to remove the native oxide and surface contaminants accumulate during the exposition in air. Fig. 4.3a) shows a slightly reduced surface roughness compared to the experiments for the untreated and standard-RCA cleaned surfaces (figure 4.1a and 4.1c). However, the contaminants could not be completely removed, as can be observed by the presence of C-clusters after heating the sample to 900°C for 15 minutes (figure 4.3b).

Observing figure 4.1a), 4.1c) and 4.3b) it is possible to affirm that the C-cluster do not exhibit a crystalline structure. The remaining sample surface is atomically flat with an increased step density around the contaminant clusters. These steps are generated by the lattice mismatch between Si and a different material formed on top of the Si surface. In this case they indicate the formation of SiC on the Si surface, as could be shown in experiments on the SiC formation from C_{60} as a precursor [Stimpel03].

In their oxide desorption experiments, Gray et a. [Gray96] also found out that local peaks of C contamination appeared in AES measurements of the silicon surface. Thus it has to be concluded that the observed clusters consist of amorphous carbon with a probable formation of minor amounts of SiC at the Si-C-interface. Si(100) and (111) surfaces exhibit the same behaviour.

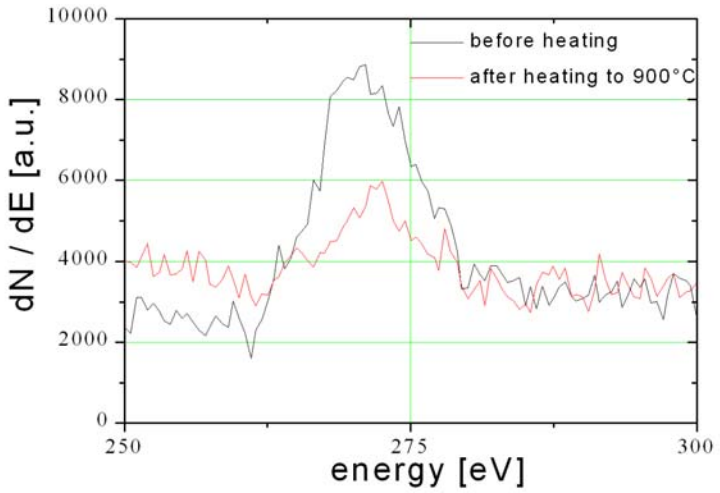
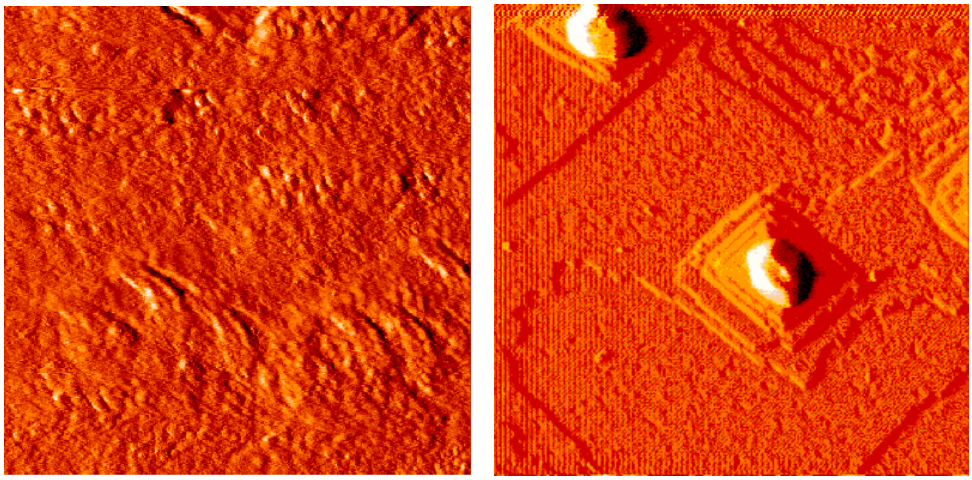


Figure 4.2 AES spectrum of the native oxide covered Si surface (black line) and of the sample surface after thermal desorption of the native oxide at 900°C for 5 minutes (red line). Carbon could not be removed completely by thermal desorption. C- Major AES line: KL1 263eV

The silicon surface preparation for microelectronic application requires to achieve a contaminant-free atomically smooth Si surface. For this reason it is necessary to remove the carbon contamination. It would be preferable to remove the contaminations as first and then desorb the native oxide, avoiding the C diffusing into the sample. Possible carbon removal by temperature treatment in oxygen ambient are investigated and the results reported in the next section of this chapter.



a) b)

Figure 4.3 STM images of Si surface after thermal smoothing at 1200°C, exposure to air for 15 minutes and subsequent thermal removal of contaminants at 900°C for a) 5 minutes (image size: 373×373nm^2) and b) 15 minutes (image size: 39×39nm^2).

4.2. Influence of $T_{Substrate}$ and oxygen pressure: C-burning

The possibility to remove the carbon contamination from the silicon wafer by temperature treatment in oxygen atmosphere is treated in this section. It is known that carbon reacts with silicon at 650°C to form SiC, which is very stable and cannot be eliminated from the silicon wafer. In order to eliminate the C-contamination without forming SiC, the silicon wafer are heated in oxygen ambient with substrate temperature ($T_{Substrate}$) lower than 650°C, but high enough to activate the reaction between carbon and oxygen. As such carbon will desorbts from the silicon surface as CO and CO_2. During the carbon-removal (C-burning) a thin silicon dioxide layer forms on the silicon surface.

Finally, the efficiency of C-burning process and the subsequent removal of the silicon dioxide formed during the cleaning process are verified by AES investigations and electrical characterisation of $Al/Al_2O_3/Si$ capacitors .

4.2.1 AES analysis on the efficiency of C-burning

The efficiency of the carbon removal process from silicon wafers has been studied. Si(100) wafers were cleaned with standard RCA. After cleaning, Si-samples were loaded in UHV and heated at different substrate temperature ($T_{Substrate}$=500°C – 550°C – 600°C) in oxygen atmosphere ($p_{O2}=1\cdot10^{-5}$mbar) for 30min. High $T_{Substrate}$ are necessary to activate the reaction between oxygen and carbon but they have to lower than 650°C in order to avoid the formation of SiC.

Auger analysis have been performed after RCA-cleaning and after thermal treatment to investigate the effect of the C-burning process on the silicon substrate.

The auger spectrum of silicon samples measured directly after RCA cleaning is reported in figure 4.4. The location of peaks illustrates the presence of oxygen (E_O=505eV) and carbon (E_C=263eV) on the silicon surface.

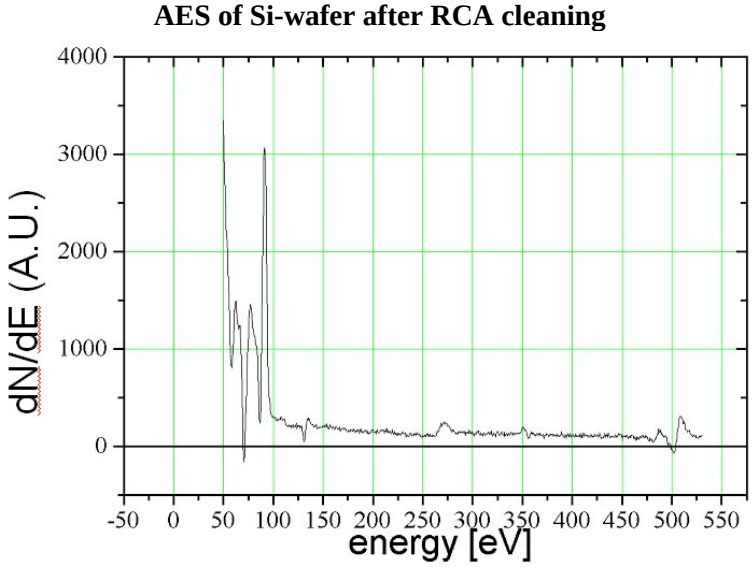


Figure 4.4 AES spectrum of silicon sample after RCA cleaning. Oxygen and carbon can be identified by evident peaks in the characteristics energy regions.
O- Major AES line: KL1 505eV; C- Major AES line: KL1 263eV [Surface]

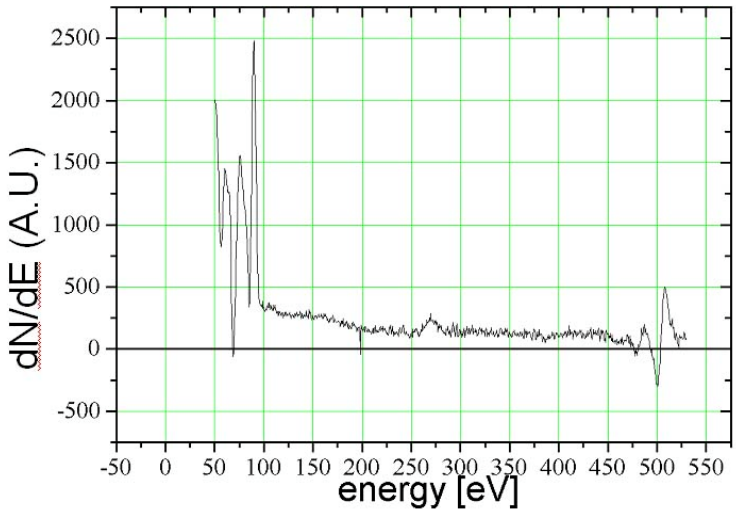


Figure 4.5 AES spectrum of silicon sample after C-burning. $T_{Substrate}$=500°C, p_{O2}=1·10^{-5}mbar, t=30min. Oxygen and carbon can be identified: O- Major AES line: KL1 505eV; C- Major AES line: KL1 263eV [Surface]
The higher oxygen peak compared to fig. 4.4 indicate a thicker SiO_2 layer, that can be eliminate by thermal desorption in UHV ($T_{Substrate}$=900°C, t=5min)

4.2.1.1. C-Burning: $T_{Substrate}$=500°C; p_{O2}=1·10^{-5}mbar, t=30min

RCA-cleaned silicon samples were loaded in UHV-system and heated to a substrate temperature $T_{Substrate}$=500°C in oxygen ambient (p_{O2}=1·10^{-5}mbar) for 30min.

The AES investigations after temperature treatment are reported in figure 4.5. These analysis shows that carbon contamination cannot be eliminated from the silicon surface by heating the sample at the condition indicated above, since an high peak in the characteristic C-energy region can still be evidenced after C-burning.

During heating, a thin silicon oxide layer is formed on the silicon substrate. This layer is evidenced by comparing the oxygen peaks of figure 4.4 and figure 4.5 and noting that after C-burning at $T_{Substrate}$=500°C, the height of the oxygen peak increases (fig. 4.5). Further investigations (not reported) have shown that this SiO_2 layer can be eliminated submitting the sample to a subsequent thermal desorption process (900°C, 5min), as indicated in paragraph 4.1. Based on this results the desorption process was performed for the subsequent samples as well.

4.2.1.2. C-Burning: $T_{Substrate}$=550°C; p_{O2}=1·10^{-5}mbar, t=30min

The investigations on the efficiency of the C-burning process have been repeated for higher substrate temperature. In figure 4.6, the AES analysis results for silicon samples submitted to temperature treatment in UHV with $T_{Substrate}$=550°C (p_{O2}=1·10^{-5}mbar; t=30min) are reported.

It can be clearly seen that no more carbon peaks are present in the AES spectrum for samples which have seen C-burning at $T_{Substrate}$=550°. A zoom-view of the region where the carbon peak should be found is illustrated in figure 4.6b. The AES analysis reported in fig. 4.6a (wide view) was carried out after thermal desorption (900°C, 5min) and confirms that the thermal SiO_2 formed during C-burning can be eliminated by this treatment.

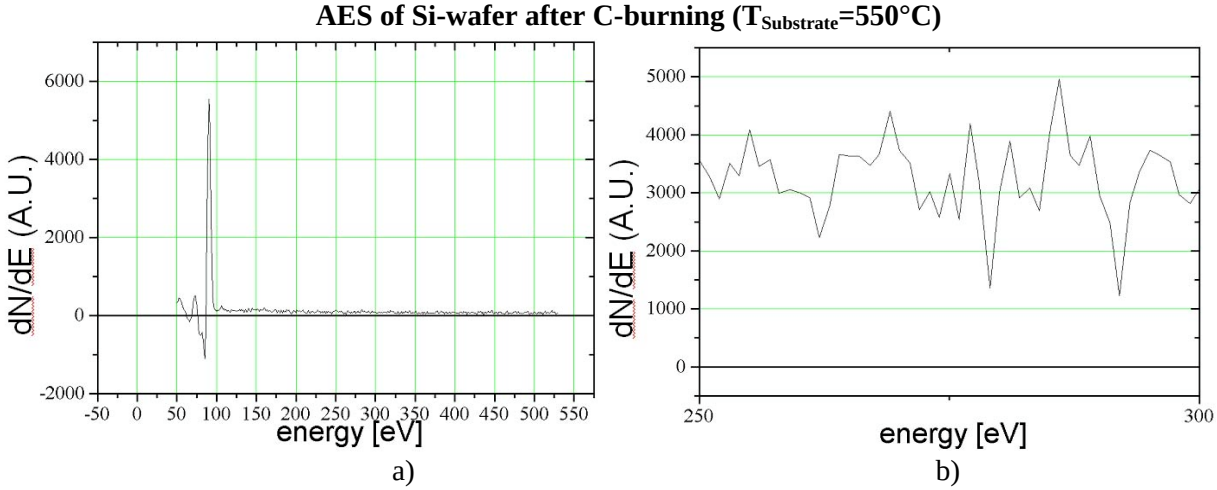


Figure 4.6 AES spectrum of silicon sample after C-burning. $T_{Substrate}$=550°C, p_{O2}=1·10^{-5}mbar, t=30min. a) wide view, after thermal desorption ($T_{Substrate}$=900°C, t=5min); b) zoom of the region where the carbon peak should be found. No oxygen or carbon peaks are evident. O- Major AES line: KL1 505eV; C- Major AES line: KL1 263eV [Surface]

4.2.1.3. C-Burning: $T_{Substrate}$=600°C; p_{O2}=1·10^{-5}mbar, t=30min

Performing the temperature treatment with $T_{Substrate}$ of 600°C leads to the elimination of the carbon contamination from the silicon wafer, as can be seen from the absence of C-peak in figure 4.7b. However, the AES analysis show that oxygen is still present on the silicon wafer. This is due to the fact that the higher process temperature leads to the formation of a thicker silicon oxide which cannot be removed using the standard thermal desorption process.

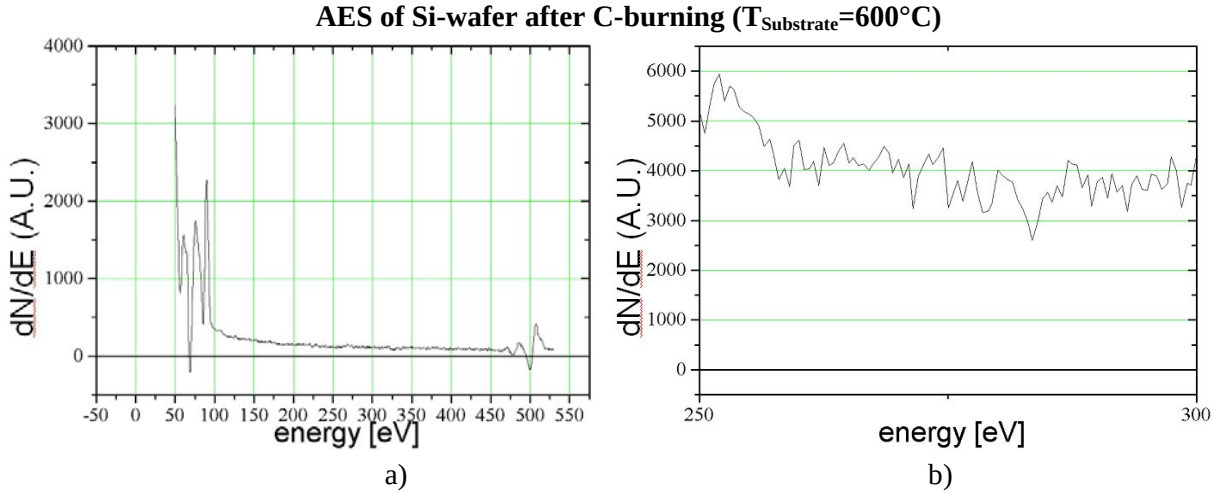


Figure 4.7 AES spectrum of silicon sample after C-burning. $T_{Substrate}$=600°C, p_{O2}=1·10^{-5}mbar, t=30min. a) wide view, after thermal desorption ($T_{Substrate}$=900°C, t=5min): oxygen peak is still present; b) zoom C region. The carbon contamination can be eliminated from the silicon surface, but SiO_2 layer formed during treatment cannot be desorbt. O- Major AES line: KL1 505eV; C- Major AES line: KL1 263eV [Surface]

4.2.2 Electrical Investigation on the efficiency of C-burning

The efficiency of the carbon removal have been tested by measuring the electrical characteristics of MOS capacitors grown on silicon wafers treated with C-burning before the deposition of the gate oxide. Al_2O_3 was used as gate oxide for these investigations.

STM and AES investigations reported in this chapter have indicated that carbon removal from the silicon substrate is possible by heating the wafer in oxygen atmosphere. This process will produce a thin SiO_2 layer that can be eliminated by thermal desorption (TD). After standard TD (T=900°C, t=5min) the silicon surface will become rough, as illustrated in figure 4.3a, and this roughness will decreases the electrical performances of the MOS capacitors. For this reason, thermal desorption was omitted during the processing of the MOS capacitors investigated in this section.

In order to have an interface oxide as thin as possible, the silicon wafers prepared with and RCA-cleaning and HF-last to remove the chemical oxide. Afterward they were immediately loaded in UHV and C-burning process was done. Ellipsometer measurement effectuated on silicon wafers after C-burning (UHV, $T_{Substrate}$=550°C; p_{O2}=1·10^{-5}mbar; t=30min) determinates a silicon dioxide thickness formed during thermal process of around 0.2-0.5nm.

Following the indication furnished by the AES analysis (4.2.1), the substrate temperature for the C-burning process was fixed to 550°C and the heating time to t=30min. The oxygen pressure during carbon removal was optimised for the UHV system used for Al_2O_3 deposition. Al_2O_3 thin films were grown on Si(100) wafers. The important information concerning the samples preparation are summarised in table 4-1 and the current density vs. voltage measurements for $Al/Al_2O_3/Si(100)$ capacitors are reported in figure 4.8. The lowest leakage current was measured for a C-burning process with an oxygen pressure $p_{O2}=1\cdot10^{-5}$mbar.

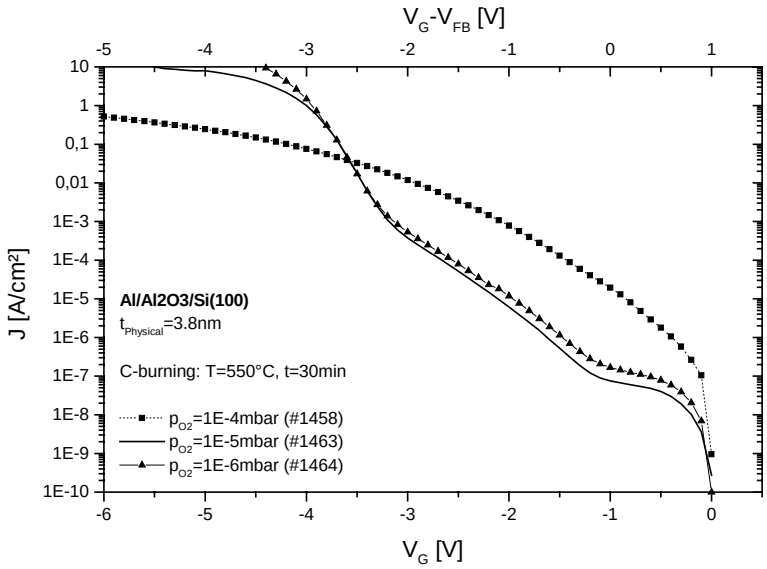
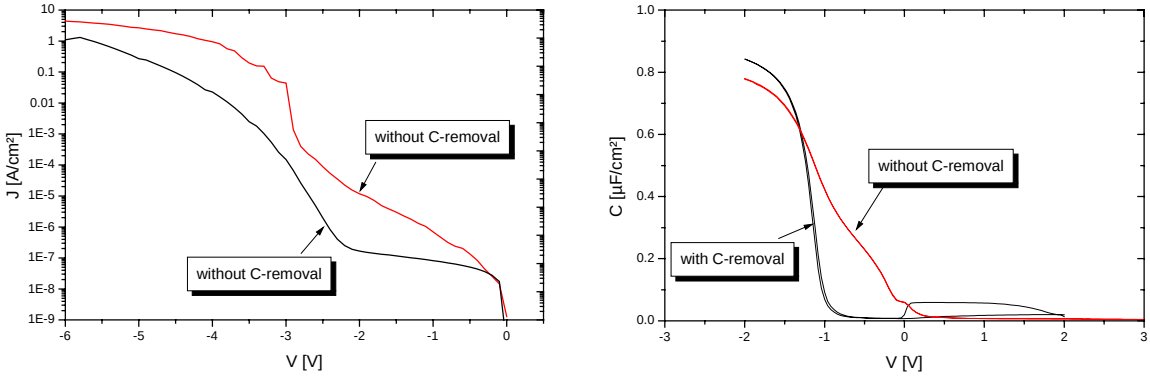


Figure 4.8 J(V) measurements for $Al/Al_2O_3/Si(100)$ capacitors with 3.8nm thick gate oxide. The Al_2O_3 films were deposited under the same process conditions, only the C-burning changed.



a) b)

Figure 4.9 J(V) and C(V) characteristics for samples prepared with and without C-burning (T=550°C, $p_{O2}=1\cdot10^{-5}$mbar; t=30min)

Table 4-1 Process parameters for C-burning and Al_2O_3 deposition

Wafer Cleaning	RCA + HF-last
C-burning T=550°C – t =30min	#1558: $p_{O2}=1\cdot10^{-4}$mbar #1563: $p_{O2}=1\cdot10^{-5}$mbar #1564: $p_{O2}=1\cdot10^{-6}$mbar
MBD Deposition	$T_{Substrate}$=500°C $p_{O2}=1\cdot10^{-4}$mbar
Furnace Annealing	Nitrogen T=600°C t=30min

The improvement of the electrical characteristics of MOS capacitors which have seen C-burning compared with samples grown without carbon removal process can be observed in the current density vs. voltage J(V) and capacitance vs. voltage C(V) characteristics illustrated in figure 4.9. The introduction of a C-burning step before high-k deposition reduces the leakage current of the MOS capacitors. Additionally a strong improvement of the C(V) shape is achieved which indicated lower defect density at the interface between gate dielectric and silicon substrate.

4.2.3 C-burning in UHV system: summary

In this chapter the influences of temperature and oxygen pressure in UHV-system during silicon surface preparation have been investigated. It was found that the carbon contamination present on the silicon substrate after RCA-cleaning can be efficiently removed by C-burning process. In this way, a thin silicon oxide layer is formed on the silicon surface, which can be removed by thermal desorption (900°C, 5min) or used as interface as high-k and silicon substrate.

The process parameters for carbon removal have been optimised for the different UHV-system used for aluminium- and lanthanum oxide deposition and are indicated in table 4-2.

Table 4-2 C-burning process parameters optimised for UHV-systems

UHV - System	**Process Parameters**
Al_2O_3 – old UHV system	T=550°C $p_{O2}=1\cdot10^{-5}$mbar t=30min
La_2O_3 – new UHV system	T=550°C $p_{O2}=7\cdot10^{-6}$mbar t=30min

Chapter 5

Deposition process optimisation and characterisation of thin Pr_2O_3 films grown by means of MBD

Purpose of this chapter is to develop a fabrication method for the molecular beam deposition of praseodymium oxide thin films and study their electrical and physical characteristics.

Praseodymium oxide thin films were grown on silicon Si(100) substrate by MBD. The stoichiometry and morphology of the Pr_2O_3 grown with the developed process were studied by AES, XPS and TEM and the electrical properties investigated by current-voltage and capacitance-voltage characterisation.

This chapter is divided into five section. In the first section (Section 5.1) the physical properties of Pr_2O_3 system are described.

The second section (Section 5.2) explains the parameters which have an influence on the Pr_2O_3 deposition in UHV-system (temperature, oxygen partial pressure, source material).

Section 5.3 investigates in detail the effects introduced in section 5.2 using current density vs. voltage J(V) and capacitance vs. voltage measurements C(V) of Al/Pr_2O_3/Si capacitors.

The physical characterisation of the Pr_2O_3 films grown by MBD is treated in section 5.4, while the development of an interface passivation before Pr_2O_3 deposition is the content of section 5.5.

5.1 Physical properties of Pr_2O_3

Praseodymium oxide is a rare-earth-metal oxide that has not been largely used for application in microelectronic so far. In recent years, rare earth metals and particularly Pr_2O_3 have been vigorously studied as alternative gate dielectric in CMOS applications. The interest on praseodymium oxide as alternative gate dielectric is due to its high dielectric constant (around 30 for bulk material).

Pr_2O_3 grown on silicon typically behaves as a stable system [Hubba96]. This results cannot be confirmed by thermo-dynamical calculation while thermodynamic data for $PrSi_2$ and Pr_2SiO_5 are missing. However, experimental results [Tarsa] of epitaxial Pr_2O_3 grown on silicon show no evidence of reaction at the Pr_2O_3/Si interface.

Praseodymium oxide is a very reactive material: at room temperature, Pr_2O_3 keeps bixbyte type lattice structure of cubic (figure 5.1a); at high room temperature and low pressure, Pr_2O_3 has a monoclinic type lattice structure (figure 5.1b). In oxidising ambient, it becomes PrO_2 of fluorite type structure.

An extensive study of the behaviour of praseodymium in oxygen ambient can be found in [Hide66] and [Burnham68]. Praseodymium oxide and oxygen phase diagram is reported in figure 5.2. The temperature-composition projection of the PrO_x-O_2 phase diagram shows the existence of several ordered intermediate phases of narrow composition belonging to an homologous series, Pr_nO_{2n-2} and at higher temperatures two immiscible phases (α, σ) covering nearly the entire composition range of PrO_x, $1.5 \leq x \leq 2$ [Burnham68].

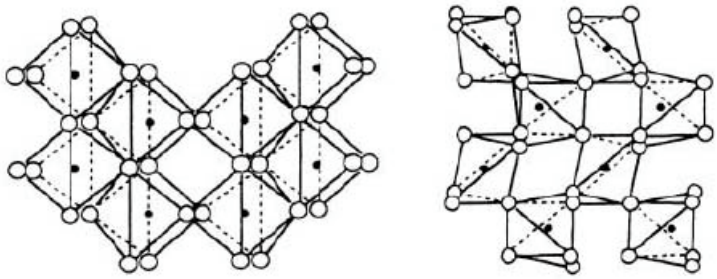


Figure 5.1 (a) A-type lattice structure (b) C-type lattice structure

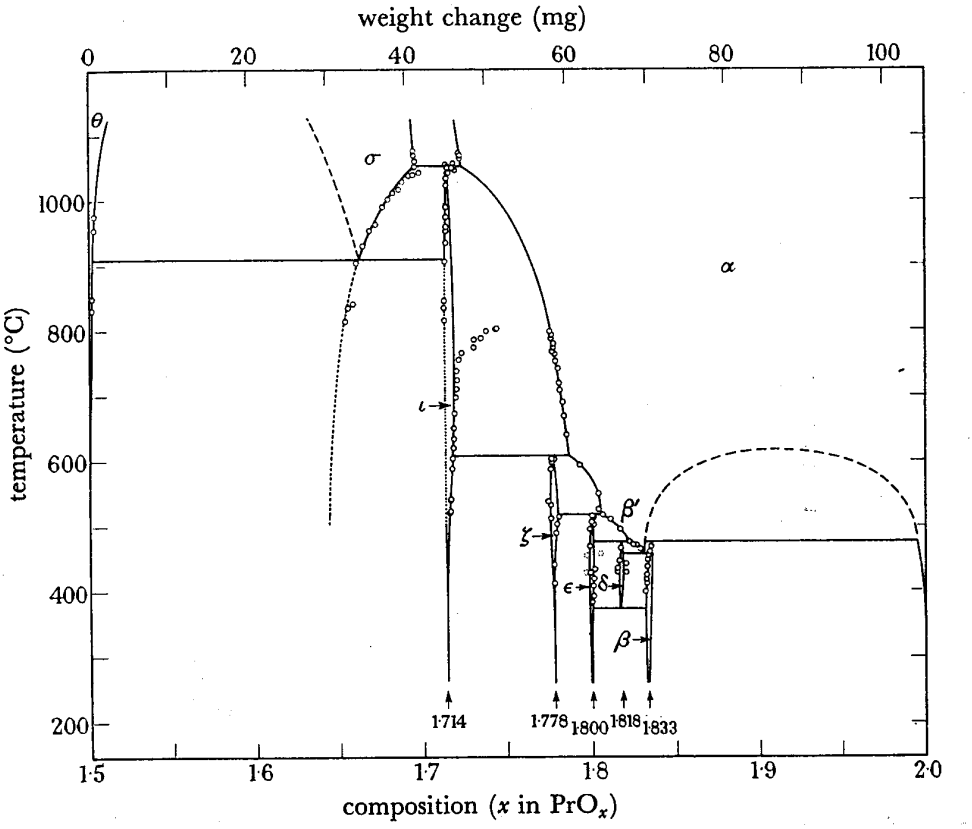


Figure 5.2 Projection of the praseodymium oxide + oxygen phase diagram on the temperature-composition plane. ○: experimental points for the isobars; dashed lines indicate assumed extension. After [Hyde66]

One of the first work in which praseodymium oxide was used as gate dielectric was published by H.J. Osten et al [Osten00]. In this report, ultra thin praseodymium oxide films were made by MBE on silicon substrate and excellent data was reported:

- this Pr_2O_3 films on Si(100) have a dielectric constant of around 30, independent of substrate doping type
- films with EOT of 1.4nm have leakage current densities below 10^{-8}A/cm² at V_G=-1V.
- Pr_2O_3 exhibited symmetrical band offset larger 1eV to Si. The fundamental band gap is between 3 and 4eV.

Further investigations and reports indicate Pr_2O_3 as a very promising material for gate oxide applications. Unfortunately, praseodymium oxide is not stable against air [Osten]. Oxygen diffusion through the oxide (even at room temperature) leads to the formation of interfacial SiO_x layers which causes structural and electrical degradation and significant structural changes take place after the samples have been exposed to air at room temperature [Zaum01].

5.2 Process optimisation and thermal stability of MBD-grown Pr_2O_3 thin films

Praseodymium oxide thin films were grown on silicon substrate by MBD. The UHV-deposition process has been optimised by studying the influence of substrate temperature, oxygen partial pressure and source material introduced in the evaporation system. Moreover, the behaviour of the Pr_2O_3 films during post-growth annealing has been investigated.

5.2.1. Influence of substrate temperature

The high reactivity of praseodymium oxide even for low temperature makes the molecular beam deposition of amorphous Pr_2O_3 layer very critical. Epitaxial growth of crystalline Pr_2O_3 layer has been starkly investigated [Osten]. However, this procedure cannot guarantee the reproducibility of the results since mono-crystalline films are difficult to be grown and mostly the MBE-grown Pr_2O_3 will be polycrystalline.
For this reason, deposition of amorphous films is investigated in this thesis. The possibility to deposit Pr_2O_3 amorphous layers in UHV-system is investigated growing the rare earth oxide with substrate temperature ($T_{Substrate}$) in the range 400-700°C.
As well room temperature deposition and $T_{Substrate}$=800°C experiments have been performed and praseodymium oxide films grown under these conditions had very high leakage currents.

The process conditions, thickness and substrate temperature used to study the influence of the substrate temperature during Pr_2O_3 deposition are indicated in Table 5-1.
From the current density vs. voltage J(V) characteristics it can be concluded that the lowest leakage current is evidenced for praseodymium oxide films grown with a substrate temperature of 600°C (Subsection 5.3.1.1, figure 5.3).

Table 5-1 Influence of substrate temperature during Pr_2O_3 deposition process. The process parameters are summarised. No external oxidation source.

Wafer no.	Thermal Desorption	$T_{substrate}$ [°C]	$t_{Physical}$ [nm]	$J_{Leakage}$ @ -1V [A/cm²]	ε
13052/11	Y	700	27	$2\cdot10^{-8}$	22
13052/10	Y	600	27	$1\cdot10^{-8}$	26
01072/02	Y	400	16	$3\cdot10^{-7}$	17
01072/03	Y	600	16	$3\cdot10^{-8}$	17
15072/05	Y	600	90	$3\cdot10^{-9}$	23
15072/06	Y	500	90	$1\cdot10^{-8}$	21

5.2.2. Influence of oxygen partial pressure

The experiments here illustrated show that stoichiometry and physical properties of praseodymium oxide are strongly influenced by the oxygen partial pressure during the deposition process. Moreover, the extreme simplicity with which the oxygen can be transferred between solid PrO_x and the gas phase, even at temperature as low as 400°C, makes the process control and samples preparation very difficult, as also pointed out by [Hide66]. The influence of oxygen partial pressure has been studied taking in consideration the electrical properties of the Pr_2O_3 deposited layers. The process parameters are summarised in Table 5-2.

Analysing the electrical characteristics measured for praseodymium oxide grown with different oxygen pressure (Section 5.3) no big differences can be observed in J(V) measurements (Subsection 5.3.1.2, figure 5.4). C(V) shows that oxygen ambient during Pr_2O_3 growth reduce the dielectric constant of the deposited layer as can be seen from the dielectric constant value reported in table 5-2.

Table 5-2 Influence of oxygen pressure during Pr_2O_3 deposition process. The process parameters are summarised.

Wafer no. Oldie no.	**Thermal Desorption**	**$T_{substrate}$** [°C]	**Thickness (ellipsometer)** [nm]	**Oxygen pressure** [mbar]	**ε**
20082/03	Y	600	20	No additional O_2 ($p=1\cdot10^{-7}$mbar)	18
20082/04	Y	600	20	$1\cdot10^{-6}$	16
20082/05	Y	600	20	$1\cdot10^{-5}$	17
20082/06	Y	600	20	$1\cdot10^{-4}$	11

5.2.3. Source material

Praseodymium oxide is a very difficult material to be used for electron beam evaporation. Before to be evaporated it has to be preconditioned with low power sweep until spitting and outgassing. Commercially available Pr_6O_{11} and Pr_2O_3 powder have been used as source material for praseodymium oxide deposition.
Pr_6O_{11} is the most used source reported in literature [Osten, Lui01]. It is know that Pr_6O_{11} changes to a composition with less oxygen when treated at temperature higher than 480°C [wolf04] which is typically reached during the target outgassig. To avoid this composition modification and reduce the outgassing time Pr_2O_3 powder was additionally evaluated as possible ESV-source material.

C(V) investigation show evidence of a doping of the silicon substrate when praseodymium oxide films were grown from Pr_2O_3 99.9% (subsection 5.3.2.3, figure 5.11). Spectroscopic analysis effectuated on Pr_2O_3 powder 99.9% revealed the presence of 0.02% of boron inside the source material. The complete list of impurities detected in Pr_2O_3 99.9% is reported in table 5-3.

Table 5-3 Impurity concentration Pr_2O_3: Spectrographic Analysis

Element	**Results(%)**
Boron	0.02
Calcium	0.01
Copper	<0.01
Magnesium	<0.01
Silicon	0.02

5.2.4. Influence of the annealing ambient and temperature

The thermal stability and the influence of the annealing ambient on praseodymium oxide thin films have been studied by ex-situ temperature treatment of MBD-grown Pr_2O_3 films in nitrogen and oxygen ambient.

Capacitance vs. voltage C(V) measurements show that MBD-grown praseodymium oxide samples furnace annealed in oxygen ambient (600°C for 30min) have lower dielectric constant ε if compared with samples which have been annealed in nitrogen ambient (subsection 5.3.2.3, figure 5.12). This results is explained by taking into consideration the high oxygen diffusion which is a characteristic of the rare earth oxides: during annealing oxygen atoms diffuse through the praseodymium oxide, they reach the silicon substrate and start to form an interface SiO_x layer [Wolfo4, Gory02, Zaum01].

The thermal stability of Pr_2O_3 films on Si(100) have been studied by Goryachko et al.[Gory03]. They observed that the thickness of the deposited films increased after annealing. The cause of thickening was not the increase of praseodymium in the sample but a structural change of the film material. Starting from annealing at 700°C, evidence of silicon diffusion can be seen in the Pr_2O_3 film; this silicon accumulate at the surface where it reacts with oxygen available from the residual atmosphere and form SiO_2. Due to this outdiffusion from the substrate, the pure Pr_2O_3 is transformed into Pr_2O_3-Pr_x-O_y-Si_z mixture. Decomposition of praseodymium oxide and desorption of SiO_x starting from 700°C was also observed by Müssig et al [Mussig02].

Research on post-growth annealing shows the critical behaviour of Pr_2O_3 gate oxide. High annealing temperature are necessary to eliminate the hysteresis from C(V) measurements. Unfortunately, the electrical characterisation has shown that Pr_2O_3 samples which have good capacitance characteristic reveal high leakage currents in J(V) measurements. A most probable explanation for this behaviour is a change in morphology and a possible crystallisation of the praseodymium oxide layer, as also highlighted by [Liu01].

5.3 Electrical characterisation

This section treats with the electrical characterisation of praseodymium oxide films grown by MBD. Pr_2O_3 properties and the influence of the different deposition parameters (paragraph 5.2) are investigated by means of current density vs. voltage J(V) and capacitance vs. voltage C(V) characteristics of Al/Pr_2O_3/Si(100) capacitors. A detailed description of the measurement set-up and measurement conditions are reported in chapter 2 (2.2.1 and 2.2.2).

5.3.1. Current Density vs. Voltage (J-V) Measurements

Current density vs. voltage measurements for Al/Pr_2O_3/Si(100) capacitors have been used to study the influence of temperature and oxygen pressure during deposition process. Furthermore, the conduction mechanism in Pr_2O_3 films has been considered.

5.3.1.1. Influence of substrate temperature on J(V)

The influence of the substrate temperature during deposition process of Pr_2O_3 films has been investigated in the range of room temperature (RT) and 800°C.
For $T_{Substrate}$=RT and $T_{Substrate}$=800°C, very high leakage currents where evidenced (J(V) curves not reported). Detailed investigation for substrate temperature in the range 400°C-

700°C have been performed and the J(V) characteristics are illustrated in figure 5.3 (process data reported in Table 5-1).

The J(V) investigation shows that Pr_2O_3 films grown for low substrate temperature ($T_{Substrate}$=400°C, cross symbols in figure 5.3) have high leakage currents when compared with samples grown at higher temperature. The lowest leakage currents has been measured for Pr_2O_3 samples grown with substrate temperature of 600°C. For $T_{Substrate}$ in the range of 700°C the leakage current increases again due to a beginning of crystallisation of the Pr_2O_3 layer.

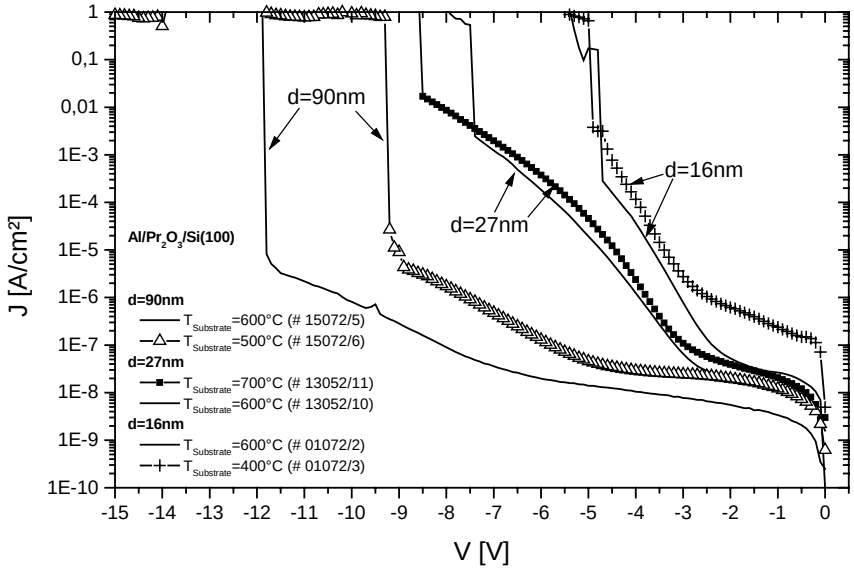


Figure 5.3 J(V) characteristics for Al/Pr_2O_3/Si(100) capacitors with different gate oxide thicknesses. Pr_2O_3 grown by MBD with different substrate temperatures.

5.3.1.2. Influence of the Oxygen Pressure on J(V)

Praseodymium oxide samples having the same physical thickness (20nm) have been grown in UHV under different oxygen partial pressure. The process parameters are reported in table 5.2 and the J(V) characteristics in figure 5.4.

Pr_2O_3 films grown without additional oxygen ($p_{process}=1\cdot10^{-7}$mbar) are characterised by low leakage current and a breakdown field of 4MV/cm (straight line, figure 5.4). Increasing the oxygen pressure to $p_{O2}=1\cdot10^{-6}$mbar, the breakdown voltage (V_{BD}) and the leakage current for low voltages decrease (square symbols, figure 5.4). A further increase of oxygen pressure ($p_{O2}=1\cdot10^{-5}$ – $1\cdot10^{-4}$mbar, pyramids symbols in fig. 5.2) improves the V_{BD} but increases the leakage current of the Pr_2O_3 films.

5.3.1.3. Influence of the Annealing Temperature on J(V)

The influence of the annealing temperature on praseodymium oxide films grown by MBD has been investigated. All MBD-grown Pr_2O_3 films have been annealed ex-situ in furnace with a maximal annealing temperature of 600°C, as exposed for Al_2O_3 (Chapter 3 – section 3.3.2.2). Pr_2O_3 samples were annealed in nitrogen ambient for 30min at 500°C and 600°C. The J(V) measurements are reported in figure 5.5: praseodymium oxide samples annealed in nitrogen at 600°C drastically change the J(V) shape and show high

leakage currents for voltages higher than 1.5V (square symbols, figure 5.5). This is due to a change of the morphology in the praseodymium oxide film and to a beginning of crystallisation, which produced preferential path for the leakage current.
Annealing in nitrogen at 500°C slightly increases the leakage current of the deposited layer compared to as-grown samples. Anyway, the J(V) characteristic maintains the expected behaviour with a knee around 3V and a breakdown field of 6MV/cm.

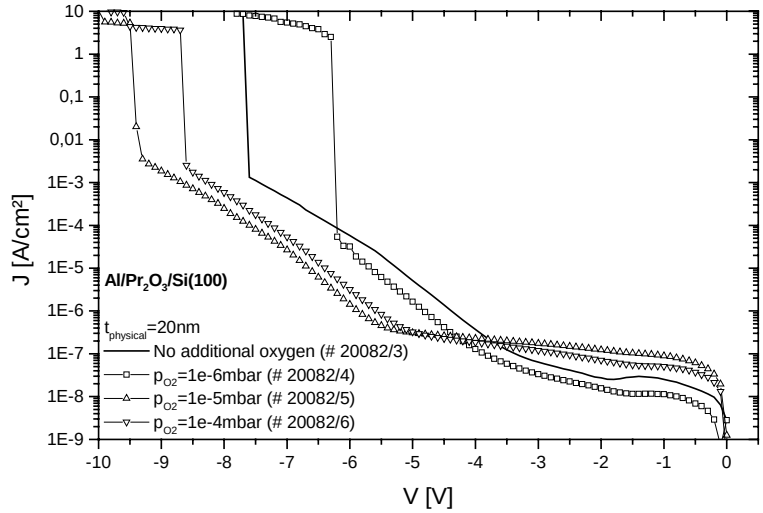


Figure 5.4 J(V) characteristics for 20nm thick Pr_2O_3 gate oxide on Si(100). The samples were grown under different oxygen partial pressure.

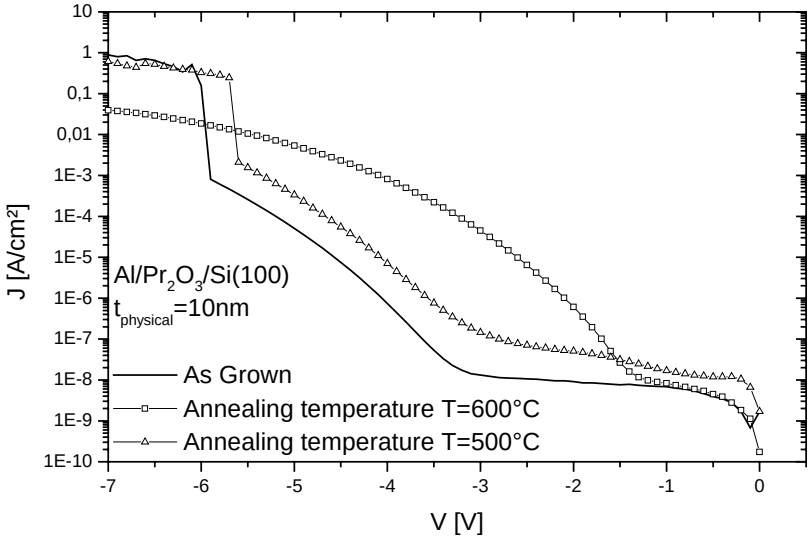


Figure 5.5 J-V measurement for capacitors having 10nm Pr_2O_3 gate oxide, grown under the same process conditions. Straight line: as grown; square symbol: annealed in N_2, at 600°C for 30min; triangle: annealed in N_2, at 500°C for 30min.

5.3.1.4. Temperature dependent J(V) measurements on Al/Pr_2O_3/Si(100) structures

The conduction mechanism of praseodymium oxide films was studied by measuring J(V) characteristics at different temperatures. The back-side of the wafer was placed on a hot-chuck plate and current density vs. voltage characteristics were measured for a temperature range going from room temperature (RT) to 220°C in ambient atmosphere. The J(V) characteristics are reported in Fig. 5.6 for as grown and in Fig. 5.7 for annealed samples.

This investigation was done in collaboration with O. Blank, Infineon Technologies AG. The important results measured for Al/Pr_2O_3/Si(100) capacitors are reported in this section.

J(V) temperature-characteristics for as-grown Pr_2O_3

J(V) characteristics for different measuring-temperature of Pr_2O_3 as-grown films are shown in figure 5.6. All the measurements were performed in ambient atmosphere. The current density increase by increasing the hot-plate temperature during J(V) measurements. Repeating the room temperature measurement on the same sample after one temperature-cycle, no substantial differences were shown with the first run. This result suggests that the increasing temperature only effects the conductivity behaviour but does not alter the properties of the gate insulator.

J(V) temperature-characteristics for annealed Pr_2O_3 (N_2, 600°C, 30min)

Additional investigation was done on furnace annealed samples (nitrogen, 600°C, 30min). Current density vs. voltage measurements show important modifications on the conduction mechanism depending on the measuring-temperature. In figure 5.7, two measurement runs are reported: in the first run, the J(V) characteristics of Al/Pr_2O_3/p-Si capacitors have been measured for measuring-temperature increasing from room temperature to 225°C. In the run, the hot-chuck temperature was decreased (from 225°C to room temperature) and the J(V) characteristics where measured again:

a) 1^{st} measurement cycle: hot-chuck temperature increased from 25°C to 225°C
b) 2^{nd} measurement cycle: hot-chuck temperature decreased from 225°C to 25°C

Observing the J(V) curves it can be noticed that increasing the temperature of the hot-chuck from 25°C to 125°C, the current density J(V) increases too. When $T_{hot\text{-}chuck}$ reachs 225°C the current density measured for the capacitor becomes lower and the J(V) characteristics modifies his shape (figure 5.7a).

Performing a second cycle of measurements with decreasing $T_{hot\text{-}chuck}$ (Fig. 5.7b), the leakage current of the Pr_2O_3 annealed sample decreases some orders of magnitude and finally reaches a value far below the first J(V) measurements for $T_{hot\text{-}chuck}$ =25°C (straight line, figure 5.7a compared with straight line, figure 5.7b - factor 10^{-5} @-5V). The stability of the system was checked by repeating the room temperature measurements after one week. No evidence of difference between the two measurement was observed (straight line, figure 5.7b compared with circle symbol, figure 5.7b).

The electrical behaviour shown from the J(V) characteristics clearly indicates that for temperature higher than 200°C the praseodymium oxide furnace annealed change his chemical nature. The new Pr_2O_3 structure is stable at room temperature, as confirmed by the measurement repeated after one week.

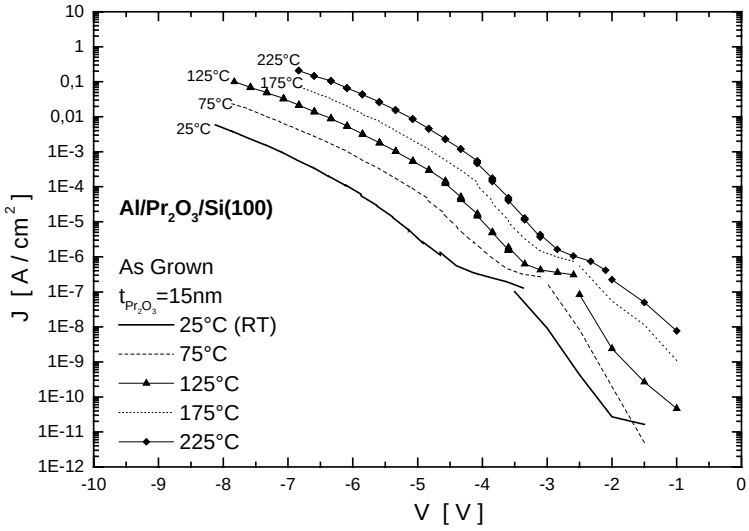


Figure 5.6 J(V) measurement for Al/Pr_2O_3/Si(100) capacitor with 15nm Pr_2O_3 gate oxide. As Grown sample. Hot-chuck temperatures from 25°C to 225°C in steps of 50°C.

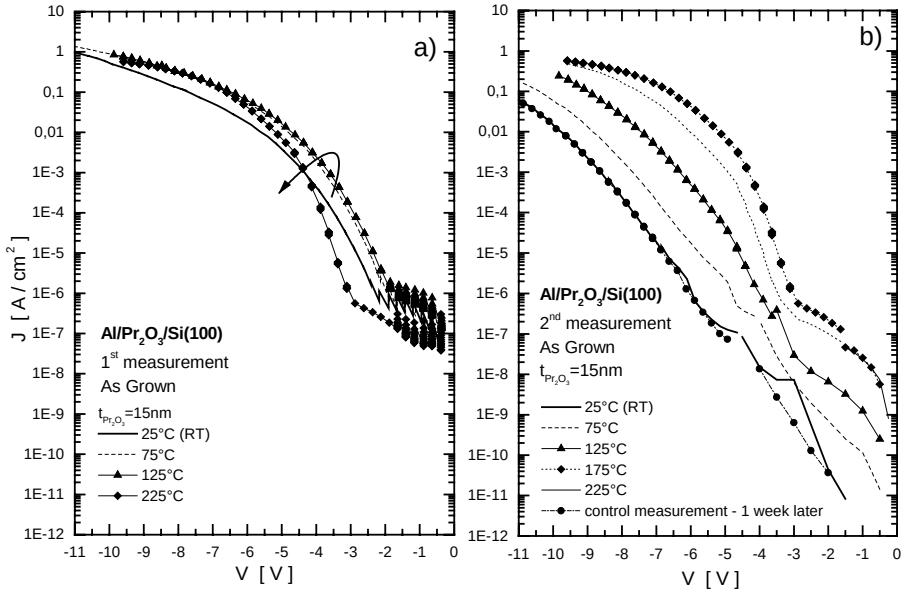


Figure 5.7 J(V) measurement for capacitor with 15nm Pr_2O_3 gate oxide. Furnace annealing (nitrogen, 600°C, 30min).

Modelling the temperature dependent J(V)-data

The J(V) data, measured for as-grown Pr_2O_3 films, have been analyzed and a conduction model extracted [Blank]. The current density vs. voltage characteristics reported in figure Fig.5.8 shows a $J \propto F \exp[F^{1/2}]$ dependence which suggest a Poole-Frenkel conduction mode in the temperatures range from 25°C to 125°C (figure 5.8a) and a $J \propto F^2 \exp[-1/F]$ (Fowler-Nordheim) dependence at higher temperatures (Fig.5.8b), where F is the electrical field in the oxide. A change in the dominant charge transport mechanism at temperatures between 125°C and 225°C happens. The conduction mechanism at high temperatures cannot be dominated by Fowler-Nordheim-Tunneling since the observed behaviour is approximately temperature independent.

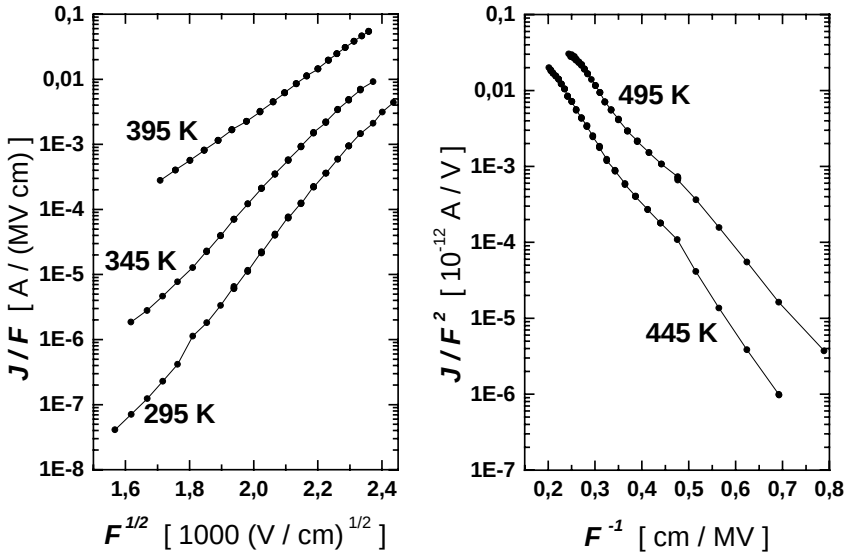


Figure 5.8 a) Poole-Frankel plot and b) Fowler-Nordheim plot from data reported in figure 5.4.

5.3.2. Capacitance vs. Voltage (C-V) Measurements

This section concerns the capacitance vs. voltage C(V) measurements and the extraction of the fundamental parameters that characterise the Pr_2O_3 gate oxide: dielectric constant (ε), equivalent oxide thickness (EOT) and interface state density (D_{it}).

5.3.2.1. Influence of substrate temperature on C(V)

The influence of the substrate temperature during Pr_2O_3 deposition in UHV-system has been introduced in section 5.2.1 of this chapter. The J(V) characteristics have been studied (subsection 5.3.1.1) and low leakage current where measured for $T_{Substrate}$=600°C.

In this section, the capacitance vs. voltage behaviour for Pr_2O_3 grown with different substrate temperature is presented. The process parameters are summarised in table 5-1.

Capacitance vs. voltage C(V) measurements are reported in figure 5.9. In general, as-grown sample have high hysteresis, that can be eliminated after annealing (as discussed later in this chapter). Comparing the C(V) characteristics of Pr_2O_3 samples grown with a

substrate temperature of 700°C and 600°C, it is possible to highlight some difference between the two oxide: samples grown with $T_{Substrate}$=700°C have bump in the C(V) curve, which indicate the presence of a thick SiO_2 layer at the interface between praseodymium oxide and silicon substrate. This is also confirmed by a lower dielectric constant when compared with samples grown at $T_{Substrate}$=600°C (ε=22 for $T_{Substrate}$=700°C while ε=26 for $T_{Substrate}$=600°C). Samples grown at $T_{Substrate}$=400°C have similar C(V) characteristics as Pr_2O_3 films grown with $T_{Substrate}$=600°C but higher leakage currents. For this reason, $T_{Substrate}$=600°C was chosen as substrate temperature during praseodymium oxide growth in UHV.

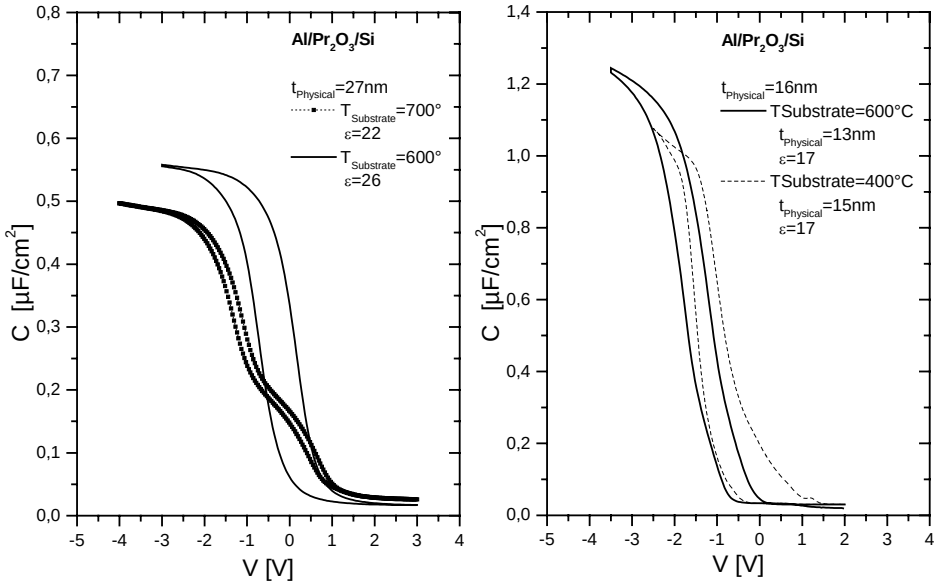


Figure 5.9 C(V) characteristics for MIS capacitors with Pr_2O_3 gate oxide MBD grown. Comparison between samples grown with different substrate temperatures

5.3.2.2. Influence of the ESV-Source material

The influence of the source material on the electrical characteristics of the deposited Pr_2O_3 films has been studied. As indicated in section 5.2.3, standard material used for praseodymium oxide growth in MBD system is Pr_6O_{11}, but the utilisation of this source requires long outgassing time and the stoichiometry of the deposited films is difficult to be controlled. In order to reduce the processing time and have a stable process, stoichimetric Pr_2O_3 was considered as alternative source material. The results obtained on samples grown using Pr_2O_3 as ESV-source material will be reported in this section.

Praseodymium Oxide grown from Pr_2O_3 99.9%

Capacitance vs. voltage C(V) characteristics for praseodymium oxide films grown in UHV, using a commercially available powder ceramic Pr_2O_3 99.9% as source material, are reported in figure 5.10. The praseodymium oxide films have a physical thickness of 15nm and have been grown with a $T_{Substrate}$=600°C. C(V) measurements for as-grown and nitrogen annealed samples are reported.

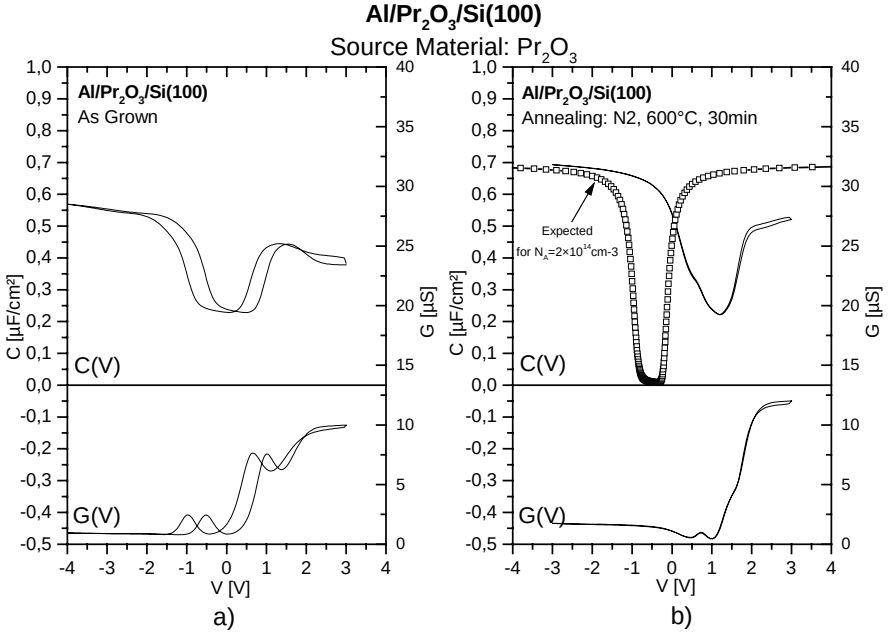


Figure 5.10 Capacitance vs. Voltage measurements for praseodymium oxide sample, growth using Pr_2O_3 99.9% as source material. Modulation frequency=20kHz.

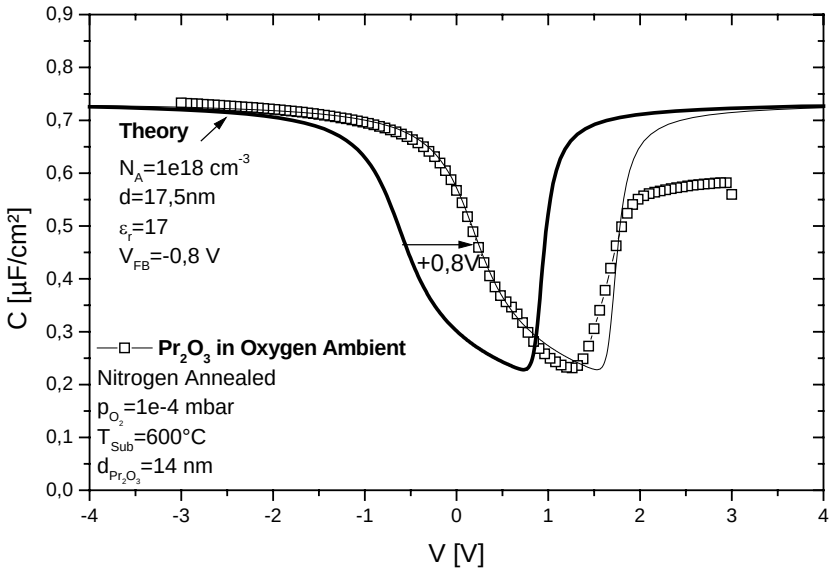


Figure 5.11 Capacitance vs. voltage measurements for praseodymium oxide sample growth using Pr_2O_3 99.9% as source material and the theoretical curve of silicon substrate doping N_A=1·18cm^{-3}. Modulation frequency=20kHz.

With respect to the expected C(V) behaviour for the substrate doping of the Si(100) wafers used for these experiments ($N_A=2\cdot10^{14}cm^{-3}$), the measured capacitance drastically increases in inversion and depletion region. In figure 5.10 b), the theoretical curve for the substrate doping under consideration is reported. Performing C(V) simulation [Sze], a good agreement was found between measured data and theoretical curves for a substrate doping of about $1\cdot10^{18}cm^{-3}$ (fig. 5.11). Forming the hypothesis that the silicon substrate has been p-doped during deposition, the Pr_2O_3 99.9% source material was investigated and the presence of 0.02% of boron was found. This impurity causes an unintentional contamination of the silicon substrate, that is evidenced with a change of the C(V) shape. The results show that Pr_2O_3 99.9% is not suited as source material for praseodymium oxide grown by MBD. The list of impurities detected by spectroscopic analysis in Pr_2O_3 99.9% powder is reported in table 5-3.

5.3.2.3. Influence of the annealing temperature on C(V)

The influence of annealing ambient on C(V) characteristics is argument of this section. The first studies reported in subsection 5.2.4 show that annealing in oxygen ambient produces the growth of an interface oxide that causes a reduction of the dielectric constant of the gate oxide.

In order to have an interface layer as thin as possible, annealing process in nitrogen ambient has been further investigated. The annealing temperature under consideration were 600°C and 500°C. First the standard process used for aluminium oxide has been taken in consideration: the Pr_2O_3 samples were annealed in nitrogen ambient, for 30min at 600°C. In a second moment, the MBD-grown praseodymium oxide films were nitrogen annealed at 500°C for 30min.

Capacitance vs. voltage characteristic C(V) for as-grown, 600°C and 500°C annealed samples are reported in figure 5.12. As-grown samples have high hysteresis (fig. 5.12, dashed line). Furnace annealing at 600°C drastically reduce the hysteresis but the C(V) shift to positive voltage, which indicates negative charges in the oxide layer (O^-). Moreover, the capacitance in the inversion region increases and the interface state density D_{it} is reduced of one order of magnitude (fig. 5.12, straight line).
Annealing the Pr_2O_3 samples in nitrogen at 500°C also reveals a reduction of the interface state density compared to as-grown samples, but C(V) measurements still show relevant hysteresis (fig.5.12, square symbols).

The important information that can be extracted from the C(V) characterisation are indicated in table 5-4. Al/Pr_2O_3/Si(100) capacitors show critical behaviour depending on the annealing temperature. If the annealing temperature is too low (500°C), the charges which causes the hysteresis cannot be eliminated. Higher annealing temperatures (600°C) are necessary to eliminate the hysteresis from C(V) measurements and to reduce the interface state density. Unfortunately this treatment produces a shift of the flat-band voltage which indicates the presence of negative charges inside the praseodymium oxide layer and a modification of the Pr_2O_3 morphology indicated by higher leakage current in J(V) characteristics.

Summarising the results:

Annealing at 600°C:
- reduces drastically the hysteresis
- C(V) shifts to positive voltage: negative charges in the oxide layer (O^-)
- increases the ε

• reduces the interface state density D_{it}

Annealing at 500°C:
• does not remove the hysteresis
• C(V) shifts to the expected V_{FB} (V_{FB} =-0.8V) for the Al-Si system under consideration
• reduces the interface state density D_{it}

Table 5-4 EOT and D_{it} extracted from C(V) measurements. All the annealing have been done in nitrogen for 30 min at 600°C.

Post-growth Temperature Treatment	**C/A** F/cm²	**T_{Al2O3}** ellipsometer nm	**ε_r**	**CEOT** nm	**Dit** [$eV^{-1}cm^{-2}$]
As Grown	6.6E-07	15	11	5.2	9E+12
Annealing at T=600°C	8.7E-07	15	15	4.0	8E+11
Annealing at T=500°C	9.0E-07	10	11	3.6	2E+12

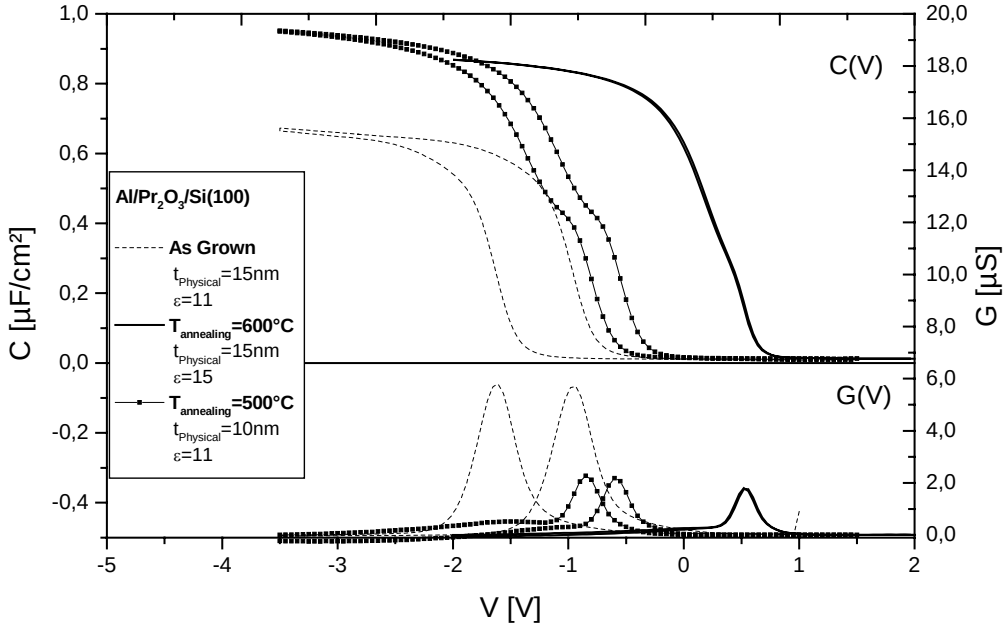


Figure 5.12 C(V) measurement for Al/Pr_2O_3/Si(100) annealed at different temperature. Dashed line: as-grown; square symbol: annealed in N_2, at 500°C for 30min; straight line: annealed in N_2, at 600°C for 30min.

5.3.3. Comparison of MBD-Pr_2O_3 with SiO_2 and Literature Reported Data

The leakage current measured for V_G-V_{FB}= -1V is used as parameter to compared the praseodymium oxide grown by MBD with silicon oxide having the same equivalent oxide thickness and with literature reported Pr_2O_3-data.

$J_{Leakage}$ vs. EOT is illustrated in figure 5.13. As reference, the leakage current measured for MBD-aluminium oxide are also reported. The direct tunneling behaviour indicated for SiO_2 and Al_2O_3 have been calculated has reported in Chapter 3 (Section 3.3.3).

UHV-grown Pr_2O_3 films have lower leakage current if compared with silicon dioxide having the same equivalent oxide thickness, but $J_{Leakage}$ are still high if compared with the electrical results reported from Osten et al. in their work on Pr_2O_3 [Osten].

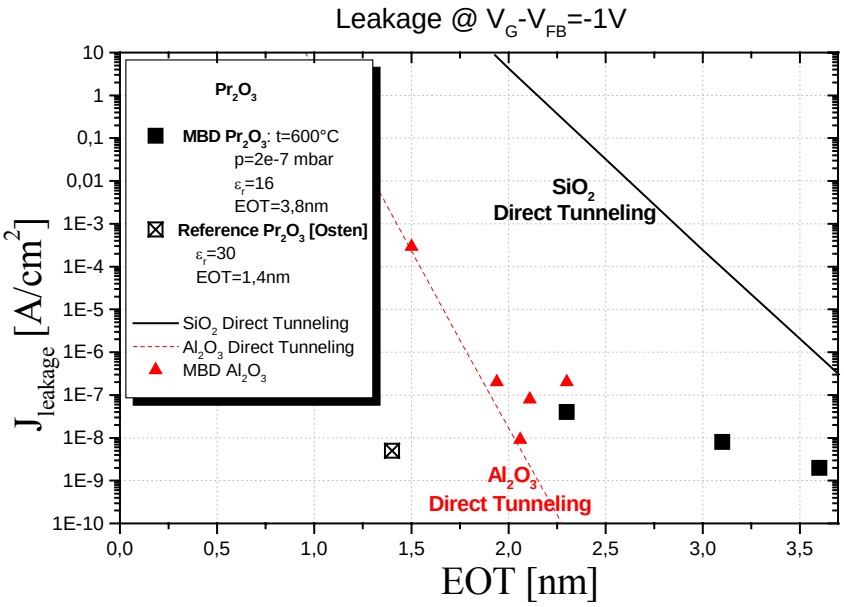


Figure 5.13 Leakage current density vs. EOT of MBE-Pr_2O_3 compared with SiO_2 and literature reported data.

5.3.4. Definition of UHV deposition process for Pr_2O_3

The investigation on praseodymium oxide reported in this chapter lead to the definition of the main process parameters for the MBD of praseodymium oxide on silicon substrate:

- source material: Pr_6O_{11}
- no external oxidising gas
- process pressure in the range of $1 \cdot 10^{-7}$mbar
- substrate temperature: T=600°C
- furnace Annealing: Nitrogen, 600°C, 30min to eliminate the hysteresis

5.4 Physical Analysis of MBD-grown Pr_2O_3 thin films

Praseodymium oxide thin films grown by molecular beam deposition have been analysed using different techniques in order to study the film composition and stoichimetry. In particular, chemical composition and physical structures of the gate stacks were studied by X-ray Photoelectron Spectrometry (XPS), Rutherford Back Scattering Spectrometry (RBS) and high-resolution Transmission Electron Microscope (TEM).

5.4.1. XPS Analysis

Composition and stoichiometry of Pr_2O_3 layer were analysed by X-ray Photoelectron Spectroscopy (XPS). Preceding the analysis the surface of the sample was sputtered with argon ions in order to eliminate the possible carbon contamination due to contact with air (approximately 4 nm of the film were etched). In figure 5.14 the complete spectrum of a 16 nm Pr_2O_3-layer a is reported.

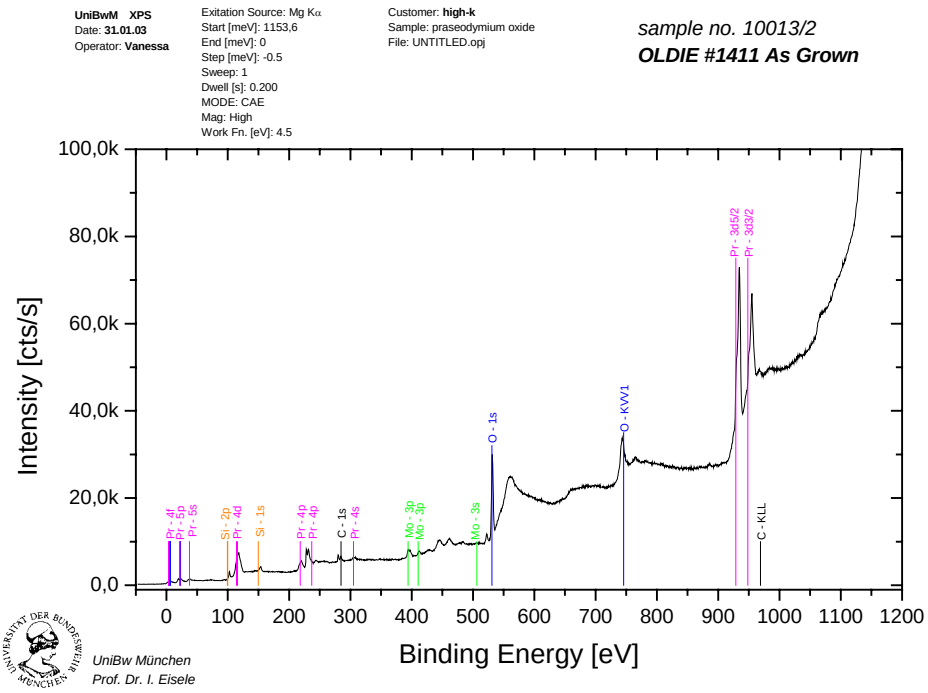


Figure 5.14 XPS spectrum of 16nm-thick praseodymium oxide layer after 15 min sputtering with Ar ions. All the reported lines refer to pure materials: magenta: praseodymium; orange: silicon; black: carbon; green: molybdenum; blue: silicon.

The XPS spectrum clearly shows the presence of praseodymium, oxygen and silicon inside the film. Small carbon and molybdenum can be identified as well and this is due to the sample holder.
The praseodymium peaks are shifted with respect to the pure material peaks (reference lines) in the direction of praseodymium oxide. Additional small silicon peaks can be seen, indicating bonding with oxygen to form SiO_x-Si.

In fig. 5.15, the zoom of Si 2*p* is reported together with peak Pr 4*d*. The surface scan (meas. 1) shows an high praseodymium peak and a low silicon one. Lines for pure silicon

and praseodymium are also reported. The silicon peak is shifted to higher energies with respect to the reference Si 2*p* and correspond to Si-O binding energy (102.6 eV). This effect was also reported by Fissel et al. [Fissel02]. In this work it is explained that a silicon peak at about 102.5 eV energy indicates its origin in a Si^{+3} suboxide state (or Si-SiO_3) interface configuration. This implies that during the growth process additional oxygen enters in the interface region. This peak increases for higher temperatures indicating a diffusion-driver accumulation of oxygen in the interface region.

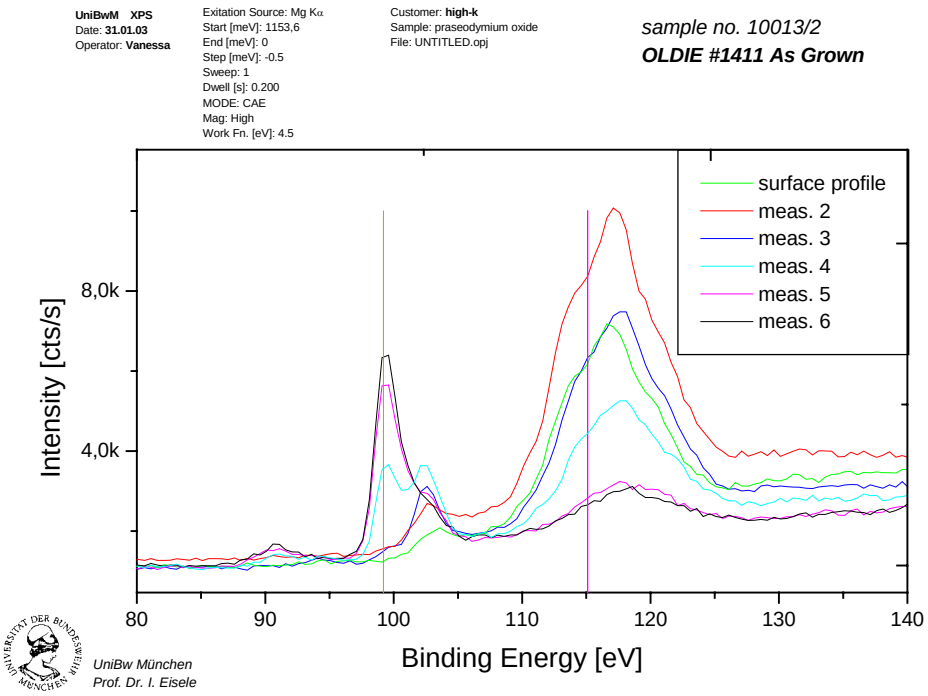


Figure 5.15 Si 2*p* and Pr 4*d* core-level spectra for MBD Pr_2O_3 on Si(100) substrate

5.4.2. RBS (Rutherford back scattering)

The stoichiometry of a praseodymium oxide grown from Pr_6O_{11} source material has been studied by RBS analysis.

As-grown samples have a nearly ideal Pr_2O_3 stoichiometry. The analysis of the capacitance measurement show that this sample also has a flat band voltage around the theoretical value (-0,8V). RBS analysis and C-V measurements for as grown sample are reported in fig. 5.16.

After annealing (nitrogen, 600°C, 30 min), RBS shows an oxygen-rich stoichiometry ($Pr_2O_{3.5}$) that can also be deduced from C(V) curves. As can be seen in fig. 5.17, after annealing the C(V) curve is shifted to positive voltage (around +1V), which indicates negative charges inside the insulator film.

During annealing the praseodymium oxide becomes oxygen rich as it is confirmed by coherent RBS and C(V) results.

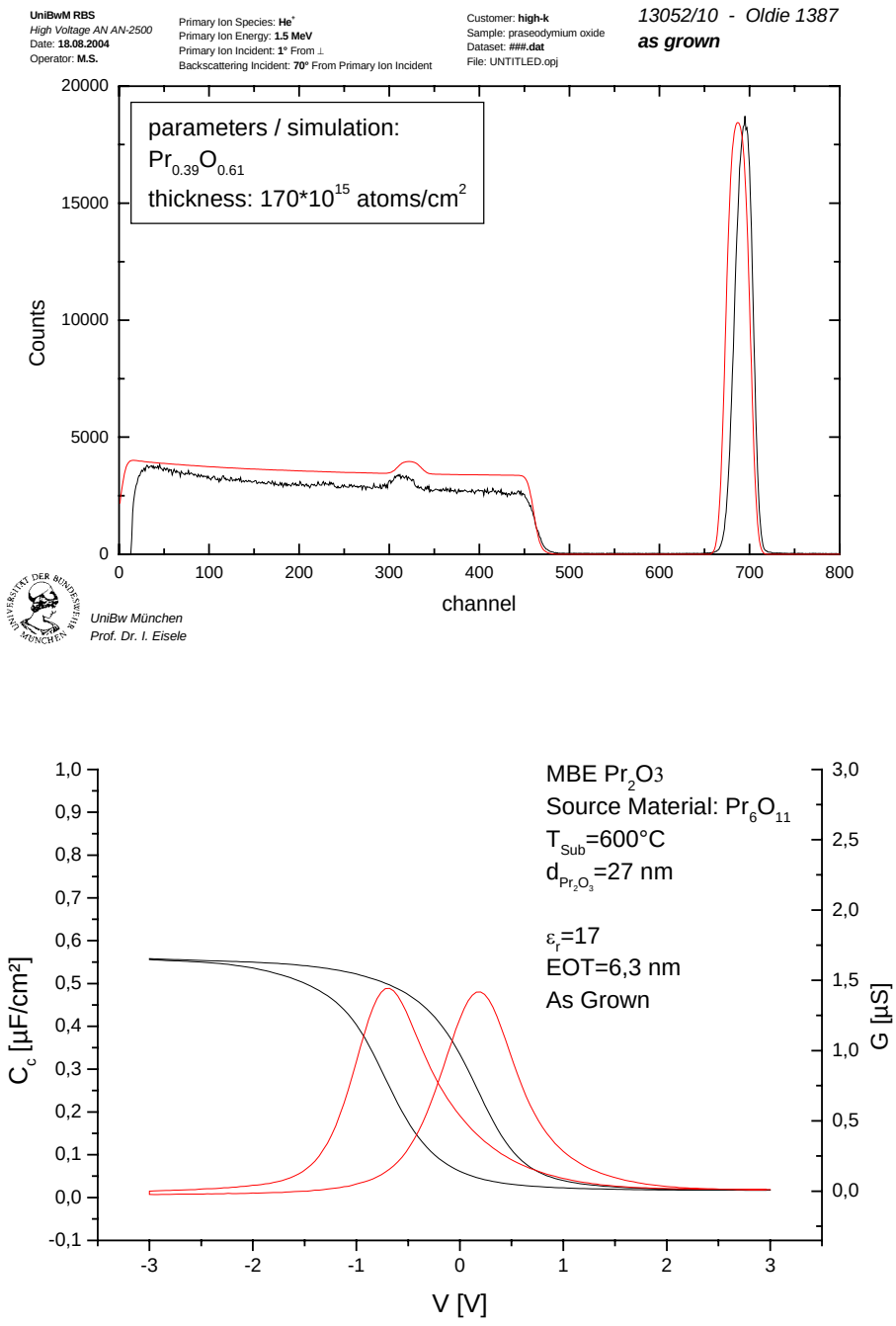


Figure 5.16 RBS analysis of praseodymium oxide grown from Pr_6O_{11} source material. As Grown: nearly stoichiometric Pr_2O_3. Capacitance vs. voltage measurements are also reported: flat band voltage is around the expected value (-0,8V).

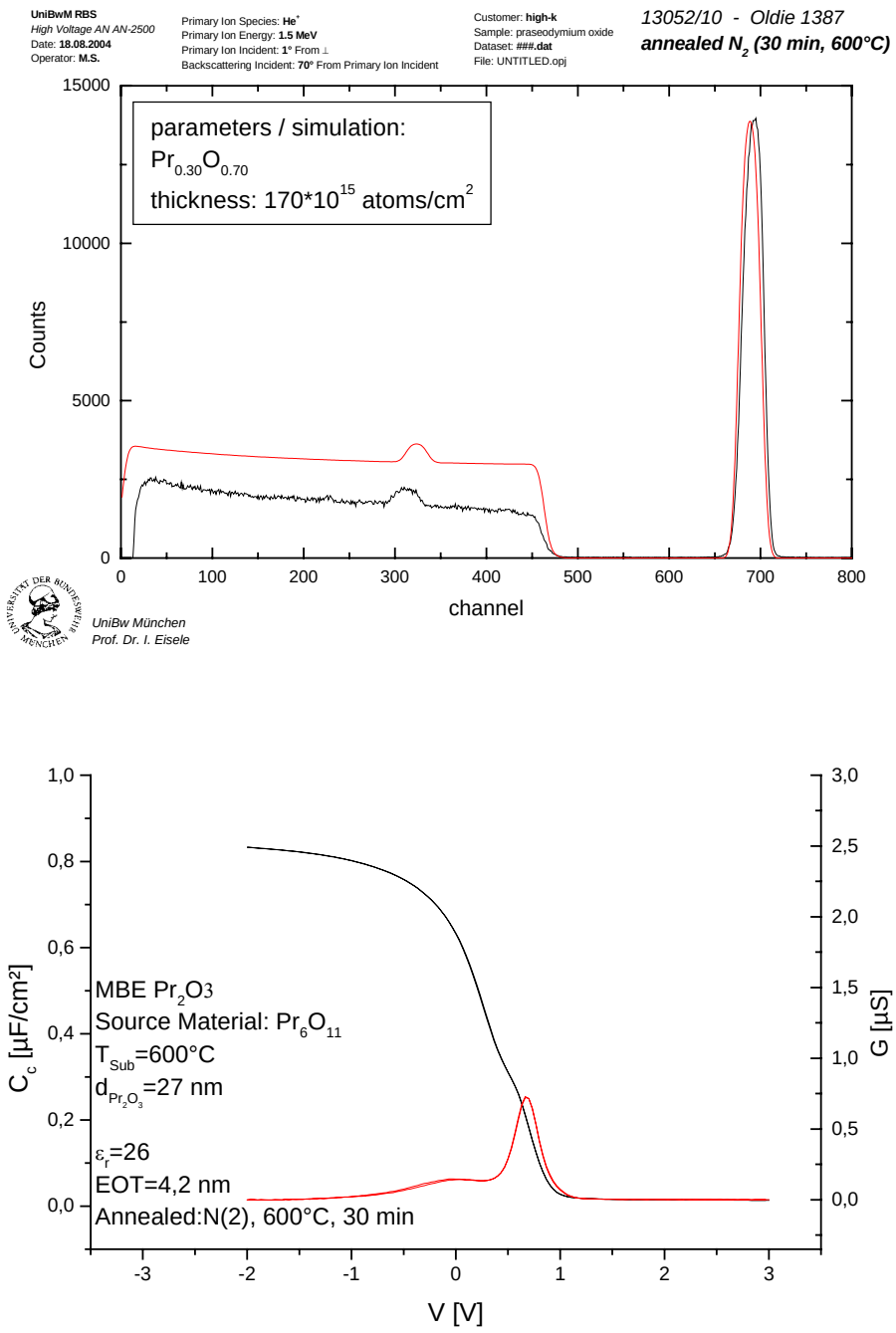


Figure 5.17 RBS analysis of praseodymium oxide grown from Pr_6O_{11} source material. Oxygen rich praseodymium oxide (shift in C-V curve to positive voltage).

5.4.3. TEM: Pr_2O_3 on Silicon: Structural characterization

TEM analysis of MBD grown Pr_2O_3 has been performed in collaboration with Infineon AG [Inf_rep].
The first important result that can be extracted from these TEM analysis is that the interface between gate oxide and silicon substrate is extremely rough. As-grown samples have a thin intermediate layer (1 nm) between the Pr_2O_3 and the silicon substrate.
The measured thickness is around 14 nm, very close to the ellipsometer measurement which was 15 nm for this sample. From figure 5.18 it can be seen that the bottom 3 nanometers of Pr_2O_3 are amorphous while the top 11 nm are polycristalline.
Samples annealed in nitrogen at 600°C for 30min are similar to as-grown-samples. They only present lightly thicker interface layer (1.5 nm).
An electron diffraction pattern from a thin area of the TEM specimen contains both circles and nearly discrete diffraction spots (figure 5.22). The grain size is about 15 nm.

Selected Area Electron Diffraction (SAD)

Both silicon substrate and praseodymium oxide layer are contained in the TEM planview specimen in thicker sample areas. The according SA electron diffraction patterns show both reflexes of the silicon substrate and the praseodymium oxide layer (figure 5.20 a-b). The four-fold arrangement of the praseodymium oxide diffraction spots is related to domain-like growth of the praseodymium oxide structure and dynamical diffraction effects, i.e. electrons are subsequently diffracted by the substrate and the praseodymium oxide layer. Thus each substrate reflex becomes the center of a praseodymium oxide pattern (figure 5.20 b)

The electron diffraction patterns of thin and thick TEM specimens areas depict a maximal lattice spacing of 0.315 nm. None of the three known Pr2O3 phases has such a lattice parameter (table 5-4). However, there are four cubic praseodymium oxide phases ($PrO_{1.83}$, Pr_4O_7, PrO_2, Pr_6O_{11}), all with a similar lattice parameter and a (111)-lattice spacing of about 0.315 nm.

All lattice spacing of the present electron diffraction patterns can be attributed to this cubic structure (figures 5.20 and 5.21 a-b). The cubic structure is (110) textured and the praseodymium oxide (200) planes are preferentially parallel to the Si substrate (220) planes (3.2a). There are two types of domains presented, rotated over an angle of 90° with respect to each other (figure 5.22).

Table 5-5 Power Diffraction data for known praseodymium oxide phases [Inf_rep].

Phase	Space Group	PDF-Card	lattice spacing (sorted by intensity)
Pr2 O3	P-3m1	06-0410	2.92/X 3.01/4 1.93/4 3.34/4 2.24/4 1.72/3 1.63/3 1.61/2 1.67/1 1.46/1
Pr2 O3	P-3m1	37-0825	2.92/G 1.93/G 3.34/G 3.01/G 1.72/G 2.23/G 1.62/G 1.61/G 1.67/X 1.46/2
Pr2 O3		22-0880	2.88/X 2.77/X 2.85/7 3.26/5 1.89/5 1.79/4 3.15/4 2.74/4 1.99/3 1.84/3
Pr O1.83	Fm3m	06-0329	3.15/X 1.93/5 1.65/4 2.73/4 1.25/1 1.58/1 1.22/1 1.12/1 1.05/1 0.92/1
Pr4 O7	F	14-0341	3.19/X 1.94/8 1.66/8 2.71/6 5.60/4 2.24/4 1.98/4 1.59/4 6.40/2 2.52/2
Pr O2	Fm3m	24-1006	3.11/X 1.91/7 1.63/6 2.69/3 1.24/3 1.10/2 1.21/2 1.56/1 1.35/1 0.00/1
Pr O	F	33-1076	2.91/X 2.52/9 1.78/6 1.52/5 1.15/2 1.45/2 1.26/2 1.13/1 1.03/1 0.00/1
Pr O1.83		35-0104	3.02/X 3.42/5 1.79/5 5.00/3 3.60/3 2.33/3 2.01/3 1.70/3 0.00/1 0.00/1
Pr6 O11	Fm3m	42-1121	3.16/X 1.93/3 2.73/3 1.65/2 1.25/1 1.58/1 1.22/1 1.12/1 1.05/1 1.37/1

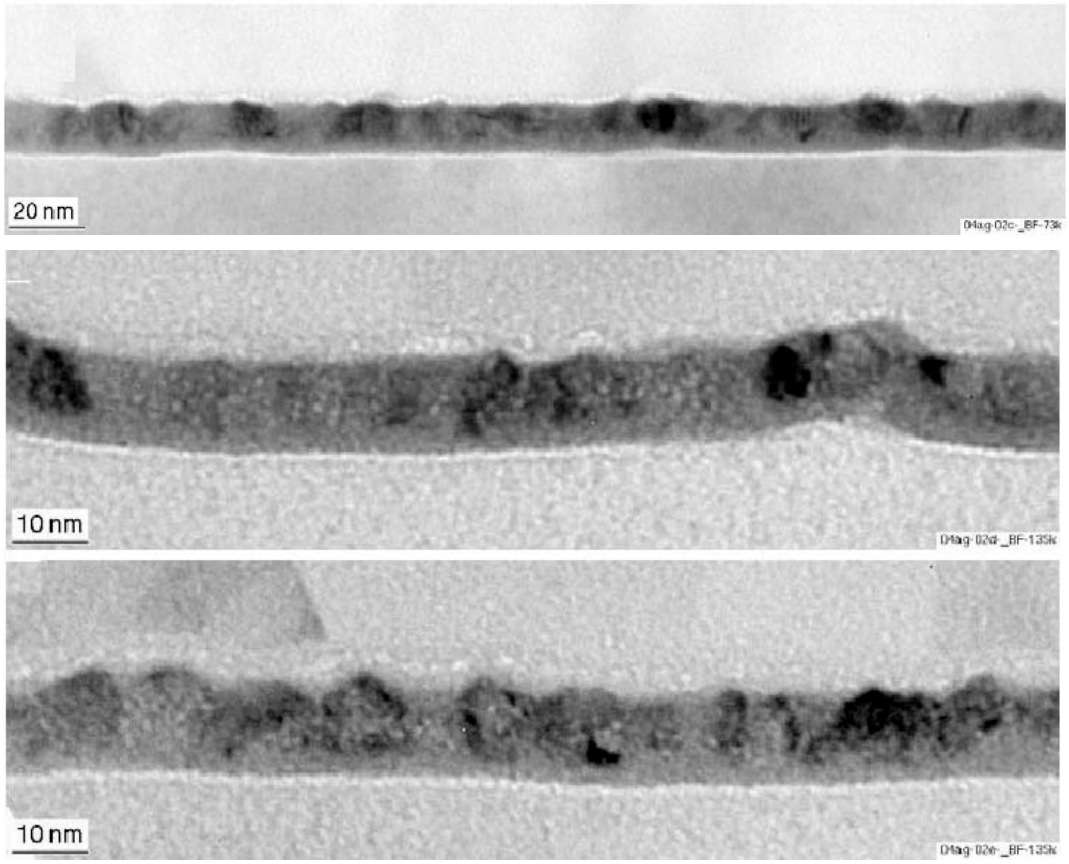


Figure 5.18 Praseodymium oxide on silicon, plan view [fig. 3.1j - Inf_rep].

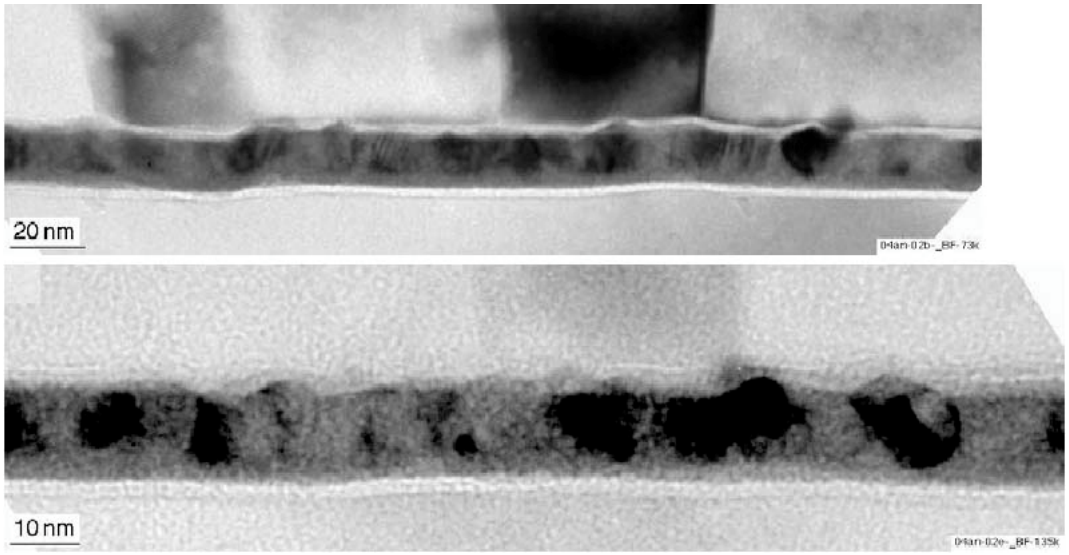


Figure 5.19 Praseodymium oxide on silicon, plan view [fig. 3.1j - Inf_rep].

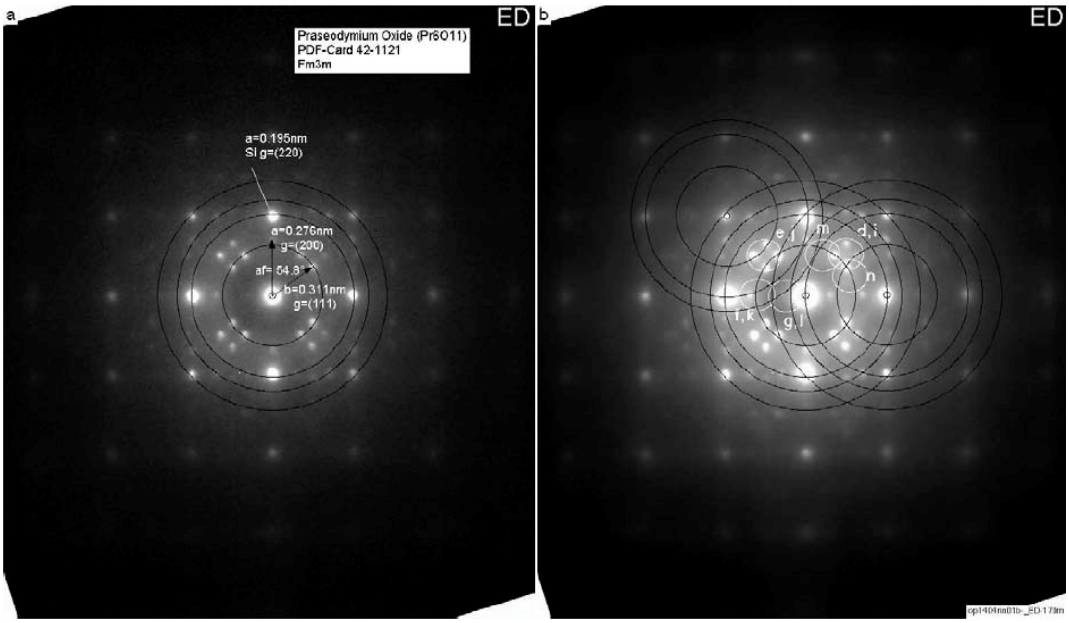


Figure 5.20 Praseodymium oxide on silicon. 200kV PV-TEM (plan view). Black circles indicate power diffraction lattice spacing. White circles depict object aperture settings for the dark field images [fig. 3.2a-b - Inf_rep].

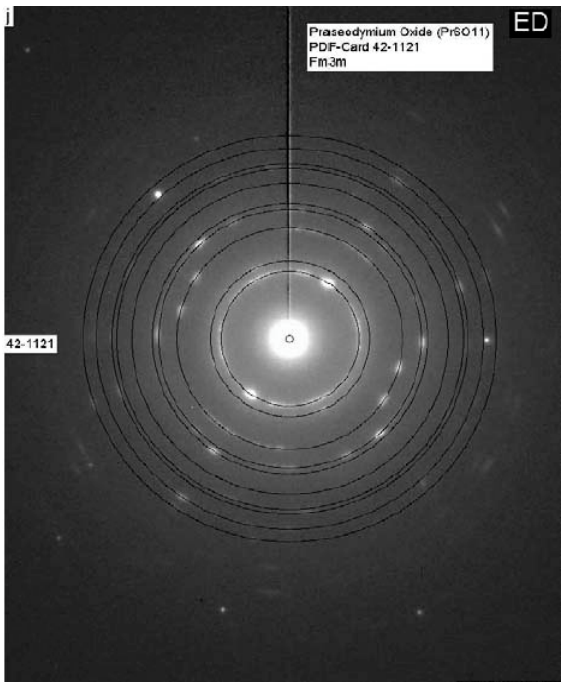


Figure 5.21 Praseodymium oxide on silicon, plan view [fig. 3.1j - Inf_rep].

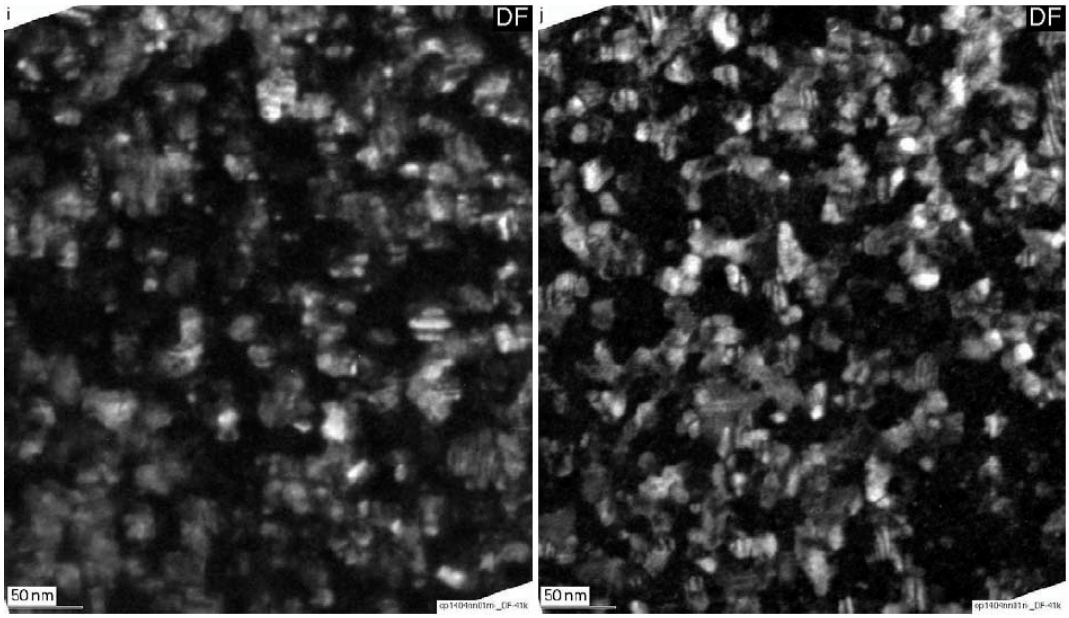


Figure 5.22 Praseodymium oxide on silicon. 200kV PV-TEM (plan view). [fig. 3.2i-j - Inf_rep].

5.5 Development of Interface Passivation Process

Electrical characterisation has shown that praseodymium oxide is not a barrier for oxygen diffusion. Moreover, if impurities are present in the deposited film these diffuse through the Pr_2O_3 layer and the insulator/silicon interface to reach the silicon substrate and alter the electrical characteristics of the MOS capacitor (see 5.3.2.3).

A sharp transition between gate oxide and silicon substrate is required to have a control of the device performances. Therefore it is necessary to develop a diffusion barrier that decreases or prevents diffusion of impurity atoms without increasing the interface state density. The idea is that a surface treatment of silicon wafers with nitrogen radicals generated by a remote plasma source will form a barrier on the silicon wafers which hinder the diffusion of the impurities.

The plasma passivation process is carried out at room temperature. In this way, an ultra-thin nitrogen layer is expected be formed at the interface between insulator and silicon substrate. Plasma passivation is part of the PhD thesis "Modification von Silizium-Grenzflächen für MOS-Technologie", drew up by T. Sulima [Sulima03]. The interesting results concerning praseodymium oxide are reviewed in this chapter.

Praseodymium Oxide grown from Pr_2O_3 with Interface Passivation

In order to avoid involuntary reaction at the interface between dielectric and silicon substrate, the passivation of the silicon interface was studied.
Praseodymium oxide films where grown on Si(111) n-doped wafers. Before deposition, part of the wafers were treated with plasma passivation and some others, used as references, were only cleaned with RCA.

A source material rich of impurities (Pr_2O_3 99.9%) has been chosen in order to investigate the effect of the passivation process. Although it has been shown that this source material is not indicated for the MBD of praseodymium oxide layer (see subsection 5.3.2.2), its high content of impurities can give a clear indication on the efficacy of the N_2-plasma passivation.

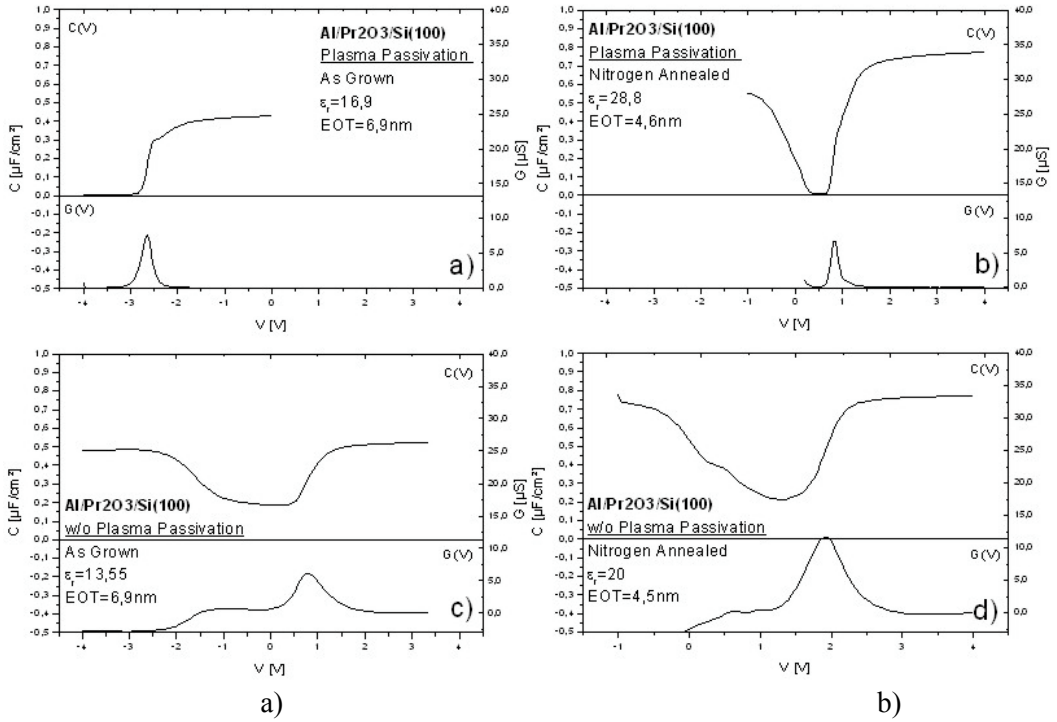
A comparison of the capacitance vs. voltage characteristics for treated and untreated samples is reported in fig. 5.23. All the Pr_2O_3 films were grown in UHV, with a $T_{Substrate}$=600°C.

- As Grown Samples

As-grown Pr_2O_3 films on plasma passivated wafers (fig. 5.23a) have the expected C(V) shape for the substrate doping under consideration, but they also how relevant shift of the V_{FB} to negative voltage. This indicates positive charge inside the dielectric film. These charges are due to an excess of metal atoms, meaning that the deposited layer under this condition is praseodymium rich. Considering the capacitance vs. voltage characteristic for as-grown Pr_2O_3 films deposited on un-passivated wafers (fig. 5.23c), it is evident that the V_{FB} is not shifted. The C(V) shape reveals rather a substrate doping due to the impurity present in the source material (as reported in section 5.3.2.3 of this chapter)

- Annealed Samples

After annealing in nitrogen for 30min at 600°C the curves are shifted to the positive voltage, which indicates negative charge inside the insulator due to O^-.
After annealing an increase in dielectric constant can be noticed especially for samples grown on passivated wafers, indicating an higher stablility against oxygen diffusion (table 5-6).



a) b)

Figure 5.23 Capacitance vs. voltage measurements for Pr_2O_3 films grown on silicon substrate with and without interface passivation. a) and c) as-grown, with and w/o plasma passivation, respectively; b) and d) annealed (nitrogen, 600°C, 30min) with and w/o plasma passivation, respectively.

These results suggest that nitrogen passivation is a very effective barrier against impurity diffusion. The proposed plasma treatment leads to an higher shift of the C(V) curves with respect to the expected behaviour, suggesting a relevant presence of charge inside the gate oxide. Moreover, the interface state density increases. Samples grown on plasma-treated wafers have an interface state density one order of magnitude higher than untreated ones.

Table 5-6 EOT and D_{it} extracted from C(V) measurements. All the annealing have been done in nitrogen for 30 min at 600°C.

Process (Wafer no.)		C/A	T_{Pr2O3} ellipsometer	ε_r	CEOT
		F/cm²	nm		nm
Si(111) n-type - #1398	As-grown	5,00E-07	30	16,94	6,9
N_2- Plasma passivation	Annealing	7,50E-07	34	28,80	4,6
Si(111) n-type - #1399	As-grown	5,00E-07	24	13,55	6,9
Not passivated	Annealing	7,70E-07	23	20,00	4,5

5.6 Conclusion

The possibility to grow praseodymium oxide thin films on silicon substrate by molecular beam deposition has been investigated in this chapter.

To optimise the deposition process the influence of the different process parameters on the Pr_2O_3 films and the material source used for e-beam evaporation were deeply studied by electrical characterisation of Al/Pr_2O_3/Si capacitors.

J(V) and C(V) measurements highlight that praseodymium oxide is a very critical system, highly temperature dependent and strongly influenced from the ambient moisture.

Comparing the leakage current measurements of praseodymium oxide with SiO_2 and literature data it is evident that MBD-Pr_2O_3 films grown with the developed deposition process have lower $J_{Leakage}$ than SiO_2 for the same EOT, but are still far away from the better results reported in literature [Osten]. The reason for this result is to be researched in the system used for sample preparation. Osten et al. work with a close system in which the praseodymium oxide films do not enter in contact with the ambient and maintain their properties.

Temperature studies on Al/Pr_2O_3/Si capacitors have highlighted the low thermal stability of the praseodymium oxide, who starts to crystallise already at low temperature and easily changes its composition. This instability and the critical deposition process excludes Pr_2O_3 from the interesting candidate for alternative gate dielectric in CMOS technology.

Chapter 6

Deposition process optimisation and characterisation of thin La_2O_3 films grown by means of MBD

Because of the its high dielectric constant and resistance to crystallisation La_2O_3 is a very promising candidate as alternative gate oxide. This chapter investigates the properties of lanthanum oxide and illustrates the development and the optimisation of a molecular beam deposition process for La_2O_3 thin films on silicon substrate.

The high sensibility to moisture adsorption, typical of lanthanide oxides, is one of the unsolved problems when using lanthanum oxide as gate oxide. Therefore the influence of the humidity on the electrical properties is especially considered for the investigated system and intensive research has been done to solve this problem with an optimisation of the post-growth annealing.

La_2O_3 thin films grown with the developed process have been electrically and physically characterised and compared with Al_2O_3- and Pr_2O_3-system. Stoichiometry and morphology of the lanthanum oxide were studied by AES, XPS and TEM, and the electrical properties investigated by current density vs. voltage J(V) and capacitance vs. voltage C(V) characterisation.

6.1. Physical properties of La_2O_3

Rare earth oxides, also called lanthanide oxides, are very interesting candidates as alternative gate. The results reported for La_2O_3 [Iwai02], Pr_2O_3 [Osten00] and CeO2 [Nishi01] underline that in particular lanthanum oxide (La_2O_3) is an attractive material because of its high dielectric constant (20-30) [Huff05], thermal stability on silicon substrate until 1000K [Hubba96; Maria01], resistance to crystallisation [Iwai02] [Iun02] and appreciable high band-gap and band-offset with respect to silicon.

The principal properties for the high-k systems studied in this thesis compared with silicon oxide and silicon nitride are illustrated in table 6-1. In the selection of the alternative dielectric for gate application not only the dielectric constant plays a fundamental role: special attention must be also be paid to the barrier height and to the conduction band offset. A large conduction band offset (silicon-to-insulator energy barrier height) is desirable because the gate direct-tunneling grows exponentially with the barrier height. Moreover, the high-k material should not only have a large band-gap, but also a band alignment with silicon which results in a large conduction band offset.

Figure 6.1 shows the values of band-gap, lattice energy and dielectric constant for the rare oxides. It is evident, among the lanthanide oxide, that La_2O_3 exhibits the requested properties for high-k gate dielectric and it is a strong candidate to substitute SiO_2 as gate oxide.

Because of the expected high temperature excursion during CMOS processing thermodynamic stability against silicon is of primary consideration. From the evaluation of the available solid-state thermodynamics data it can be concluded that La_2O_3 is stable in contact with silicon at 1000K. However, this stability is expected under equilibrium conditions [Hubba96].

The exact phase diagram of the lanthanum–oxygen system is not known. A tentative to calculate the La-O phase diagram has been published by Grundy et al. [Grundy01] and it is shown in figure 6.2. This diagram has to be considered as highly speculative because of the lack of binary data.

In general, the lanthanum oxide exist in several modifications depending on the temperature. The crystallographic data are given in table 6-2 [LB-IV/5].

The only stable polymorphic form La_2O_3 at room temperature is α-type. In a mixture with lanthanum metal the equilibrium composition of the lanthanum oxide is sub-stoichiometric, an effect that is due to the formation of oxygen vacancy.

Table 6-1 Electrical properties of high-k dielectrics. Data from [Wong02]

Material	Dielectric constant (ε)	Band-gap E_g [eV]	ΔE_C to Si [eV]
Silicon dioxide (SiO_2)	3.9	9	3.5
Silicon nitride (Si_3N_4)	7	5.3	2.4
Aluminium oxide (Al_2O_3)	≈ 10	8.8	2.8
Praseodymium oxide (La_2O_3)	≈ 30		
Lanthanum oxide (La_2O_3)	20-30	6	2.3

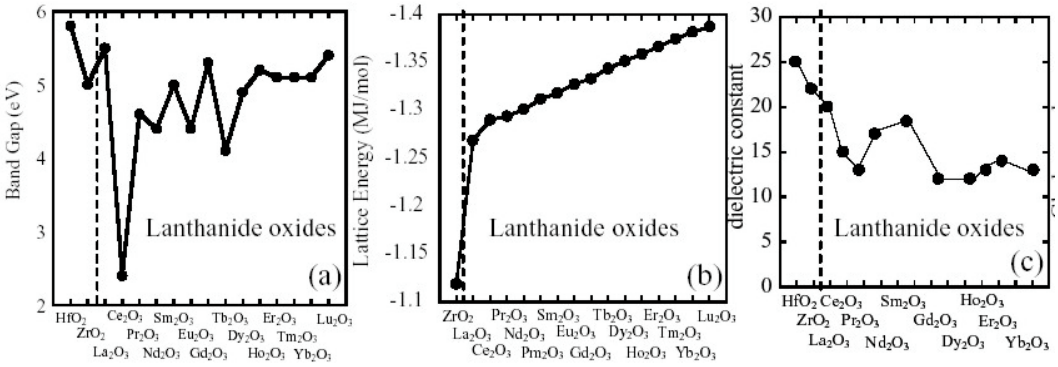


Figure 6.1 Properties of lanthanide oxides. (a) band gap; (b) lattice energy, (c) dielectric constant. After [Iwai02]

Table 6-2 Crystal structure for La-O system. After [LB-IV/5, page 284]

Phase	T [K]	Structure	Type
α-La_2O_3	< 823	cub	Mn2O3
β- La_2O_3	823...2273	hex	La_2O_3
γ- La_2O_3	2273...2373	hex (?)	
δ- La_2O_3	> 2373	cub	La_2O_3
La_2O_3 *)		mon	

* prepared by chemical reaction

Although the thermodynamic stability of lanthanum oxide on silicon substrate has been evaluated at 1000K under equilibrium conditions, a recent study on interfacial reaction

between lanthanide oxides and Si- substrate highlighted that in rare-earth oxides silicon atoms from the substrate diffuse easily into Re_2O_3 films (Re are rate-earth elements) and form Si-O-Re bonds, creating an interfacial $ReSi_xO_y$ layer [Ono01; Wu02]. It is very interesting to take into consideration the published phase diagram for the La_2O_3-SiO_2 system, illustrated in figure 6.3: the line composition corresponding to $La_2O_3 \cdot SiO_2$ and $La_2O_3 \cdot 2SiO_2$ extends to low temperature and melt congruently, suggesting that at the process and annealing temperature used, depending on the quality of the silica present, the silicate phase would be thermodynamically preferred.

The major drawback of lanthanum oxide, as all others rare earth metal oxide, is its high sensibility to humidity. Moisture adsorption leads to film degradation and solutions to this problem have to be found when La_2O_3 is to be used as gate dielectric.

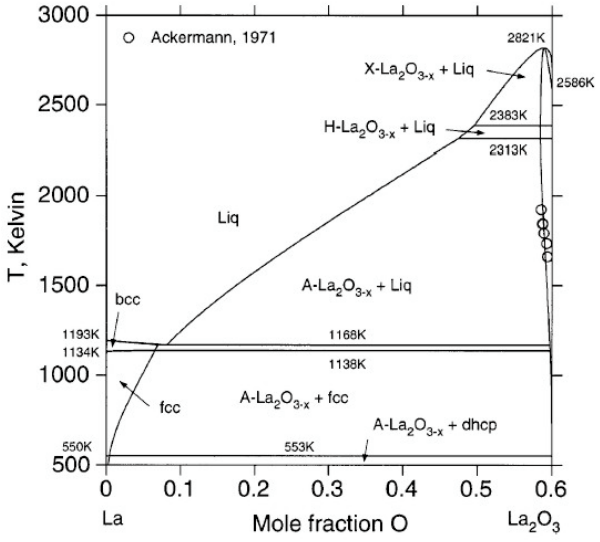


Figure 6.2 phase diagram for La-La_2O_3 system. Of interest is the stability of the α-La_2O_3 for temperature lower that 800°C

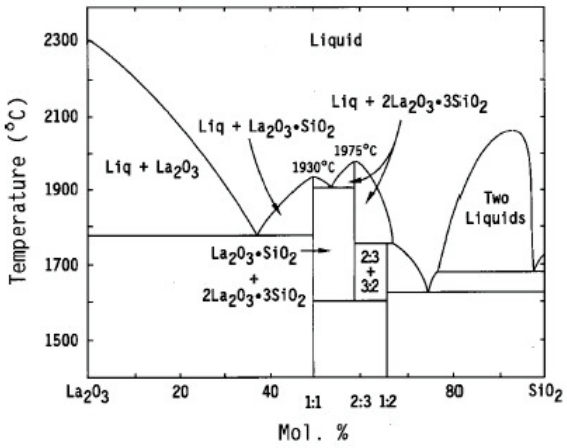


Figure 6.3 phase diagram for La_2O_3-SiO_2 system. Of interest is the low temperature stability of the $La_2O_3 \cdot SiO_2$ and $La_2O_3 \cdot 2SiO_2$ phases and the congruent melting $La_2O_3 \cdot SiO_2$ and $La_2O_3 \cdot 2SiO_2$. After [Levi85]

6.2. Process optimisation and electrical characterisation of MBD-grown La_2O_3 thin films

Lanthanum oxide thin films were grown on silicon substrate by MBD. The deposition process in UHV-system was optimised investigating the influence of substrate temperature, oxygen partial pressure and post-growth annealing on the electrical characteristics of Al/La_2O_3/Si capacitors. After deposition, the influence of the annealing process was studied by treating the La_2O_3 samples in nitrogen and oxygen ambient. The effects of furnace annealing and rapid thermal processing (RTP) were studied separately and then combined to achieve the better properties for lanthanum oxide thin films.

6.2.1. Current Density vs. Voltage (J-V) Measurements

In this section the influence of substrate temperature and oxygen pressure during deposition process of La_2O_3 thin films by current density vs. voltage J(V) measurements of Al/La_2O_3/Si(100) capacitors are investigated.

6.2.1.1. Influence of substrate temperature on J(V)

The substrate temperature $T_{Substrate}$ normally used during deposition of lanthanum oxide films for gate application is included in the range of 300-700°C in order to avoid possible beginning of crystallisation, as indicated in most of the papers on La-based dielectrics [Lu04,Mereu04, Velli04, Yang04, Jun02, Maria01, Stem01].

During this thesis amorphous lanthanum oxide has been grown by MBD on silicon substrate. The influence of the substrate temperature on the electrical properties of MBD-La_2O_3 layer has been studied within the range $T_{Substrate}$=400-700°C.

Figure 6.4 shows the J(V) characteristics of 15nm and 25nm La_2O_3 MOS devices measured under accumulation. Process conditions, film thickness and substrate temperatures are listed in Table 6-3.

Lanthanum oxide films grown with a substrate temperature of 400°C (fig. 6.4, pyramid symbol) have higher leakage current compared to La_2O_3 samples grown under the same condition but with higher $T_{Substrate.}$ The leakage currents measured for -1V gate voltage given in table 6-3. Increasing the $T_{Substrate}$ from 400°C to 600°C the leakage current is reduced by nearly one order of magnitude. Moreover, a higher substrate temperature strongly improves the breakdown behaviour of the gate oxide: the breakdown voltage (V_{BD}) moves from 3MV/cm ($T_{Substrate}$=400°C) to 6MV/cm ($T_{Substrate}$=600°C). This result is due to the fact that the deposition process of lanthanum oxide for low substrate temperature ($T_{Substrate}$=400°C) will produce an oxide layer with high defect density which will increase the leakage mechanism inside the gate oxide. A confirmation of this model is given when the interface state density are compared (D_{it} in table 6-3): lanthanum oxide grown with $T_{Substrate}$=400°C have D_{it}= $1 \cdot 10^{13}$ $eV^{-1}cm^{-2}$, while higher substrate temperature will reduce the state density of one order of magnitude (D_{it}= $1 \cdot 10^{12}$ $eV^{-1}cm^{-2}$ for $T_{Substrate}$=600°C and 700°C).

A further increase of the substrate temperature will produce a thicker interface oxide between gate dielectric and silicon substrate without improving the electrical properties of the La_2O_3 films. Comparing the J(V) measurements for $T_{Substrate}$ of 600°C and 700°C shows that the two samples have nearly the same V_{BD} (4MV/cm and 3MV/cm, respectively). The leakage currents measured for –1V gate voltage is lightly smaller for $T_{Substrate}$=600°C.

Table 6-3 Study of the influence of substrate temperature La_2O_3 deposition process

Wafer no.	Interface Engineering	$T_{Substrate}$ [°C]	Ambient / Pressure [mbar]	$t_{Physical}$ [nm]	D_{it} [$eV^{-1}cm^{-2}$]	$J_{Leakage}$ @ -1V [A/cm^2]
10024/01	Ther. Desorption T=900°C, t=5min	700	Oxygen/ $1*10^{-4}$	25	$1\cdot10^{12}$	$2\cdot10^{-8}$
10024/02	Ther. Desorption T=900°C, t=5min	600	Oxygen/ $1*10^{-4}$	25	$1\cdot10^{12}$	$8\cdot10^{-9}$
14064/04	C-burning	400	Oxygen/ $1*10^{-5}$	15	$1\cdot10^{13}$	$1\cdot10^{-7}$
14064/03	C-burning	600	Oxygen/ $1*10^{-5}$	15	$1\cdot10^{12}$	$4\cdot10^{-8}$

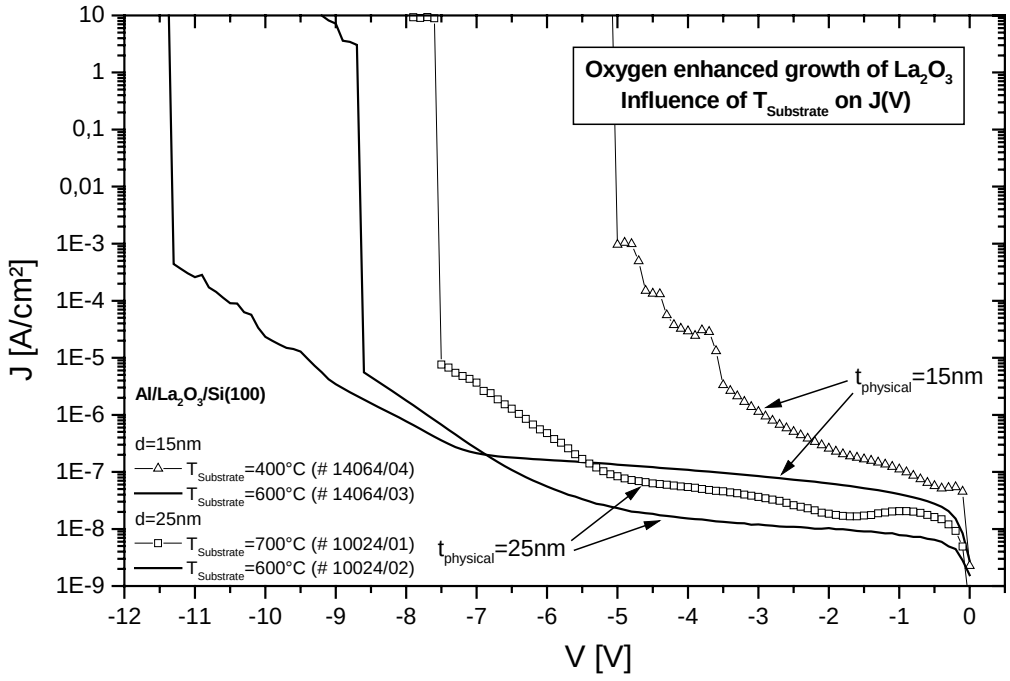


Figure 6.4 J(V) characteristics for $Al/La_2O_3/Si(100)$. La_2O_3 films were grown by MBD with different substrate temperatures.

6.2.1.2. Influence of oxygen partial pressure on J(V)

During the growth of La_2O_3 films in oxidising ambient the high oxygen diffusivity in La_2O_3 films [Jun03] has to be taken into account. To avoid an excessive silicon dioxide formation at the interface between the gate oxide and the silicon substrate during the MBD-process, a maximal oxygen pressure of $1 \cdot 10^{-4}$mbar was considered.

Lanthanum oxide films have been grown in UHV-system under different the oxygen partial pressure. Table 6-4 summarises the important MBD-parameters and electrical properties of the studied La_2O_3 layers.

Current density vs. voltage J(V) measurements are reported in figure 6.5. Three different oxygen conditions have been used: a first sample (fig. 6.5, cross symbol) was grown without additional oxygen; a second one (fig. 6.5, straight line) was grown with a oxygen pressure of $p_{O2}=1 \cdot 10^{-5}$ mbar and a third one (fig. 6.5, square symbol) was grown with $p_{O2}=1 \cdot 10^{-4}$mbar

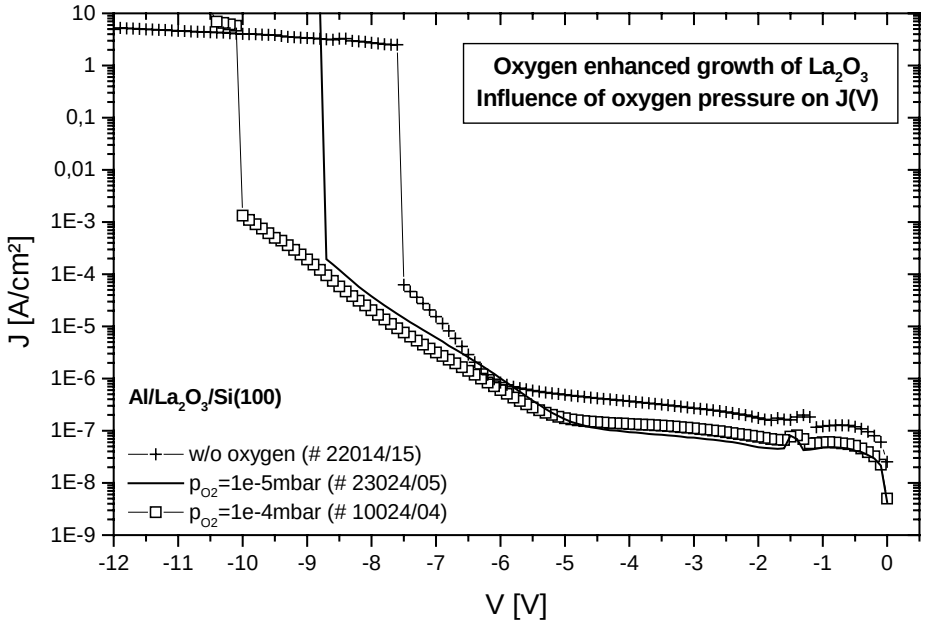


Figure 6.5 Leakage current vs. gate voltage J(V) of MOS capacitors having an 15nm La_2O_3 gate oxide grown under different oxygen partial pressure. Process parameters are reported in table 6-4.

The different oxygen partial pressure do not influence significantly the leakage current of the lanthanum oxide layers deposited by MBD. In particular, samples grown in oxidising ambient show very similar behaviour (straight line and square symbol), while samples grown without additional oxygen have a lightly higher leakage current and lower V_{BD} (4MV/cm compared to 6MV/cm for oxygen enhanced deposition). Similar behaviour has also been reported in literature from other groups working on La_2O_3 deposition [Xiang03].

The leakage current improvement measured for samples grown in oxidising ambient is due to the formation of a thin interface layer between La_2O_3 and silicon substrate, confirmed by XPS analysis.

Further information about the influence and the quality of the interface layers will be given by capacitance vs. voltage measurements illustrate in section 6.2.2.1 of this chapter.

The analysis of the first part of the investigation suggests that a small additional oxygen gas is necessary in order to have a good interface between the high-k and the substrate, but high oxygen pressure will reduces the dielectric constant (ε) of the gate oxide (ε indicated in Table 6-4).

Table 6-4 Study of the influence of oxygen partial pressure La_2O_3 deposition process.

Wafer no.	**Interface Engineering**	**$T_{Substrate}$ [°C]**	**Ambient / Pressure [mbar]**	**$t_{Physical}$ [nm]**	**D_{it} [$eV^{-1}cm^{-2}$]**	**$J_{Leakage}$ @ -1V [A/cm^2]**	**ε**
22014/15	C-burning	600	no additional oxygen	15	$1\cdot10^{11}$	$1\cdot10^{-7}$	20
23024/05	C-burning	600	Oxygen / 1*10-5	15	$1\cdot10^{11}$	$4\cdot10^{-8}$	18
10024/04	C-burning	600	Oxygen / 1*10-4	15	$1\cdot10^{12}$	$6\cdot10^{-8}$	15

6.2.1.3. Current Density-Voltage (J-V) Measurements

Current density vs. voltage characteristics for $Al/La_2O_3/Si$ capacitors are shown in figure 6.6 for 15nm and 22nm La_2O_3 physical thickness, respectively 2.2nm and 4nm EOT.

Lanthanum oxide films have very low leakage currents compared to silicon dioxide (as shown later in this chapter) and a breakdown field around 6MV/cm, which is lightly smaller than silicon dioxide breakdown field (10MV/cm).

As highlighted for aluminium oxide, also UHV-grown lanthanum oxide shows a conduction mechanism that depends on the thickness of the gate dielectric.

Two current regimes can be distinguished in the J(V) characteristics for thicker La_2O_3 layers. At low gate voltages the current density exhibits a plateau. This transient current strongly depends on the delay time (t_{delay}) used for the measurement and on the measuring tool. J(V)-characteristics measured with two different tools and different delay times for the same La_2O_3 sample are illustrated in figure 6.7. Tool number one works with a constant delay time and as a minimum detectable current of $1\cdot10^{-9}A/cm^2$. For the second tool, the delay time decreases with increasing voltage and the detect current limit is smaller than $1\cdot10^{-10}A/cm^2$. The different current characteristics measured for the same La_2O_3 sample are due to charge trapping inside the dielectric layer which modifies the original oxide barrier and influence the leakage behaviour of the dielectric layer.

At higher voltages, MBD-La_2O_3 films present the expected Fowler-Nordheim (FN) Tunneling conduction mode, highlighed by a straight line in the FN-characteristics reported in fig. 6.8. The typical FN plot can be found according to equation (Chapter 3, 3.3.1.4)

$$J = \frac{q^3 E^2}{8\pi h \phi_B} \exp\left(-\frac{8\pi\sqrt{2m^*}\cdot\phi_B^{3/2}}{3hq\cdot E} \right) \rightarrow \ln\left(\frac{J}{E^2}\right) = \ln A + \frac{B}{E}$$

Fixing the value of La_2O_3 barrier height ϕ_B=2.3eV [Wilk01], the extracted effective electron mass for MBD-grown La_2O_3 is $m^*=0.2\ m_0$.

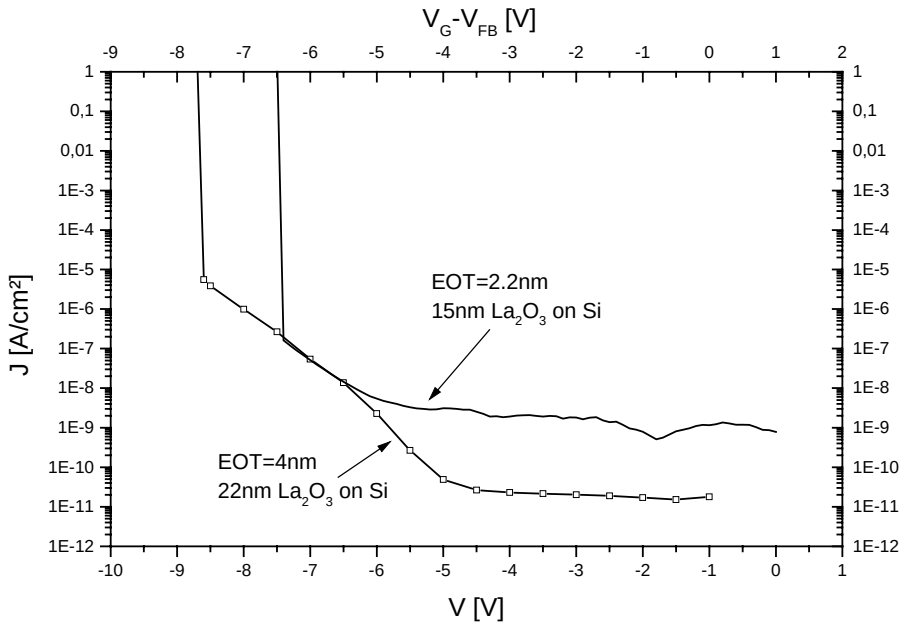


Figure 6.6 J(V) characteristics for Al/La_2O_3/Si(100). EOT=4nm (# 10024/2) and EOT=2.2nm (# 10024/5)

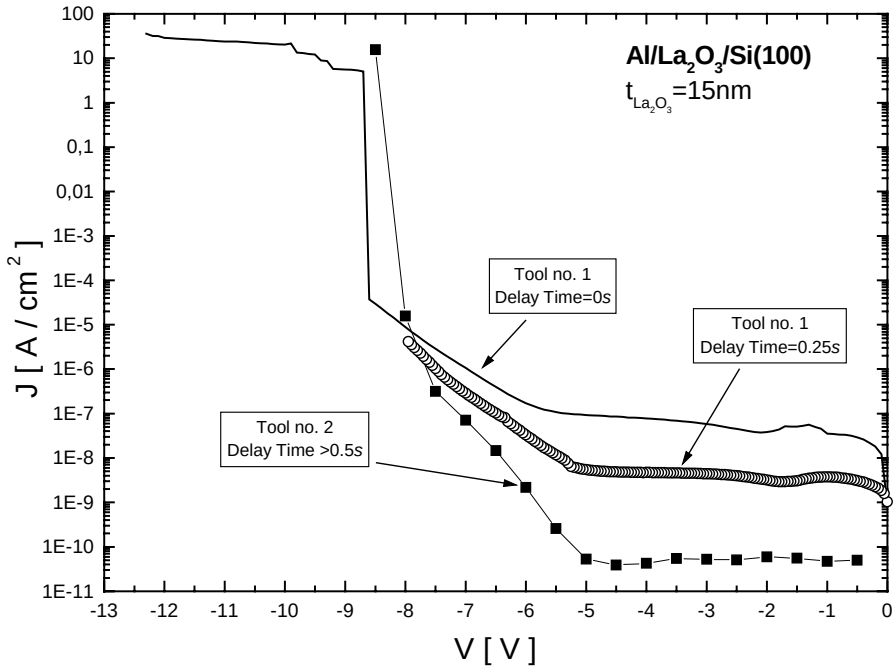


Figure 6.7 J(V) characteristics for Al/La_2O_3/Si(100). Comparison between different measuring tools and delay time (# 10024/5)

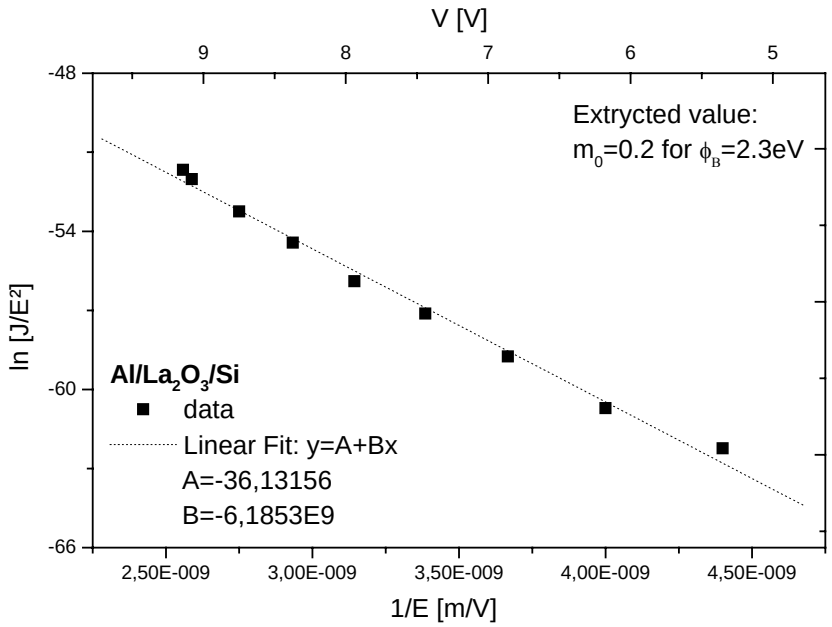


Figure 6.8 Fowler-Nordheim plot of La_2O_3 film (20nm) at high voltage. Straight line characteristic of FN-tunneling

6.2.2. Capacitance vs. Voltage C(V) Measurements

The investigation on the influence of the process parameters and the post-growth annealing on La_2O_3 thin films is studied in detail using capacitance vs. voltage C(V) measurements. C(V) characterisation is used to extract the dielectric constant (ε), equivalent oxide thickness (EOT) and interface state density (D_{it}) of the lanthanum oxide films grown with the optimised process.

6.2.2.1. Influence of oxygen partial pressure on C(V)

The studies on the influence of the oxygen content during La_2O_3 growth introduced in the subsection 6.2.1.2 are now deeply investigated by C(V) characterisation. The capacitance vs. voltage C(V) characteristics for La_2O_3 samples grown with different oxygen pressure are reported in figure 6.9. Process conditions, dielectric constant and equivalent oxide thickness extracted from C(V) measurements are summarised in table 6-5.

La_2O_3 samples grown by MBD without additional oxygen have a higher dielectric constant compared to oxygen enhanced growth, but they also have high hysteresis (fig. 6.9, cross symbol). The capacity measured in accumulation decreases by increasing the oxygen pressure during deposition, which means that the higher the oxygen content the lower is the dielectric constant ε of the deposited layer. This behaviour is due to the formation of an interface layer between the La_2O_3 and the silicon substrate. This layer on one side improves the interface quality (lower hysteresis in C(V) characteristics), on the other side reduces the dielectric constant of the stack.

Based on these studies standard oxygen pressure for successive experiments has been fixed to $p_{O2}=1\cdot10^{-5}$ mbar.

Table 6-5 Study of the influence of oxygen partial pressure La_2O_3 deposition process.

Wafer no.	Interface Engineering	$T_{Substrate}$ [°C]	Ambient / Pressure [mbar]	EOT [nm]	ε
22014/15	C-burning	600	w/o additional oxygen	2.6	20
23024/05	C-burning	600	Oxygen / 1·10-5	3.2	18
10024/04	C-burning	600	Oxygen / 1·10-4	3.8	15

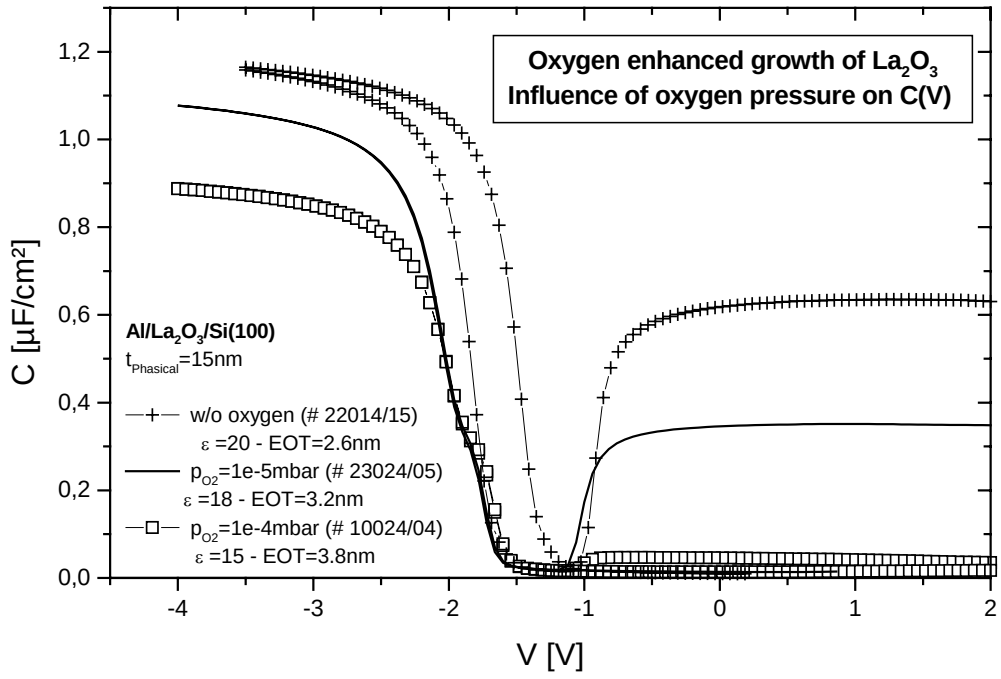


Figure 6.9 Capacitance vs. gate voltage C(V) of MOS capacitors having an 15nm La_2O_3 gate oxide grown under the same process conditions and different oxygen pressure (Table6-2). Hysteresis measurements. Frequecy=20MHz.

6.2.2.2. Influence of the Annealing Temperature on C(V)

Post-growth annealing is a fundamental step for all lanthanum-based dielectrics since as-grown samples have high hysteresis in C(V) characteristics, high flat-band voltage shift (ΔV_{FB}) and high interface state density ($D_{it}=5\cdot10^{12}eV^{-1}cm^{-2}$).

Different annealing methods and condition have been considered in this study. In a first moment, lanthanum oxide films were annealed in furnace, under the same process condition used for Al_2O_3 and Pr_2O_3 samples (nitrogen ambient, 600°C, 30min). Then rapid thermal process (RTP) was applied, in order to study the material behaviour of lanthanum oxide films at higher temperature and to optimise the electrical properties of MBD-grown La_2O_3.

Capacitance vs. voltages C(V) characteristics of lanthanum oxide annealed under different conditions are reported in figure 6.10. After nitrogen annealing in furnace (600°C, 30min) the interface state density of the lanthanum oxide films is one order of magnitude

lower than as-grown samples ($D_{it}=5\cdot10^{11}eV^{-1}cm^{-2}$ instead of $D_{it(as\text{-}grown)}=5\cdot10^{12}eV^{-1}cm^{-2}$), but the hysteresis is still very high.

On the other side, La_2O_3 films RTP annealed at 900°C in nitrogen ambient with 5% oxygen show very low hysteresis, but still have an high interface state density ($D_{it}=2\cdot10^{12}eV^{-1}cm^{-2}$). The dielectric constant of as-grown and furnace-annealed samples is around 20, after RTP annealing becomes 16-19. This reduction is probably dues to a thicker silicon oxide at the interface between silicon substrate and the high-k dielectric.

The effects of post-growth annealing on lanthanum oxide films having a thickness between 15nm and 20nm are shortly summarised:

- As-Grown La_2O_3
  high hysteresis – high D_{it} ($D_{it}=5\cdot10^{12}eV^{-1}cm^{-2}$) – ε=20
- Furnace Annealing (nitrogen, 600°C, 30min)
  high hysteresis – low D_{it} ($D_{it}=5\cdot10^{11}eV^{-1}cm^{-2}$) – ε=20
- RTP Annealing (N_2 + 5%O_2, 900°C, 30s)
  low hysteresis – high D_{it} ($D_{it}=2\cdot10^{11}eV^{-1}cm^{-2}$) – ε=16-19

To combine the effects of the different annealing treatment, after RTP an additional furnace annealing in nitrogen (550°C, 15min) was done. Temperature and time of the furnace treatment were reduced compared with the standard annealing in oven in order to avoid unnecessary growth in thickness of the interface layer while ameliorating its quality (D_{it} reduction).

The influence of the combined annealing on the lanthanum oxide is shown in the C(V) and G(V) measurements reported in figure 6.11. The two-steps treatment reduces the interface state density of one order of magnitude ($D_{it}=2\cdot10^{11}eV^{-1}cm^{-2}$), as the G(V) characteristics highlight, while maintaining the dielectric constant between 18 and 25.

Table 6-6 Influence of post-growth annealing on the electrical properties of La_2O_3.

Post-growth Annealing $t_{Physical}$ = 15 – 20nm	**Hysteresis**	**Dit** [$eV^{-1}cm^{-2}$]	**ε**
As-grown	high	$5\cdot10^{12}$	20-25
Furnace Annealing (N_2, 600°C, 30min)	high	$5\cdot10^{11}$	20
RTP N_2 + 5%O_2 - 900°C, 30s	low	$2\cdot10^{12}$	16-19
RTP (N_2 + 5%O_2 - 900°C, 30s) + Furnace Annealing (N_2, 550°C, 15min)	low	$2\cdot10^{11}$	18-25

The higher dielectric constant measured for some samples is due to a modification of the interface layer, who changes from silicon oxide to La-silicate layer, having higher ε ($\varepsilon_{SiO2}=3.9$, $\varepsilon_{LaSixOy}=10$). The mechanism of this modification is not jet well understood and it is subject of further investigation. This silicate layer has been detected by XPS analysis as illustrated later in this chapter. Although it is reported that La_2O_3 is stable on silicon at equilibrium condition, an interfacial reaction may occur during deposition and post-deposition annealing, which are far from equilibrium. Lanthana film (La_2O_3) can react with a substrate SiO_x interface formed by oxygen diffusion through the La_2O_3 film, to form $(La_2O_3)_x(SiO2)_{1-x}$.

Silicate formations after thermal processing have been reported in many papers concerning lanthanum-based dielectrics [Cheng04, Maria01, Wu02, Copel01].

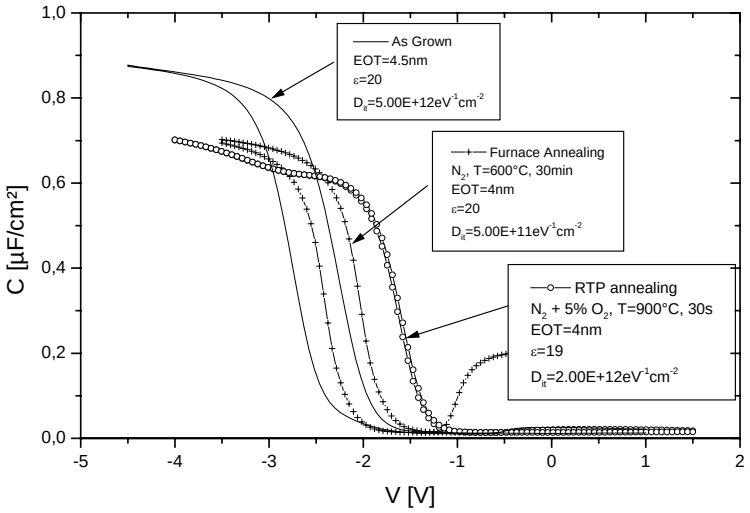


Figure 6.10 Study of the inf#luence of annealing procedure on MBD-grown lanthanum oxide films: straight line: as-grown; cross: furnace annealed (N_2, 600°C, 30 min); circle: RTP anneal (N_2+5%O_2, 900°C, 30s). Hysteresis measurements. Frequecy=20MHz.

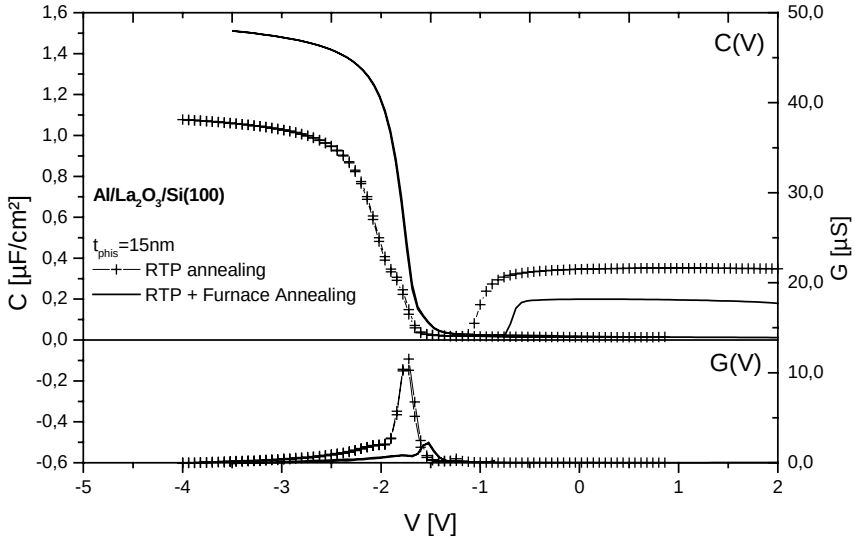


Figure 6.11 Hysteresis C(V) and G(V) curves for Al/La_2O_3/Si(100) capacitors (#10024/5) having 15nm thick La_2O_3 gate oxide and annealed in RTP (cross symbol) and combined RTP + furnace annealing (straight line). Hysteresis measurements. Frequecy=20MHz.

For thinner layers the dielectric constant of La_2O_3 films is reduced, as shown in figure 6.14b. This is principally due to the fact that RTP with N_2 and 5%O_2 leads to the formation of 1.5-2nm interface oxide (or silicate) between silicon substrate and lanthanum oxide, as analysed by TEM and reported later in this chapter. The thinner the La_2O_3 layer, the higher the influence of this interface oxide on the total gate stack dielectric constant.

Another possible explanation to the lower ε measured for thinner La_2O_3 films can be given considering the results published by Wu et al. [Wu02] concerning the characterisation of lanthanum oxide films grown on Si(100). In their paper Wu et all show HRTEM images of 11nm La_2O_3 grown on silicon substrate: after annealing for 2min at 900°C in oxygen nearly all the lanthanum oxide film converts into La-silicate ($LaSi_xO_y$) as confirmed by Auger depth profiles of the film. $LaSi_xO_y$ have a dielectric constant around 10 [Wata03]. HRTEM images and Auger analysis published by Wu et al. are reported in figure 6.12.

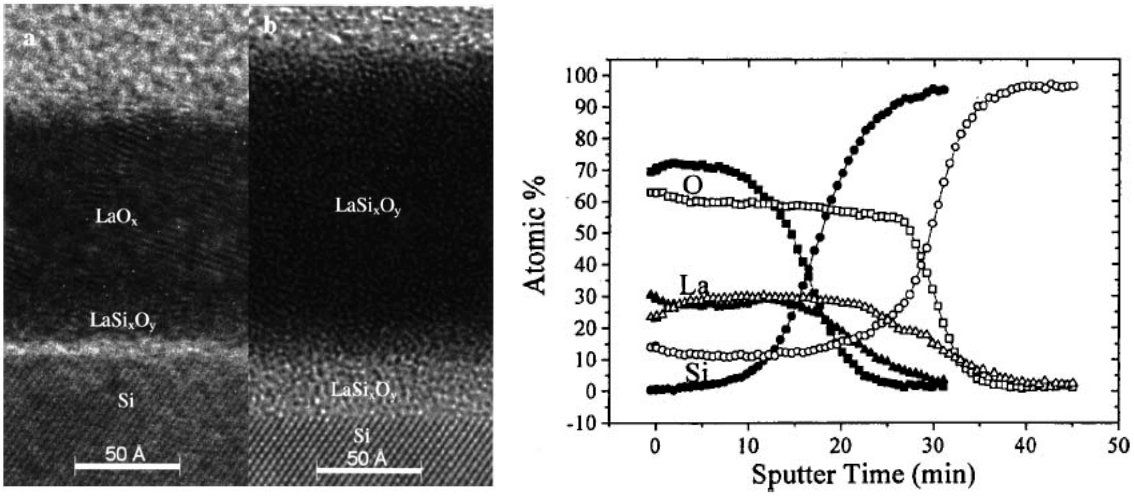


Figure 6.12 11.3nm thick lanthanum oxide film deposited by e-beam evaporation. a) HRTEM images: left) as-deposited and right) annealed at 900°C in oxygen for 2min. b) Auger depth profile: solid symbols are for as deposited film and open symbols are for the film annealed at 900°C in oxygen for 2 min [Wu02].

6.2.2.3. Capacitance vs. Voltage (C-V) characterization of MBD-grown La_2O_3

The capacitance-voltage characteristics for Al/La_2O_3/Si(100) capacitors are illustrated in fig. 6.13. For comparison, the ideal MIS curves for the considered system have been calculated [Sze81, chapter 7]. The comparison between the measurement and the theoretical behaviour shows that MBD-grown La_2O_3 has a nearly ideal C-V shape.

Negligible hysteresis offset, less than 10mV, has been measured for the MBE deposited La_2O_3 films for stress up to –6.5V, being in the same range or lower than literature reported data [He01, Copel01, Guha00].). The conductance peaks are also very low and the estimated interface state density [Brews83] D_{it} value is around $1 \cdot 10^{11} eV^{-1} cm^{-2}$.

Equivalent oxide thickness and flat-band voltage were calculated using the NCSU CVC program [Haus96]. The extracted flat band voltage for a set of sample with different thickness was in the range of –1.5V to –2V. This indicates the presence of positive charge in the deposited film since the expected value for Al/La_2O_3/Si system (Si-substrate resistance of 1–10 Ω·cm) is V_{FB}=-0.8eV. The same effect has been seen in many work concerning the lanthanum-based high-k materials [Peaco03, Velli04, Wata03, Maria01,

Guha00]. The fixed charge could be caused by intrinsic defects, such as vacancies, or extrinsic defects, such as hydrogen [Peaco03]. Hydrogen acts as a shallow donor in many oxides, whereas it is deep in the silicates.

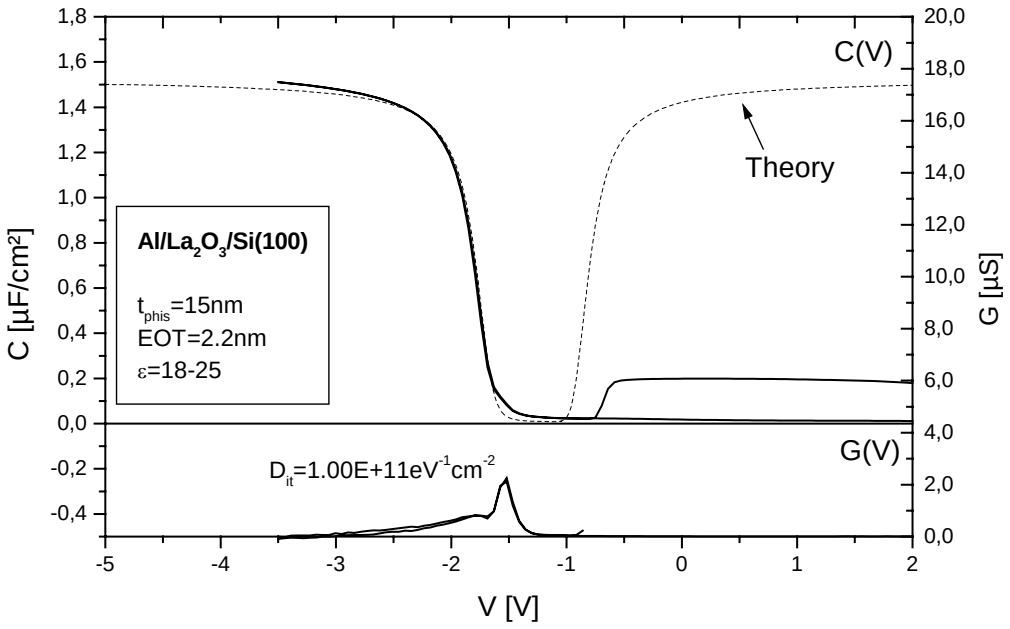


Figure 6.13 Hysteresis C(V) and G(V) curves for Al/La_2O_3/Si(100) - 15nm La_2O_3 gate oxide (# 10024/5). Hysteresis measurements. Frequecy=20MHz.

The dielectric constant ε can be extracted from the EOT vs. Physical Thickness diagram (fig. 6.14a). As introduced in chapter 1 the equivalent oxide thickness is defined as:

$$EOT = \frac{\varepsilon_{SiO2}}{\varepsilon_{high-k}} \cdot t_{physical}$$

where ε_{SiO2} is the dielectric constant of silicon dioxide (ε_{SiO2} =3.9), $\varepsilon_{high\text{-}k}$ and $t_{physical}$ the dielectric constant and the physical thickness of the high-k material, respectively.
$\varepsilon_{high\text{-}k}$ can be written as:

$$\varepsilon_{high-k} = \varepsilon_{SiO2} \cdot \frac{t_{physical}}{EOT}$$

where the ratio EOT/$t_{physical}$ is given by the slope B in figure 6.14. The dielectric constant calculated in this way is 26 and agrees with the ε extracted from capacitance measurements (20-25, depending on the film thickness). The intersection between the EOT axe and the linear fit gives an approximate value of the interface layer between La_2O_3 and silicon substrate of 2nm.

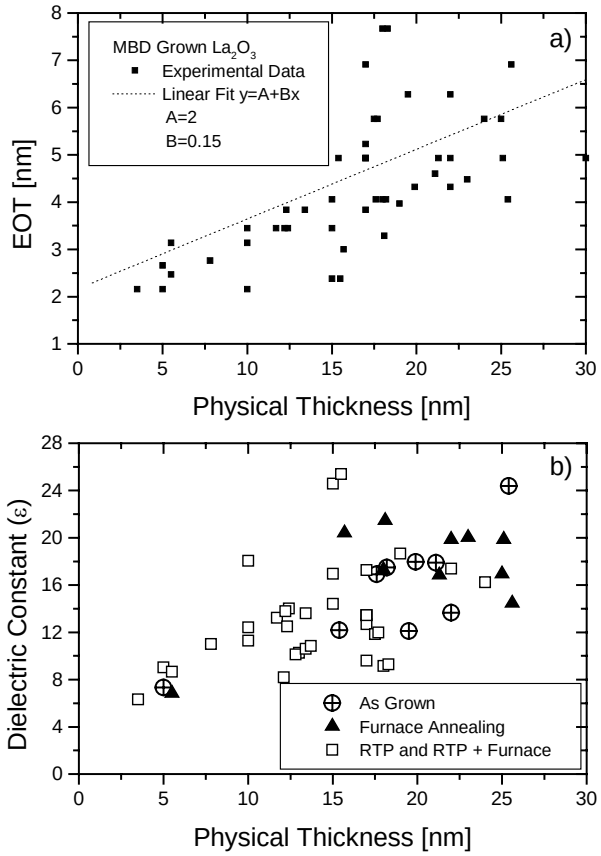


Figure 6.14 Equivalent Oxide Thickness (EOT) vs. Physical Thickness and Dielectric Constant (ε) vs. Physical Thickness of MBD-La_2O_3. a) The slope of the interpolation line gives a dielectric constant of 26. The intersection between the linear fit and the EOT axe gives the thickness of the interface layer (2nm). b) the dielectric constant of the La_2O_3 layer is reduced with the film thickness.

Temperature behaviour of lanthanum oxide thin films have been studied by measuring C(V) for different temperatures. The back-side of the wafer was placed on a hot-chuck plate and capacitance vs. voltage characteristics were measured for the same samples under increasing substrate temperature. The C(V) characteristics are reported in figure 6.15.

At room temperature, the La_2O_3 films show very low hysteresis (less than 10mV). Increasing the hot-chuck temperature the V_{FB} lightly shift to the right-direction and the hysteresis increases. This effect is reversible: when cooling the sample the hysteresis disappears and the V_{FB} returns to the initial value.

The very reactive nature of lanthanum oxide in humid ambient suggests that this temperature behaviour is due to HO^- groups inside the dielectric film. The presence of OH groups enhances the reactivity at the interface between polysilicon and La-dielectrics [Gougo02]. Based on these results it is possible to affirm that although the post-annealing process strongly ameliorate the quality of the lanthanum oxide by reducing the charges present in the deposited layer and at the interface with the silicon substrate (negligible hystestesis in C(V) characteristics and low D_{it}, respectively), the moisture adsorption cannot be completely avoid. As such flat band voltage shift and temperature dependence are still observed in capacitance vs. voltage measurements.

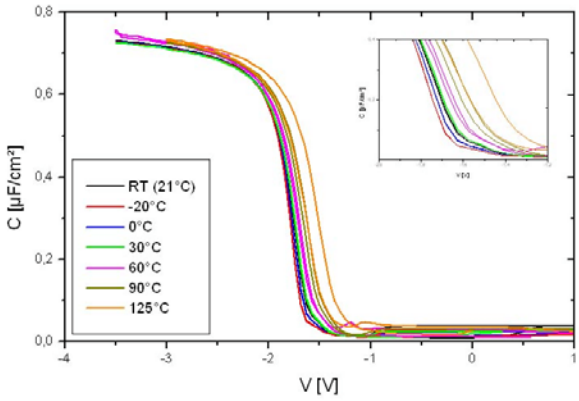


Figure 6.15 Capacitance measurements for different temperature measurements

6.2.3. Comparison of MBD-La_2O_3 with SiO_2 and Literature Data

The leakage current $J_{Leakage}$ measured at V_G-V_{FB}=-1V for MBD-lanthanum oxide grown with the optimised process is compared with the SiO_2, MBD-Al_2O_3, MBD-Pr_2O_3 and La_2O3 literature data.

$J_{Leakage}$ vs. EOT is illustrated in figure 6.16. The direct tunneling curves for SiO_2 and Al_2O_3 have been calculated as explained Section 3.1.3 of Chapter 3. The influence of the measuring tool, as illustrated in subsection 6.2.1.3 of this chapter, has been also highlighted in figure 6.16. If not otherwise specified, the tool used for J(V) measurement was the number 1, which has a minimum detectable current of $1 \cdot 10^{-9} A/cm^2$.

The interface oxide formed during La_2O_3 processing and highlighted in C(V) measurements does not allow to grow lanthanum oxide films with an EOT < 2nm. Lanthanum oxide has a leakage current density which is several orders of magnitude smaller than silicon oxide and it is in the same range of $J_{Leakage}$ for Al_2O_3.

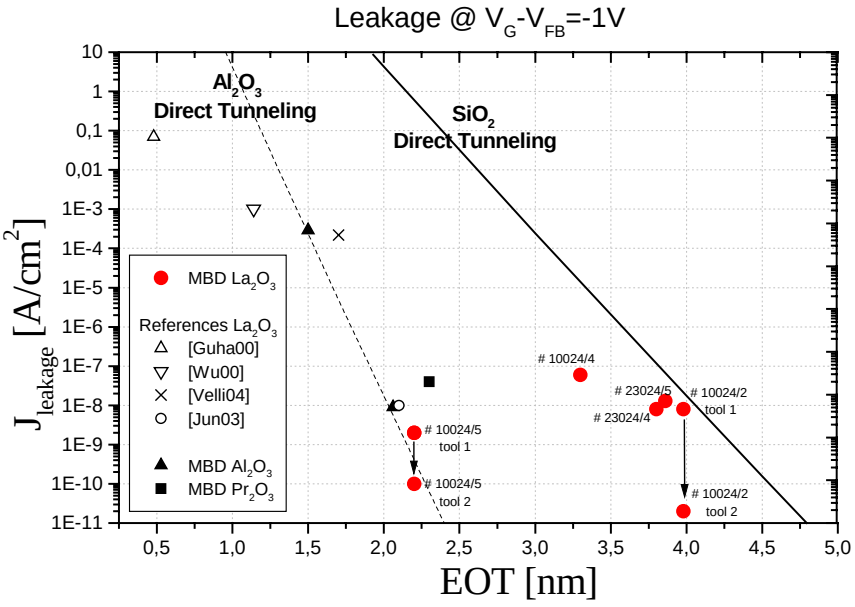


Figure 6.16 Leakage current density vs. EOT of MBE-La_2O_3 compared with SiO_2.

6.2.4. Definition of UHV deposition process for La_2O_3

The investigation on lanthanum oxide reported in this chapter lead to the following definition of the main process parameters for the MBD of La_2O_3 on silicon substrate

Table 6-7 UHV deposition of La2O3

Process	Process Parameters
RCA-cleaning	
HF-last (HF:H_2O=1:100)	t=35s
C-Burning	$T_{Substrate}$=550°C $p_{O2}=1\cdot10^{-5}$mbar t=30min
MBD-La_2O_3	oxygen enhanced deposition $T_{Substrate}$=600°C $p_{O2}=1\cdot10^{-5}$mbar
Post-growth annealing	1-step: RTP Ambient: N_2 + 5%O_2 T=900°C t=30s 2-step: Furnace Annealing Ambient: N_2 T=550°C t=15min

6.3. Physical Analysis of MBD-grown La_2O_3 thin films

Lanthanum oxide thin films grown by molecular beam deposition have been analysed using different techniques in order to study the film composition and stoichimetry. In particular, chemical composition and physical structures of the gate stacks were studied by means of X-ray Photoelectron Spectrometry (XPS), Rutherford Back Scattering Spectrometry (RBS) and high-resolution Transmission Electron Microscope (TEM). The physical principle of these analysis methods are reported in chapter 2.

6.3.1. XPS

Composition and stoichiometry of the lanthanum oxide were studied by X-ray Photoelectron Spectroscopy (XPS). The XPS analysis was performed in an ultrahigh vacuum Omicron XPS-system (base pressure $5\cdot10^{10}$mbar) equipped with an hemispherical electron energy analyser (EA 125) and a DAR 400 twin-anode X-ray source, where the X-ray source can be chosen between Al Kα (energy 1486.6eV) and Mg Kα (energy 1253.6eV). Since the Mg Kα has a smaller full width at half maximum (FWHM)[Omicron], e.g. a better analysis resolution, the Mg-anode was only used for the measurements. A piece of 0.8cm×1.5cm was cut from the centre of the sample for analysis.

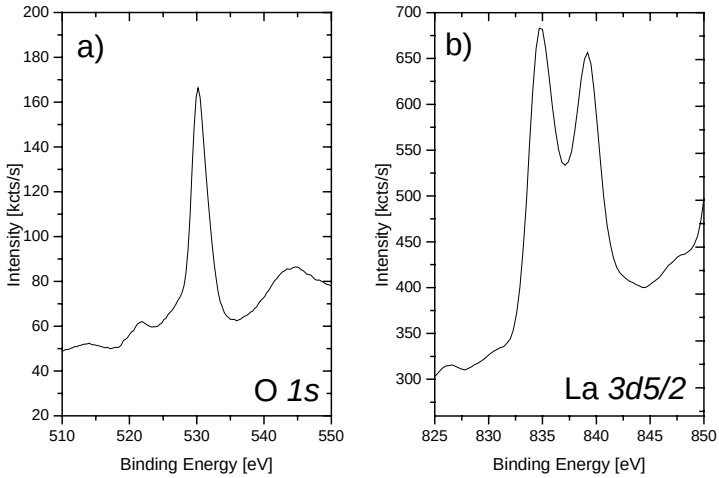


Figure 6.17 a) O 1s and b) La 3d5/2 XPS core- level spectra for 25nm La_2O_3 grown by MBD (#10024/2)

Since the lanthanum oxide get in contact with air during transport from MBE deposition system to the XPS-system, before to start the analysis the surface of the sample was sputtered with argon ions in order to eliminate the possible carbon contamination. Fig. 6.17 shows the XPS O *1s* and La 3*d5/2* peaks of 25nm-thick La_2O_3. The binding energy (BE) of the O 1*s*-peak is 530eV, and the one of La *3d5/2* is 835eV, corresponding to oxygen and lanthanum in La_2O_3 [Uwa84]. The binding energies of core levels are calibrated by setting the carbon 1s peak at 284.7eV (surface scan).

In order to determine the homogeneity of the deposited La_2O_3 thin films, the XPS measurements have been repeated on the same sample for different depths starting from the surface up to the interface between the dielectric and the silicon substrate. This kind of measurement was done by alternating argon sputtering with XPS analysis. The element percentage vs. sputtering time is reported in figure 6.20. It is interesting to note that the interface layer between the lanthanum oxide and the silicon substrate have a stoichiometry very close to silicate measured by [Wu02] and illustrated in figure 6.12b, open symbols.

In figure 6.18 the silicon peak is shown. Since the La 4*d* overlap the Si 2*p*, typically taken as reference peak for silicon (BE around 100eV), here the Si 2*s* is used to study the silicon content in the deposited film. The XPS spectrum evidences two peaks in the silicon region: inside the film (Fig. 6.18, dot line), the mean peak corresponds to silicon with Si-O bonding less than 7% of the element percentage) while a very small one correspond to Si-Si bonding (around 1% of the element percentage). At the interface between dielectric and substrate, the predominant peak is the Si-Si (substrate) but still a 9% of silicon having Si-O bonding is present in the film. As confirmation for the formation of a thin lanthanum silicate at the interface with the silicon substrate the La 3*d* and O 1*s* peaks are considered. La 3*d* and O 1*s* positions are consistent with La-O bonding, but a slight shift can be seen near the interface between the dielectric and the silicon substrate (figure 6.19): close to the interface the La 3*d* and O 1*s* peak moves to higher binding energy, thus indicating a La-O-Si bonding [He01]. Moreover this conclusion is confirmed by the O 1*s* the peak position at 532eV, which lies between La_2O_3 (530eV) and SiO_2 (533eV) indicating La-Si-O binding [Li03, Cheng04].

The stoichiometry of the deposited layer can be calculated from the major line peaks La *3d5/2* and the O 1*s* resulting in an La to O ratio of 0.67 ± 0.01 near the surface and 0.50 ± 0.01 close to silicon substrate (due to the SiO_x interface layer).

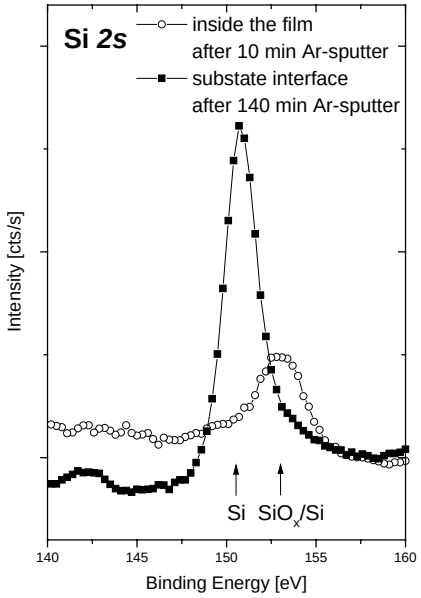


Figure 6.18 Si 2s core- level spectra for 25nm La_2O_3 MBE-grown. Circles indicate the silicon peak inside the deposited film. Squares indicate the silicon peak at the interface between the dielectric layer and the silicon substrate (#10024/2)

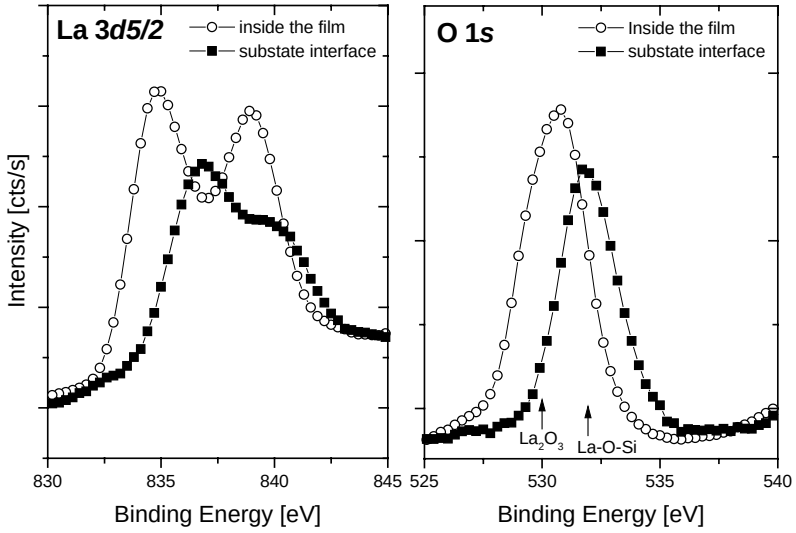


Figure 6.19 La 3*d5/2* and O 1*s* core- level spectra for 25nm La_2O_3 MBE-grown. Circles indicate the spectrum inside the deposited film and squares the spectrum at the interface between the dielectric layer and the silicon substrate (#10024/2)

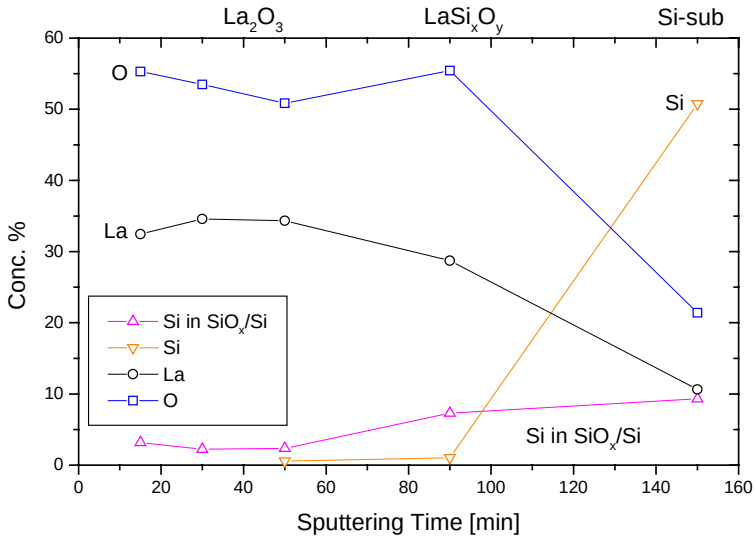


Figure 6.20 XPS depth profile of 25nm La_2O_3. Element concentration. The interface layer between the lanthanum oxide and the silicon substrate have a stoichiometry very close to La-silicate measured by [Wu02] after annealing of 11nm La_2O_3 in oxygen at 900°C for 2 min and illustrated in figure 6.12b, open symbols.

6.3.2. RBS

RBS analysis of a 20nm lanthanum oxide layer is depicted in fig. 6.21. The simulation fits the measurement for a gate stack given by LaO_3 and a thin SiO_2 at the interface between silicon and high-k. No carbon contamination can be seen.

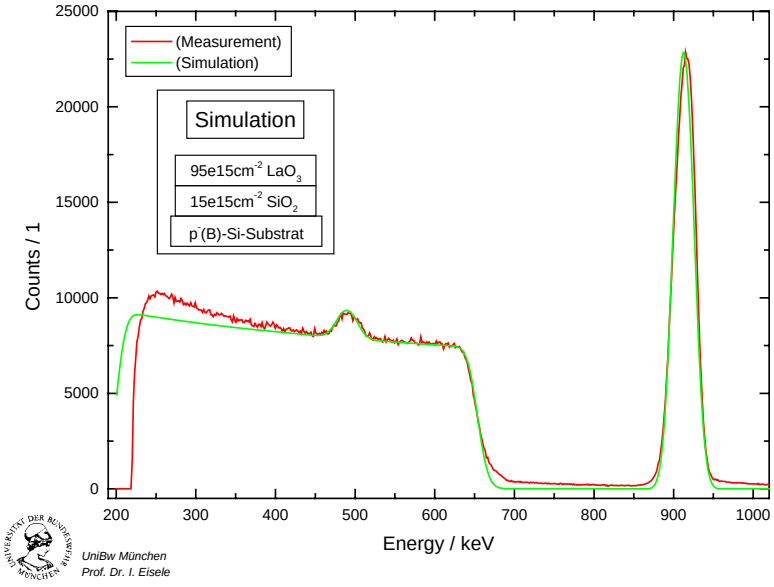


Figure 6.21 RBS spectrum of 25 nm La_2O_3 MBE-grown on silicon substrate

6.3.3. TEM

High-Resolution TEM analysis of La_2O_3 films have been performed. The La_2O_3 film has an interface oxide thicker than expected and a total thickness that is very close to the ellipsometer measurements. The lanthanum oxide was grown on a silicon wafer after C-burning. It is known than this thermal treatment in oxygen ambient causes the growth of a nearly 0.5nm SiO_x layer between the lanthanum oxide and the silicon substrate (see Chapter 4: "Interface Engineering"). During process deposition and post-growth annealing, the lanthanum oxide reacts with the silicon oxide and a thicker $(La_2O_3)_x(SiO2)_{1-x}$ layer is formed. The final structure will be given by a gate stack in which the lanthanum oxide film is separated from the silicon substrate by a 2nm-thick interface layer (brighter layer in figure 6.22).

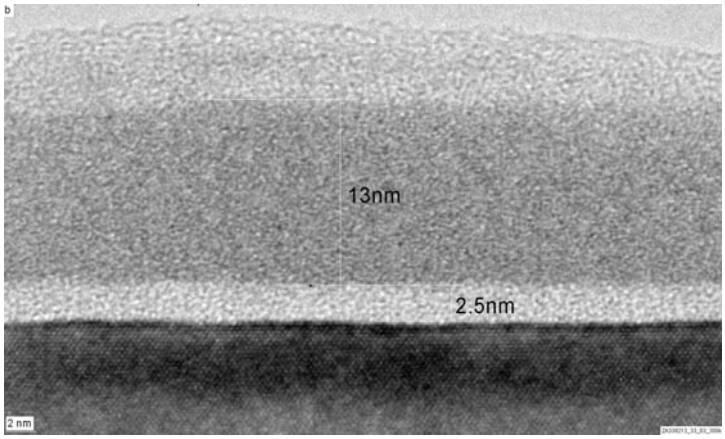


Figure 6.22 TEM analysis of La_2O_3 on Si(100) substrate. The lanthanum oxide has been grown on silicon substrate after C-burning (#10024/5).

6.4. Interface Engineering

The influence of the interface preparation before La_2O_3 deposition has been studied. Lanthanum oxide films have been grown on silicon wafers after thermal desorption of the chemical oxide and after C-burning. The differences between the two preparation methods have been studied by TEM analysis and are reported.

Thermal desorption

High-Resolution TEM analysis have been performed on lanthanum oxide layers grown on silicon substrate after thermal desorption (900°C, 5min). The analysis has been done by Infineon Technologies [ref. 20040639].

The investigated structure $Al/La_2O_3/Si$ presents an extremely rough interface (figure 6.23 a), due to carbon still presents on the silicon surface before La_2O_3 deposition. The upper part of the lanthanum oxide seems to be polycrystalline while the lower part (close to the interface with substrate) amorphous (figure 6.23b).

C-burning

Carbon burning was introduced to remove the carbon contamination presents on the silicon wafer after cleaning and transport to the MBD process chamber. As reported in chapter 3, during this temperature treatment of the silicon surface in oxygen ambient, a thin

silicon oxide layer (around 0.5nm) is formed. This layer can be eliminated by thermal desorption, but a rough surface will results. The 0.5nm SiO_x layer was left on the wafer and La_2O_3 was deposited on it. TEM analysis of lanthanum oxide films deposited after C-burning on silicon substrate are reported in figure 6.24. The wide view shows a very smooth interface between gate oxide and silicon substrate (figure 6.24 a). A closer view show a 2nm thick interface oxide under 13nm La_2O_3. The lanthanum oxide does not present any preferential structure hence it can be deduced that the film is still amorphous after RTP annealing at 900°C. The combination of C-burning and MBD deposition results a stable system which is still amorphous at high temperature annealing.

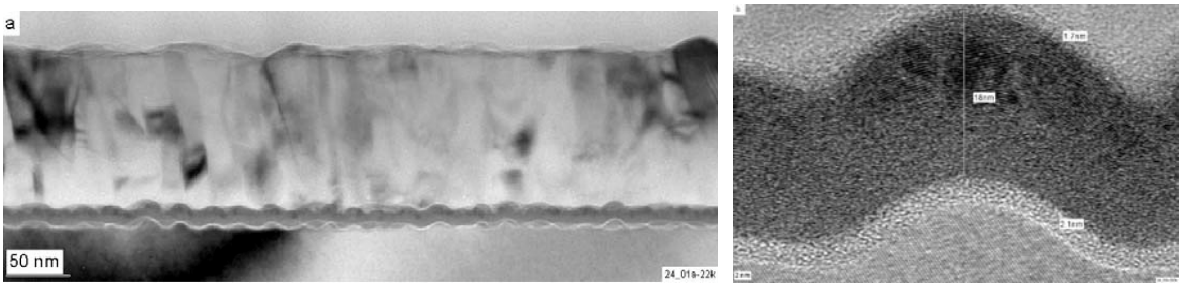


Figure 6.23 TEM analysis of La_2O_3 thin film deposited on silicon substrate after thermal desorption of the chemical oxide (10024/2)

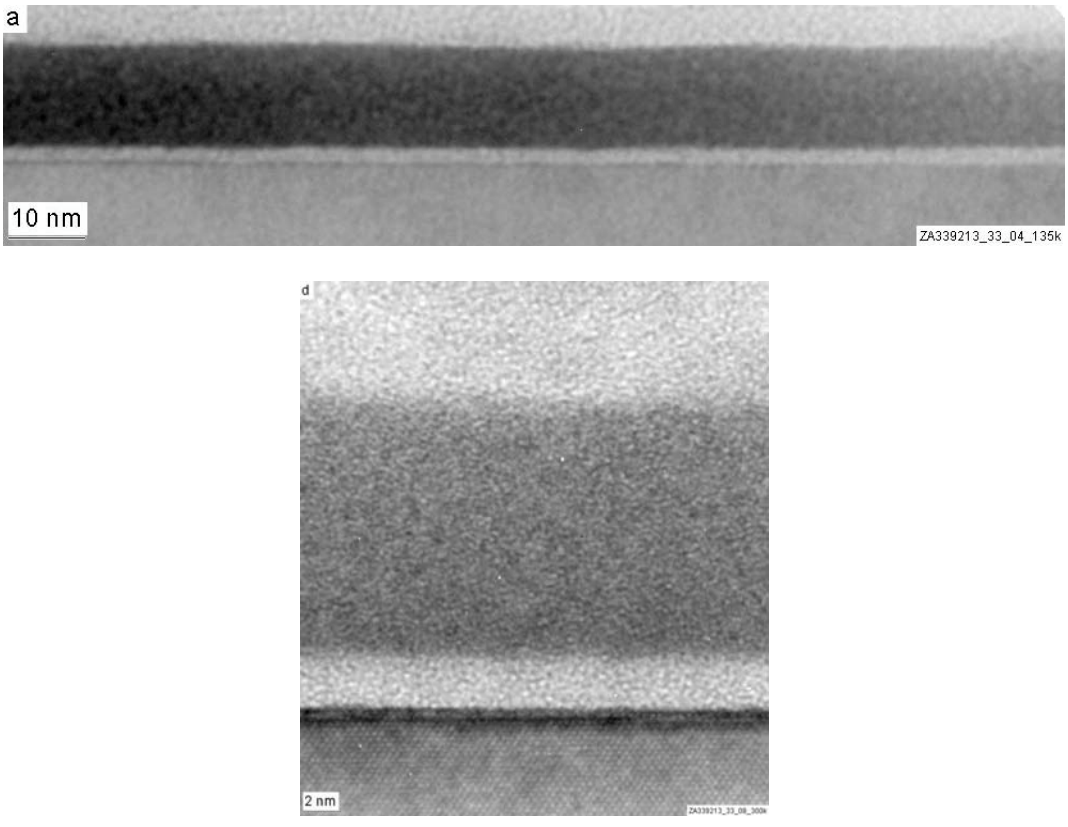


Figure 6.24 TEM analysis of La_2O_3 thin film deposited on silicon substrate after C-burning (#10024/5).

6.5. Conclusion

In this chapter it was shown that lanthanum oxide is a very promising material as gate oxide for sub-100nm technology. The high dielectric constant and the thermal stability to high temperature (900°C) let foresee a possible process integration in CMOS technology.

Molecular beam deposition of lanthanum oxide on silicon substrate as alternative gate oxide has been investigated and the process deposition optimised for UHV-system.

The influence of the different MBD-process parameters on the La_2O_3 films and the post-growth annealing were studied using electrical characterisation of $Al/La_2O_3/Si$.

MBD La_2O_3 samples grown with the optimised deposition and annealing processes have a leakage current density which is several orders of magnitude smaller than silicon oxide at the same equivalent oxide thickness and stay in the range of aluminium oxide. The high oxygen diffusion inside the lanthanum oxide film and the sample preparation process (C-burning, MBD in oxygen, annealing in nitrogen and oxygen) lead to the formation of an interface layer which hinders the deposition of La_2O_3 having EOT smaller than 2nm.

The dielectric constant measured for gate stacks having La_2O_3 film 15 – 20nm thick was in the range ε=18-25. The higher dielectric constant measured for part of the samples is due to a modification of the interface layer, who changes from silicon dioxide to La-silicate, having higher ε. The reaction process which leads to the modification of the interface between dielectric and silicon substrate is subject of further investigation.

The main problem highlighted for lanthanum oxide is its high sensibility to humidity. The moisture adsorption leads to film degradation which can be reduced by an optimised post-growth annealing process. Particular attention should also be paid to the interface engineering. Reducing the influence of the interface layer by growing a very thin silicon nitride film before lanthanum oxide deposition can be a promising way to achieve low leakage currents for EOT smaller than 2nm.

Chapter 7

Conclusion and Outlook

The research reported in this thesis concerns with the investigation of alternative gate dielectrics for replacing silicon dioxide as gate dielectric in CMOS technology. This work was financially supported by Infineon Thechnology AG (Munich, Germany).

The first part of the thesis focuses on aluminium oxide thin films grown by MBD. The influence of the different process parameters on the properties of the UHV-grown Al_2O_3 have been analysed and the deposition optimised. Capacitance vs. voltage measurement highlights the formation of a thin interface oxide between Al_2O_3 film and silicon substrate which causes the reduction of the dielectric constant of the gate stack. The composition of gate stack was studied by XPS analysis. The stoichiometry of the deposited film was $Al_{(2\pm0.1)}O_{(3.2\pm0.1)}$, with a thin SiO_x interface layer. Current density and capacitance vs. voltage characterisation of $Al/Al_2O_3/Si$ capacitors confirm the good electrical properties of the MBD aluminium oxide. In particular, the high quality of the interface was proved by the low interface state density D_{it} extracted from G(V) measurements. The leakage current density of Al_2O_3 samples grown with the optimised deposition and annealing process was several orders of magnitude smaller than silicon oxide at the same equivalent oxide thickness and stays in the range of the best reported literature values.

After having concluded the studies on aluminium oxide, praseodymium oxide (Pr_2O_3) and lanthanum oxide (La_2O_3) have been considered as alternative gate dielectric because of their high dielectric constant (20-30) and thermal stability on silicon substrate until 1000K.

First of all, the possibility to grow praseodymium oxide thin films on silicon substrate by molecular beam deposition has been investigated. The influence of the different process parameters on the Pr_2O_3 films and the material source used for e-beam evaporation were deeply studied by electrical characterisation of $Al/Pr_2O_3/Si$ capacitors. Electrical characterisation by J(V) and C(V) measurements highlight that praseodymium oxide is a very critical system, highly temperature dependent and strongly influenced from the ambient moisture. Temperature studies on $Al/Pr_2O_3/Si$ capacitors have shown the low thermal stability of the praseodymium oxide, who starts to crystallise already at low temperature and easily changes its stoichiometry. This instability and the critical deposition process excludes Pr_2O_3 from the interesting candidate for alternative gate dielectric in CMOS technology.

A very promising candidate to substitute silicon dioxide as gate dielectric is the La_2O_3-system. Lanthanum oxide has been investigated because of its high dielectric constant, resistance to crystallisation, appreciable high band gap and band-offset with respect to silicon and thermal stability to high temperature (900°C) which let foresee a possible process integration in CMOS technology.

The MBD-growth of lanthanum oxide films on silicon substrate have been optimised taking into consideration the influence of the different process parameters on the electrical characteristics of the deposited layers.

Capacitance vs. voltage measurements of Al/La_2O_3/Si MOS structures have highlighted that as grown lanthanum oxide is characterised by high hysteresis and interface state density. Post-grown annealing strongly ameliorates the electrical properties of La_2O_3 films. Different annealing methods and conditions have been considered in order to optimise the quality of the deposited films and their influence on MBD-lanthanum oxide films have been reported.

The leakage current density measured for La_2O_3 samples grown with the developed deposition and annealing processes is several orders of magnitude smaller than silicon oxide at the same equivalent oxide thickness and stay in the range of aluminium oxide. Physical analysis (XPS, RBS and TEM) showed the formation of a 2nm interface layer between lanthanum oxide and silicon substrate which hinders the deposition of La_2O_3 having EOT smaller than 2nm. This interface layer is principally due to the high oxygen diffusion inside the lanthanum oxide film and to the sample preparation itself (C-burning, MBD in oxygen, annealing in nitrogen and oxygen).

La_2O_3 gate stacks with a physical thickness of 15 – 20nm show a dielectric constant in the range ε=18-25. The investigation of the samples having the highest dielectric constant showed that the higher ε is due to a modification of the interface layer, which changes from silicon dioxide to La-silicate. Based on this observation, further research was started on the reaction process which leads to the modification of the interface between dielectric and silicon substrate.

The main focus of the work on lanthanum oxide was the persisting sensibility to humidity. The resulting film degradation through moisture adsorption until now prohibits lanthanum oxide as alternative gate oxide. The idea was to reduce this degradation through optimisation of the post-growth annealing process. But even if the developed post-growth annealing process showed significant improvements of the quality of the lanthanum oxide by reducing the charges present in the deposited layer and at the interface with the silicon substrate (negligible hystestesis in C(V) characteristics and low D_{it}, respectively), the results of this thesis clearly indicate that moisture adsorption cannot be completely avoided. To solve this problem, ternary systems like La-silicate and La-aluminate have to be taken into consideration for future investigations.

La-silicates (LaSiO) are somehow interesting materials because of their improved resistance to moisture compared to lanthanum oxide and their higher crystallisation temperature. But this system has low dielectric constant (ε around 10). Therefore La-silicates can only be a short term solution to the problem of the alternative gate oxide.

A few promising publications on lanthanum aluminate (LAO) were the reason to direct the research effort rather to this system. Here the important outcome was that the high dielectric constant typical of lanthanum oxide (ε_{LAO}=25) could be maintained when improving the resistance against moisture adsorption by adding some aluminium to La_2O_3 which reduces the oxygen diffusivity inside the film.

The presented research suggests that for future investigation on lanthanum based dielectrics for gate applications the LAO-systems is the most promising candidate. A big potential was shown to be in interface engineering and post-growth annealing. Low leakage currents for EOT smaller than 2nm should be achievable by reducing the influence of the interface layer by growing a very thin silicon nitride layer before lanthanum oxide or LAO deposition.

Bibliography

[Ahme00] K. Ahmed et al.; "Comparative Physical and Electrical Metrology of Ultrathin oxides in the 6 to 1.5 nm regime", IEEE Trans. Elect. Devices, vol. 47, no. 7, July 2000

[Alme00] R. M. C. de Almeida et al., Phys. Rev. B 61, 12992 (2000)

[Alme03] R. M. C. de Almeida et al., "Reaction-diffusion in high-k dielectrics on Si"; Surface Science Reports 49, pp. 1-114 (2003)

[Auge25] P. Auger, J. Physique Radium 6 (1925), 205

[Baum03] H. Baumgaertner, Seminar on the electrical characterisation of MIS diodes, UniBW-München

[Bird89] J.R. Bird and J.S. Williams, „Ion Beams for Materials Analysis"; Academic Press, 1989, pp. 104-106

[Blank] O. Blank, Infineon Project Report - 15 April 2003

[Brews83] J.R. Brews, „Rapid interface parameterisation using a single MOS conductance curve", Solid-State Electronics Vol. 26, no. 8, 1983

[Brig85] D. Briggs and M.P. Seah, „Practical Surface Analysis by Auger and X-ray Photoelectron Spectroscopy", John Wiley & Sons, page 94, 1985

[Buch99] D. A. Buchanan, "Scaling the gate dielectric: material, integration and reliability", IBM J. Res. Develop., Vol. 43, pp. 245-264, 1999

[Burnham68] D.A. Burnham et al., "Phase transformations in the praseodymium oxide-oxygen system: high-temperature X-ray diffraction studies", J. Phys. Chem., vol. 72, no. 13, pp. 4415-4424, December 1968

[Carter01] Carter et al.,"Electrical Characterization of high-k materials prepared by atomic layer CVD", IWGI 2001, pp.1-6, Tokyo

[Cheng04] J.B. Cheng et al., "Growth and characterization of La2O3 gate dielectrics prepared by low pressure metalorganic chemical vapor deposition", Appl. Surf. Sci., 233, pp. 91-98, 2004

[Chin99] Chin et al .; Symp. on VLSI Tech. (1999)

[Chin00] A. Chin, "High quality La2O3 and Al2O3 gate dielectrics with equivalent oxide thickness 5-10Å", Symp. VLSI Tech., 2000

[Copel01] M. Copel et al., "Formation of stratified lanthanum silicate dielectric by reaction with Si(001)", Appl. Phys. Lett., vol 78, no. 11, March 2001

[Dabr00] J. Dabrowski and H.-J. Müssig; „Silicon Surfaces and Formation of Interfaces";p. 37, World Scientific Publishing, 2000

[Do99] T. Do et al., "Pressure effects on aluminium oxidation kinetiks using X-ray photoelectron spectroscopy and parallel factor analysis", Surf. Sci. 440, pp. 438-450, 1999

[Edge04] L. F. Edge, “Suppression of subcutaneous oxidation during the deposition of amorphous lanthanum aluminate on silicon”, Appl. Phys. Lett, no. 84, vol. 23, June 2004

[Fissel02] A. Fissel et al., “Photoemission and *ab initio* theoretical study of the interface and the film formation during epityxial growth and annealing of praseodymium oxide on Si(001)”, J. Appl. Phys., vol. 91, no. 11, June 2002

[Frenk38] J. Frenkel, “On the theory of electric breakdown of dielectrics and electronic semiconductors”, Technical Physics of the USSR, 1938.

[Fuku96] T. Fukuda et al., “Crystallization and Growth of g-Al2O3 in a film prepared by sol-gel method”, Tech. Rep. of the Osaka Univ., vol. 46, no. 2251, pp. 173-179, 1996

[Gory03] A. Goryachko et al, ”Stability of Pr2O3 films grown on Si(100) substrate”, J. Vac. Sci. Technol. A 20(6), Nov/Dec 2002

[Gougo02] T. Gougousi et al., “The role of OH species in high-k/policristalline silicon gate electrode interfacial reactions”, Appl. Phys. Lett., vol. 80, no. 23, June 2002

[Gray96] Struan M. Gray, Mikael K.-J. Johansson, Lars S.O. Johansson, J.Vac.Sci.Tech. B 14 (1996) 1043

[Grundy01] A. N. Grundy et al., “Thermodynamic Assestement of the Lanthanum-Oxygen system”, J. Phase Equilibria, vol. 22, no. 2, 2001

[Guha00] S. Guha et al., “Atomic beam deposition of lanthanum- and yttrium-based oxide thin films for gate dielectrics”, Appl. Phys. Lett., vol 77, no 17, October 2000

[Guha01] Guha et al, “High-quality aluminium oxide gate dielectrics by ultra-high-vacuum reactive atomic-beam deposition”, J. Appl. Phys., vol. 90, no. 1, July 2001

[Gusev01] Gusev et al., “Ultrathin high-k gate stacks for advanced CMOS devices”, IEEE 2001

[Haef87] R.A. Haefer, “Oberflächen- und Dünnschichttechnologie, Teil I: Beschichtungen von Oberflächen, Reihe: WFT Weststoff-Forschung und –Technik, Bd. 5, Springer-Verlag, Berlin, 1987

[Haus96] J. Hauser, CVC 1996 NCSU Software, Dept. Elect. Comput. Eng., North Carolina State Univ., Raleigh, NC

[He01] W. He et a., Electrochemical and Silid-State Letters, 7 (7) G131-133 (2001)

[He04] W. He et al. “Atomic layer deposition of lanthanum oxide films for high-k gate dielectrics”, Electrochemical and Solid-State Letters, 7(7) G131-G133, 2004

[Herm89] M. A. Herman and H. Sitter, “Molecular Beam Epitaxy”, Springer-Verlag, 1989

[Hide66] B.G. Hyde, “On the praseodymium + oxygen system”, Phil. Trans. Roy. Soc. London, Ser. A, vol. 259, pp. 583-614, May 1966

[Hubba96] K.J. Hubbard et al., “Thermodynamic stability of binary oxides in contact with silicon”, J. Mater. Res., vol. 11, no. 11, Nov 1996

[Huff05] H. R. Huff and D. C. Gilmer, “High dielectric constant materials: VLSI MOSFET Applications”, Springer-Verlag, Berlin 2005

[Iwai02] H. Iwai et al. “Advanced gate dielectric materials for sub-100nm CMOS”, IEDM Tech. Dig., 2002

[Inf_rep] Analysis Report – Pr2O3 on Silicon, Structural Characterization, Rep. No. 20030080

[ITSR] “International Technology Roadmap for Semiconductor - 2004 Update – Process Intergation, Devices, and Structures”, Semiconductor Industry Association – SIA, Austin, 2004

[Jun02] J. H. Jun et al., “Structural and electrical properties of La_2O_3 thin film as a gate dielectric”, J. Kor. Phys. Soc., vol. 11, no. 6, December 2002

[Jun03] J. H. Jun et al., “Properties of lanthanum aluminate thin film deposited by MOCVD”, Electrochemical and Solid-State Lett., 6 (11) F37-F39, 2003

[Kang02] S-W. Kang, “Deposition of La2O3 films by direct liquid injection metallorganic chemical vapor deposition”, J. Electr. Soc., 149(6), C345-C348, 2002

[Kim02] J. Kim, “Improvement in electrical insulating properties of 10-nm-thick Al2O3 film grown on Al/TiN/Si substrate by remote plasma annealing at low temperatures”, Appl. Phys. Letters, Vol. 80, no. 15, pp. 2734-2736 (2002).

[Krug00] “Atomic transport and chemical stability during annealing of ultrathin Al_2O_3 films on Si”, C. Krug et al., Physical Review Letters, vol. 85, no. 19, pp. 4120- 4123, November 2000 (00prl11-krug)

[Kundu02a] M. Kundu et al., “Effect of oxygen pressure on the structure and thermal stability of ultrathin Al2O3 films on Si(100)”, J. Appl. Phys.; vol. 91, no. 1, pp. 492-500, January 2002

[Kundu02b] M. Kundu et al, “Investigation of the effect of high temperature annealing on stability of ultrathin Al2O3 films on Si(001)”, J. Appl. Phys.; vol. 92, no. 4, pp. 1914-1921, August 2002

[Kundu03] M. Kundu et al., “Interface stability during the growth of Al2O3 films on Si(001)”, J. Appl. Phys.; vol. 93, no. 3, February 2003

[LB] Landolt-Börnstein, “Phase Equilibria, Crystallographic and Thermodynamic data of Binary Alloys”, Group IV - Volume 5

[Levi85] E.M. Levine et al., *Phase diagram for Ceramists*, The American Society, Columbus, OH, vol.2, 1985

[Li03] A.-D. Li et al., “Characterization of LaAlO3 gate dielectrics on Si grown by metalorganic chemical vapor deposition”, Appl. Phys. Lett., vol. 83, no. 17, October 2003

[Liu01] J. P. Liu et al. “Epitaxial growth of Pr_2O_3 on Si(111) and the observation of a hexagonal to cubic phase transition during postgrowth N_2 annealing”, Appl. Phys. Lett., vol. 79, no. 5, July 2001

[Lu04] X. B. Lu et al., “Thermal stability of LaAlO3/Si deposited by laser molecular-beam epitaxy”, Appl. Phys. Lett., vol. 84, no. 14, April 2004

[Machanda98] L. Machanda et al, Proc. Int. Electron Device Meet. Dig. 1998, p.605

[Maria01] J.-P. Maria et al., “High temperature stability in lanthamun and zirconia-based gate dielectrics”, J. of Applied Physics, vol. 90, no. 7, October 2001

[Mereu04] B. Mereu et al. “Electrical properties of metal-oxide-silicon structures with LaAlO3 as gate oxide”, Mat. Sci. Eng. B, 109, pp. 94-98, 2004

[Moore75] Gordon E. Moore, “Progress in Digital Integrated Electronics”, IEDM, 1-3 Dec. 1975, Washington; D.C., USA

[Mussig02] H.J- Müssig et al., “Initial stages of praseodymium oxide film formation on Si(001)”, Surf. Science 504, pp. 159-166, 2002

[Neu98] A. Neubecker, “Ultrahochvakuum (UHV)-kompatible Herstellung von Niedertemperaturoxiden für die Mikroelektronik”, PhD, February 1998

[Nico82] E. H. Nicollian and J.R. Brews, “MOS (Metal Oxide Semiconductor) – Physics and Thecnology”, Wiley & Sons, 1982

[Nishi01] Y. Nishikawa et al., “Direct growth of single crystalline CeO2 high-k gate dielectrics”, Ext. Abs. SSDM, pp. 174-175, 2001

[OmiUG] Omicron EA 125 Energy Analyser User’s Guide

[Ono01] H. Ono et al., Appl. Phys. Lett. 78, 1832, 2001

[Osten] H. J. Osten, “Epitaxial praseodymium oxide: a new high-k dielectric”, IWGI 2001, Tokyo

[Osten00] H.J. Osten, “High-k gate dielectrics with ultra-low leakage current based on praseodymium oxide”, IEEE, 2000

[Osten01] H.J. Osten et al., “Band gap and band discontinuities at Pr_2O_3/Si(001) heterojuctions”, Appl. Phys. Lett., vol. 80, no. 2, January 2002

[Osten02] H.J. Osten et al., “Growth of crystalline praseodymium oxide on silicon”, J. Cryst. Growth 235, pp. 229-234, 2002

[Ozone] http://www.ozoneapplications.com/info/ozone_properties.htm

[Peaco03] P.W. Peacock et al, “Behaviour of hydrogen in high dielectric constant oxide gate insulator”, Appl. Phys. Lett., vol. 83, no 10, September 2003

[Park85] E.H.C. Parker, “The technology and physics of molecular beam epitaxy”, Plenum Press, 1985

[Philips] http://www.research.philips.com/

[Ponce] F. A. Ponce, “Fault-free silicon at the silicon/sapphire interface”, Appl. Phys. Letter, vol 41, pp. 371-373, 1982

[Schmei04] D. Schmeißer et al., “Pr2O3/Si(100) interface reaction and stability”, Mat. Sc. Eng. B, 109, pp. 30-33, 2004

[Shahja02] M. Shahjaahan et al., “Fabrication and electrical characterization of ultrathin crystalline Al_2O_3 gate dielectric films on Si(100) and Si(111) by molecular beal epitaxy”, Jpn. J. Appl. Phys., vol. 41, pp. L1474-L1477, 2002

[Signo73] A. Signorelli et al., “X-ray photoelectron spectroscopy of various core levels of Lanthanide Ions: the roles of monopole exitation and electrostatic coupling”, Phys. Review B, vol. 8, no. 1, July 1973

[Simmons63] J. G. Simmons, J. Appl. Phys.; vol. 34, no. 6, June 1963

[Schlom] D.G. Schlom et al., “High-k candidates for use as gate dielectric in silicon MOSFETs”, Submitted to Applied Physics A

[Stem01] S. Stemmer et al, “Structure and stability of La_2O_3/SiO_2 layers on Si(001)”, Appl. Phys. Lett., vol 79, no 1, July 2001

[Stimpel03] T. Stimpel, F. Hutterer, H. Baumgärtner, I. Eisele, submitted to ICSi-3 Conference, Santa Fe, USA, March 2003

[Sulima03] T. Sulima, “Modification von Silizium-Grenzflächen für MOS-Technologie”, PhD Thises, June 2003

[Surface] www.lasurface.com

[Sze81] S.M. Sze, “Physics of Semiconductor Devices”, 2nd Edition, Joho Wiley & Sons, 1981

[Taur02] Taur, „CMOS design near the limit of scaling“; IBM 2002

[Uwa84] Y. Uwamino et al; J. Electron Spectrosc. Relat. Phenom. 34, 69 (1984).

[Velli04] G. Vellianitis et al., “MBE lanthanum-based high-k gate dielectrics as candidates for SiO2 gate oxide replacement”, Mat. Sci. Eng. B, 109, pp. 85-88, 2004

[Wata03] H. Watanabe et al., “La-silicate gate dielectrics fabricated by solid phase reaction between La metal and SiO_2 underlayers”, Appl. Phys. Lett., vol. 83, no. 17, October 2003

[Wilk01] G. D. Wilk et al, “High-k gate dielectric: current status and materials properties considerations”; J. Appl. Phys., vol. 89, no. 10, 2001

[Wolf04] D. Wolfframm et al, “Pulsed laser deposition of thin PrxOy films on Si(100)”, Mat. Sc. Eng. B, 109, pp. 24-29, 2004

[Wong02] H.-S. P. Wong, “Beyond the conventional transistor”, IBM J. Res. & Dev., Vol. 46 No. 2/3 March/May 2002

[Wu00] Y. H. Wu et al., IEEE Electron Device Letters, vol. 21, no. 7, 2000

[Wu02] X. Wu et al., “Characterisation of gadolinium and lanthanum oxide films on Si(100)”, J. Vac. Sci. Technol. A 20(3), May/June 2002

[Xiang03] W. Xiang et al., “Characterization of LaAlO3/Si(100) deposited under various oxygen pressure”, J. Appl. Phy., vol. 93, no. 1, January 2003

[Yang04] M.Y. Yang et al., “High-density RF MIM Capacitors Using High-k La_2O_3 Dielectrics”, J. Electrochem. Soc., 151, (7) F162-F165 (2004)

[yu02] H. Y. Yu et al. “Thermal stability of $(HfO_2)_x(Al_2O_3)_{1-x}$ on Si”, Appl. Phys. Lett. , vol. 81, no. 19, pp. 3618-3620, November 2002

[Zaum01] P. Zaumseil et al., “Structural investigation of praseodymium oxide epitaxially grown on silicon”, IHP presentation, March 2001

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- O. Blank, H. Reisinger, R. Stengl, and M. Gutsche, F. Wiest, **V. Capodieci**, J. Schulze, and I. Eisele, “A new Model for Multistep Trap-Assisted-Tunneling in Thin High-k Dielectrics”, Journal of Applied Physics, March-April 03.2005

- F. Wiest, **V. Capodieci**, O. Blank, M. Gutsche, J. Matusche and U. I. Schmidt, J. Schulze and I. Eisele, “Conformal Al_2O_3 Coating of High Aspect Ratio Structures using MOCVD”, Submitted to IEEE Electron Device Letters

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